



SLES062A - MARCH 2003 - REVISED JUNE 2012

CCD VERTICAL DRIVER FOR DIGITAL CAMERAS

Check for Samples: VSP1900

FEATURES

- CCD Vertical Driver:
 - Three Field CCD Support
 - Two Field CCD Support
- Output Drivers:
 - 3 Levels Driver (V-Transfer) x 5
 - 2 Levels Driver (V-Transfer) x 3
 - 2 Levels Driver (E-Shutter) x 1
- Driver Capability:
 - 450 pF to 1890 pF With 60 Ω to 240 Ω
- Input Phase:
 - 3 State (V-Transfer) x 5
 - 2 State (V-Transfer) x 3
 - 2 State (E-Shutter) x 1
- Portable Operation
 - Input Interface: 2.7 V to 5.5 V

- Power Supply:
 - VDD 2.7 V to 5.5 V
 - VL -5 V to -9 V
 - VM GND
 - VH 11.5V to 15.5 V

APPLICATIONS

- Digital Camera
- Video Camera

DESCRIPTION

The VSP1900 is a CCD vertical clock driver with electric-shutter support. This device is composed of eight vertical transfer channels, which support both 3-field CCD and 2-field CCD operation. The VSP1900 contributes low power consumption and device count reduction in the system.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

VSP1900



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

PACKAGING ORDERING INFORMATION⁽¹⁾

PROD	UCT	PACKAGE	PACKAGE DESIGNATOR	OPERATING TEMPERATURE RANGE	PACKAGE MARKING	ORDER NUMBER	TRANSPORT MEDIA
VSP1	900	TSSOP30	DBT	–25°C to 85°C	VSP1900	VSP1900	Tube (60 units per tube)

(1) For the most current specification and package information, refer to our web site at www.ti.com

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		VALUES	UNIT
	VDD	GND -0.3 to 7	
Supply voltage	VL	GND to -10	V
	VH	VL + 26	<u> </u>
Input voltage, V _{IN}		GND -0.3 to (VDD + 0.3)	V
Ambient temperatu	ire under bias	-25 to 85	°C
Storage temperatu	re, T _{stg}	–55 to 150	°C
Junction temperate	ure, T _J	150	°C
Package temperat	ure (IR reflow, peak)	260	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM MAX	UNIT
Supply voltage, VDD	2.7	5.5.	V
Supply voltage, VL	-5	-9	V
Supply voltage, VH	11.5	15.5	V
Input voltage, V _{IN}		GND –.03 to (VDD + 0.3)	V

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ELECTRICAL CHARACTERISTICS

All specifications at $T_A = 25^{\circ}C$ (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN ⁽¹⁾	TYP	MAX ⁽¹⁾	UNIT
	DC power consumption			5.3		mW
	Switching power consumption			550		mW
DC CH	ARACTERISTICS	·			·	
V _{IH}	High-level input voltage		0.7VDD			V
V _{IL}	Low-level input voltage				0.2VDD	V
I _{IN}	Input current	$V_{IN} = GND$ to 5 V (without pullup or pulldown resistor)	-10	0	10	μA
		V_{IN} = GND to 5 V (pullup or pulldown resistor)	-625	0	625	
I _{IH}				0.1	0.2	
I _{DD}	Operating supply current			1		mA
IIL				0.125		
I _{OL}		V1, V2, V3A, V3B, V4, V5A, V5B, V6 = -8.1 V	10			
I _{OM1}		V1, V2, V3A, V3B, V4, V5A, V5B, V6 = -0.2 V			-5	
I _{OM2}	Output ourset	V1, V3A, V3B, V5A, V5B = 0.2 V	5			
I _{OH}	Output current	V1, V3A, V3B, V5A, V5B = 14.55 V		-7.2	mA	
I _{OSL}		SUB = -8.1 V	5.4			
I _{OSH}		SUB = 14.55 V			-4	

(1) Specified by design

SWITCHING CHARACTERISTICS

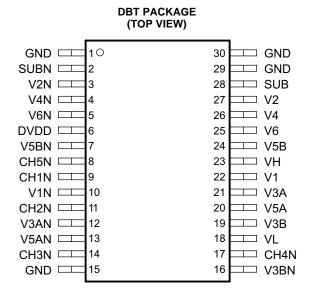
All specification at TA = 25°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN ⁽¹⁾	TYP	MAX ⁽¹⁾	UNIT
t _{d(PLM)}				15	100	
t _{d(PMH)}				20	100	
t _{d(PLH)}	Propagation delay time			20	100	20
t _{d(PML)}	Propagation delay time			15	50	ns
t _{d(PHM)}				30	50	
t _{d(PHL)}				30	50	
t _{r(TLM)}		$VL \rightarrow VM$			300	
t _{r(TMH)}	Rise time	$VM \rightarrow VH$			300	ns
t _{r(TLH)}		$VL \rightarrow VH$			300	
t _{f(TML)}		$VM \rightarrow VL$			300	
t _{f(THM)}	Fall time	$VH \rightarrow VM$			300	ns
t _{f(THL)}		$VH\toVL$			300	
V _{n(CLH)}						
V _{n(CLL)}						
V _{n(CMH)}	Output noise voltage				2	V
V _{n(CML)}						
V _{n(CHL)}						

(1) Specified by design



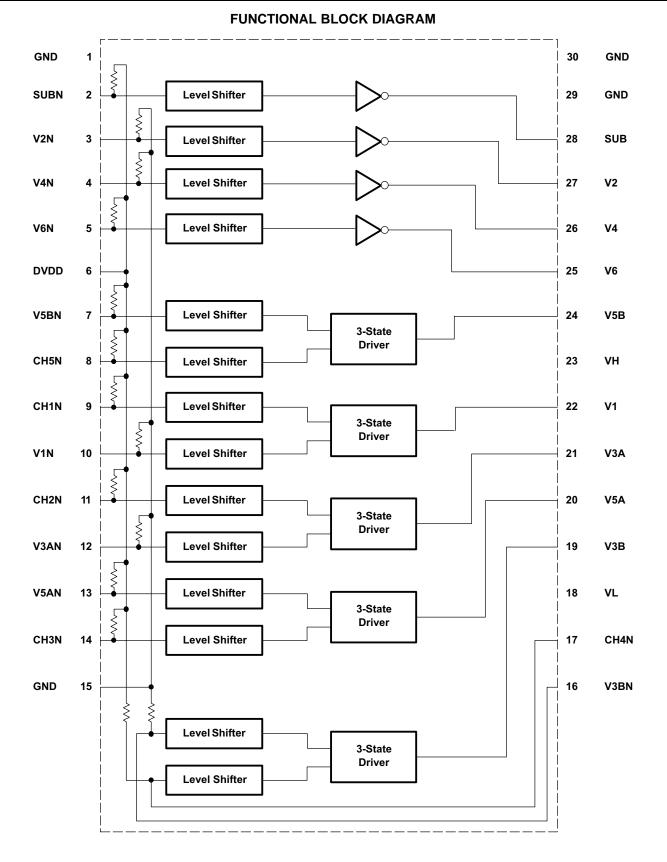
PIN ASSIGNMENTS



TERMINAL FUNCTIONS

TERMINAL		TVDE	DECODIDITION		
NAME	NO.	TYPE	DESCRIPTION		
GND	1, 15, 29, 30	Р	Ground		
SUBN	2	DI	CCD substrate clock SUB input		
V2N	3	DI	Vertical transfer clock 2 input		
V4N	4	DI	Vertical transfer clock 4 input		
V6N	5	DI	Vertical transfer clock 6 input		
DVDD	6	Р	Digital power supply		
V5BN	7	DI	Vertical transfer clock 5B input		
CH5N	8	DI	Read out clock 5 input		
CH1N	9	DI	Read out clock 1 input		
V1N	10	DI	Vertical transfer clock 1 input		
CH2N	11	DI	Read out clock 2 input		
V3AN	12	DI	Vertical transfer clock 3A input		
V5AN	13	DI	Vertical transfer clock 5A input		
CH3N	14	DI	Read out clock 3 input		
V3BN	16	DI	Vertical transfer clock 3B input		
CH4N	17	DI	Read out clock 4 input		
VL	18	Р	Output driver power supply		
V3B	19	DO	Vertical transfer clock 3B output		
V5A	20	DO	Vertical transfer clock 5A output		
V3A	21	DO	Vertical transfer clock 3A output		
V1	22	DO	Vertical transfer clock 1 output		
VH	23	Р	Output driver power supply		
V5B	24	DO	Vertical transfer clock 5B output		
V6	25	DO	Vertical transfer clock 6 output		
V4	26	DO	Vertical transfer clock 4 output		
V2	27	DO	Vertical transfer clock 2 output		
SUB	28	DO	CCD substrate clock SUB output		





VSP1900

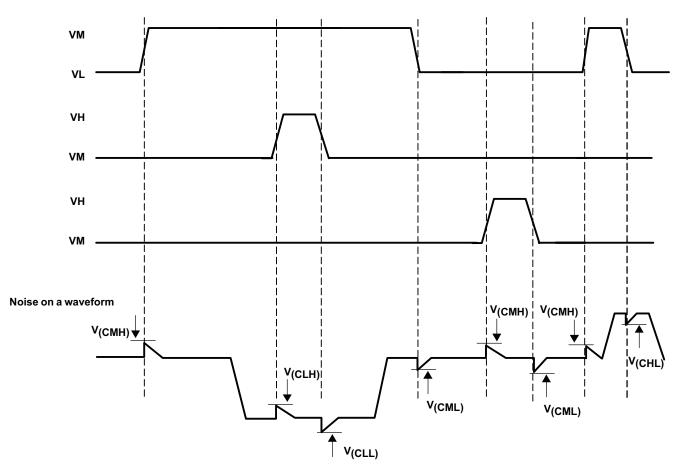
TEXAS INSTRUMENTS

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			TRUTH TABLE				
	IN	PUT		OUTPUT			
V1N	CH1N			V1			
V3AN	CH2N			V3A			
V3BN	CH4N	V2N		V3B	V2		
V5AN	CH3N	V4N		V5A	V4		
V5BN	CH5N	V6N	SUBN	V5B	V6	SUBN	
L	L	Х	Х	VH	Х	Х	
L	н	Х	Х	VM	Х	Х	
Н	L	Х	X	Z	Х	Х	
Н	н	Х	Х	VL	Х	Х	
Х	Х	L	Х	Х	VM	X	
Х	Х	Н	X	Х	VL	Х	
Х	Х	Х	L	Х	Х	VH	
Х	Х	Х	н	Х	Х	VL	

SWITCHING WAVEFORM





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LOADING DIAGRAM

	R1, R2, R4, R6	60 Ω
Vertical clock series resistor	R3A, R5A	240 Ω
	R3B, R5B	80 Ω
	CΦV1	1280 pF
Vertical cleak to CND	CΦV3A, CΦV3B	640 pF
Vertical clock to GND	СФV5А, СФV5В	640 pF
	CΦV2, CΦV4, CΦV6	400 pF
	СФV12	510 pF
	СФV23А, СФV23В	50 pF
Detunen vertical deals	СФV45А, СФV45В	50 pF
Between vertical clock	СФV3А4, СФV3В4	260 pF
	СФV5А6, СФV5В6	260 pF
	СФV61	100 pF
Substrate clock to GND	CΦVSUB	1000 pF
Vertical clock GND resistor	R GND	18 Ω

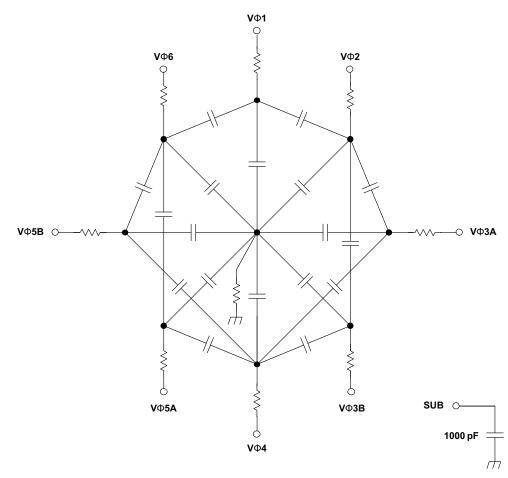


Figure 1. VSP1900 Loading Diagram

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DESCRIPTION

The VSP1900 is a CCD vertical clock driver with electric shutter. The VSP1900 is composed of five 3-state and three 2-state vertical transfer channels, which support both 3 field and 2 field CCD operation. The VSP1900 contributes low power consumption and parts number reduction in the system.

OPERATION

Power On/Off Sequence

This is the same as the CCD power up sequence, when power on, VDD powers on first VH, VM powers on second, and VL powers on later. When powering off, VL powers off first, VH, VM powers off second, and VDD powers off later.

Vertical Transfer Signal

The VSP1900 receives signals from TG (CCD timing generator). The input signal is converted into the operating voltage levels of the CCD by the level shifter. The level shifter circuits connect to a 2-state or 3-state driver, which is connected to the CCD input pin. While using a 2-field CCD, one of the 3-state drivers is used as a 2-state driver. The CH#N pin is pulled up internally, so that the VH level does not appear on the output pin.

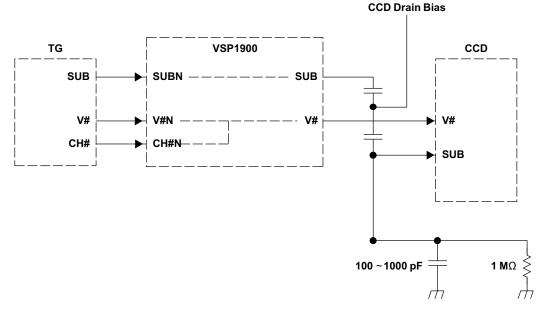


Figure 2. VSP1900 Circuit Application

REVISION HISTORY

Cł	nanges from Original (March 2003) to Revision A	Page
•	Changed the last sentence of the Description From: "part number reduction in the system." To: " device count reduction in the system.	1
•	Deleted the Tape and reel option from the Ordering Information Table	2
•	Changed the Package temperature value From 2.35°C to 260°C	2
•	Added Table Note " Specified by Design" to the MIN and MAX columns of the ELECTRICAL CHARACTERISTICS and SWITCHING CHARACTERISTICS.	3
•	Changed the Truth Table	6



11-Apr-2013

PACKAGING INFORMATION

Orderable Device	Status	Package Type	•	Pins	Package	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Top-Side Markings	Samples
	(1)		Drawing		Qty	(2)		(3)		(4)	
VSP1900DBT	ACTIVE	TSSOP	DBT	30	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 85	VSP1900	Samples
VSP1900DBTG4	ACTIVE	TSSOP	DBT	30	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 85	VSP1900	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between

the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

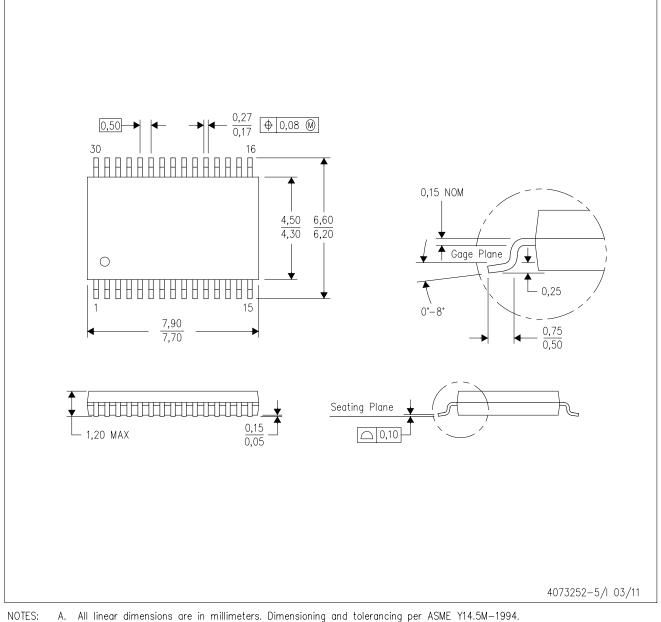
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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DBT (R-PDSO-G30)

PLASTIC SMALL OUTLINE



B. This drawing is subject to change without notice.

- C. Body dimensions do not include mold flash or protrusion.
- D. Falls within JEDEC MO-153.



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