

Thyristor/Diode and Thyristor/Thyristor (SUPER MAGN-A-PAK Power Modules), 430 A



SUPER MAGN-A-PAK

PRODUCT SUMMARY				
I _{T(AV)}	430 A			
Туре	Modules - Thyristor, Standard			
Package	SMAP			
Circuit	Two SCRs doubler circuit			

FEATURES

- · High current capability
- · High surge capability
- High voltage ratings up to 2000 V
- 3000 V_{RMS} isolating voltage with non-toxic substrate
- Industrial standard package
- UL approved file E78996
- Material categorization: For definitions of compliance please see <u>www.vishay.com/doc?99912</u>

TYPICAL APPLICATIONS

- Motor starters
- DC motor controls AC motor controls
- Uninterruptible power supplies
- Wind mill

MAJOR RATINGS AND CHARACTERISTICS				
SYMBOL	CHARACTERISTICS VALUES		UNITS	
I _{T(AV)}	T _C = 82 °C	430	_ A	
I _{T(RMS)}	T _C = 82 °C	675	^	
I	50 Hz	15.7	kA	
I _{TSM}	60 Hz	16.4	, KA	
10.	50 Hz	1232	kA ² s	
l ² t	60 Hz	1125	KA-S	
I ² √t		12 320	kA²√s	
V _{RRM}	Range	1600 to 2000	V	
T _J	Range	- 40 to 150	°C	
T _{Stg}	Range	- 40 to 130		

ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS							
TYPE NUMBER	VOLTAGE CODE	V _{RRM} /V _{DRM} , MAXIMUM REPETITIVE PEAK REVERSE VOLTAGE V	V _{RSM} , MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	$\begin{aligned} &I_{RRM}/I_{DRM} \text{ MAXIMUM} \\ &AT T_J = T_J \text{ MAXIMUM} \\ & \text{mA} \end{aligned}$			
	16	1600	1700				
VSK.430	18	1800	1900	100			
	20	2000	2100				



PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS			
Maximum average on-state current	I _{T(AV),}	180° conduction, half sine wave		I _{T(AV)} , 1000 and 1	alter half days and		430	Α
at case temperature	I _{F(AV)}	180° condu	ction, nair sine v	vave	82	°C		
Maximum RMS on-state current	I _{T(RMS)}	180° condu	ction, half sine w	vave at T _C = 82 °C	675	Α		
		t = 10 ms	No voltage		15.7			
Maximum peak, one-cycle,	I _{TSM} ,	t = 8.3 ms	reapplied		16.4	1. 4		
non-repetitive surge current	I _{FSM}	t = 10 ms	100 % V _{RRM}		13.2	kA		
		t = 8.3 ms	reapplied	Sinusoidal half wave,	13.8	ı		
Maximum I ² t for fusing	t = 8.3 ms reapplies $t = 10 ms$ t	No voltage	initial $T_J = T_J$ maximum	1232				
		t = 8.3 ms	reapplied	<u> </u>	1125	kA ² s		
		t = 10 ms	100 % V _{RRM}		871			
		t = 8.3 ms	reapplied		795			
Maximum I ² √t for fusing	I ² √t	t = 0.1 ms to 10 ms, no voltage reapplied		12 320	kA²√s			
Low level value of threshold voltage	V _{F(TO)1}	(16.7 % x π x I _{T(AV)} < I < π x I _{T(AV)}), T _J = T _J maximum		0.96	V			
High level value of threshold voltage	V _{F(TO)2}	$(I > \pi \times I_{T(AV)}), T_J = T_J \text{ maximum}$		1.06	V			
Low level value of on-state slope resistance	r _{f1}	(16.7 % x π	(16.7 % x π x $I_{T(AV)} < I < \pi$ x $I_{T(AV)}$), $T_J = T_J$ maximum					
High level value of on-state slope resistance	r _{f2}	$(I > \pi \times I_{T(AV)}), T_J = T_J \text{ maximum}$		0.45	mΩ			
Maximum on-state voltage drop	V _{TM}	I_{pk} = 1500 A, T_J = 25 °C, t_p = 10 ms sine pulse		1.65	V			
Maximum forward voltage drop	V_{FM}	I_{pk} = 1500 A, T_J = 25 °C, t_p = 10 ms sine pulse		1.65	V			
Maximum holding current	I _H	T 05:00 1 140V 111 1		500	A			
Typical latching current	ΙL	T _J = 25 °C, anode supply 12 V resistive load		1000	mA			

SWITCHING					
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS	
Maximum rate of rise of turned-on current	dl/dt	T _J = T _J maximum, I _{TM} = 400 A, V _{DRM} applied	1000	A/µs	
Typical delay time	t _d	Gate current 1 A, $dI_g/dt = 1 A/\mu s$ $V_d = 0.67 \% V_{DRM}$, $T_J = 25 °C$	2.0	110	
Typical turn-off time	t _q	I_{TM} = 750 A, T_J = T_J maximum, dI/dt = - 60 A/ μ s V_R = 50, dV/dt = 20 V/ μ s, Gate 0 V 100 Ω	200	μs	

BLOCKING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum critical rate of rise of off-state voltage	dV/dt	T_J = 130 °C, linear to V_D = 80 % V_{DRM}	1000	V/µs
RMS insulation voltage	V _{INS}	t = 1 s	3000	V
Maximum peak reverse and off-state leakage current	I _{RRM} , I _{DRM}	$T_J = T_J$ maximum, rated V_{DRM}/V_{RRM} applied	100	mA



THERMAL AND MECHANICAL SPECIFICATIONS				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum junction operating temperature range	TJ		- 40 to 130	°C
Maximum storage temperature range	T _{Stg}		- 40 to 150	
Maximum thermal resistance, junction to case per junction	R _{thJC}	DC operation	0.065	K/W
Maximum thermal resistance, case to heatsink	R _{thC-hs}		0.02	N/VV
SMAP to heatsink		A mounting compound is recommended and	6 to 8	
Mounting torque ± 10 % busbar to SMAF		the torque should be rechecked after a period of 3 hours to allow for the spread of the compound.	12 to 15	Nm
Approximate weight			1500	g
Case style		See dimensions - link at the end of datasheet	ns - link at the end of datasheet SUPER MAGN-A-PAK	

△R _{thJC} CONDUCTION				
CONDUCTION ANGLE	SINUSOIDAL CONDUCTION	RECTANGULAR CONDUCTION	TEST CONDITIONS	UNITS
180°	0.009	0.006		
120°	0.011	0.011		
90°	0.014	0.015	$T_J = T_J$ maximum	K/W
60°	0.021	0.022		
30°	0.037	0.038		

Note

• The table above shows the increment of thermal resistance R_{thJC} when devices operate at different conduction angles than DC

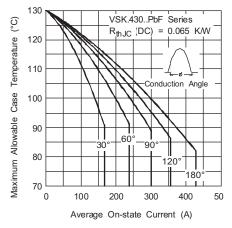


Fig. 1 - Current Ratings Characteristics

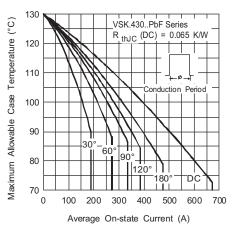


Fig. 2 - Current Ratings Characteristics

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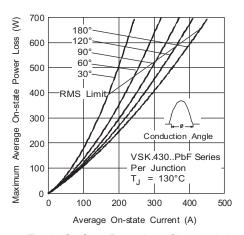


Fig. 3 - On-State Power Loss Characteristics

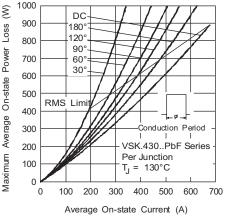


Fig. 4 - On-State Power Loss Characteristics

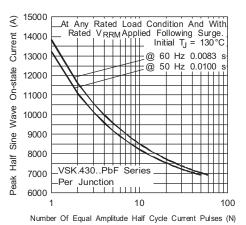


Fig. 5 - Maximum Non-Repetitive Surge Current

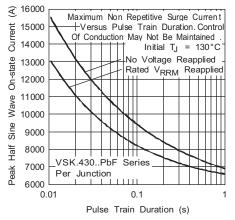


Fig. 6 - Maximum Non-Repetitive Surge Current

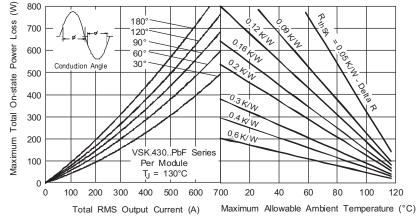


Fig. 7 - On-State Power Loss Characteristics

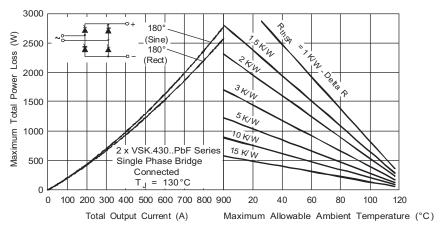


Fig. 8 - On-State Power Loss Characteristics

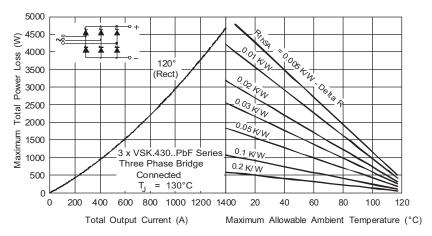


Fig. 9 - On-State Power Loss Characteristics

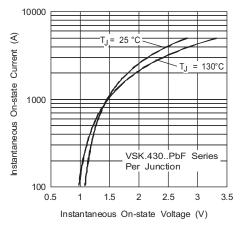


Fig. 10 - On-State Voltage Drop Characteristics

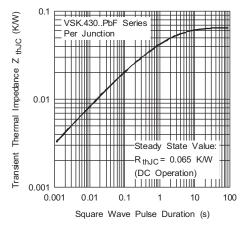


Fig. 11 - Thermal Impedance Z_{thJC} Characteristics

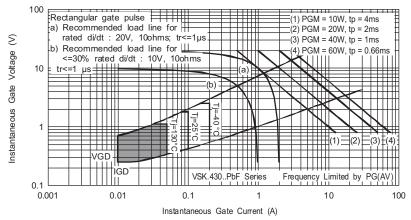
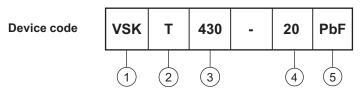


Fig. 12 - Gate Characteristics

ORDERING INFORMATION TABLE



1 - Module type

2 - Circuit configuration (see end of datasheet)

3 - Current rating

- Voltage code x 100 = V_{RRM} (see Voltage Ratings table)

5 - Lead (Pb)-free

Note

• To order the optional hardware go to www.vishay.com/doc?95172

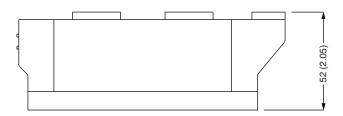
CIRCUIT CONFIGU	RATION			
CIRCUIT DESCRIPTION	CIRCUIT CONFIGURATION CODE		CIRCUIT DRAWING	
		VSKT	VSKH	VSKL
Two SCRs doubler circuit	Т	0+ 2 30-7 4, 7 (K1) (K2) 5 (G1) 6 (G2)	2 + 2 + (K1)	7 (K2) O 6 (G2)

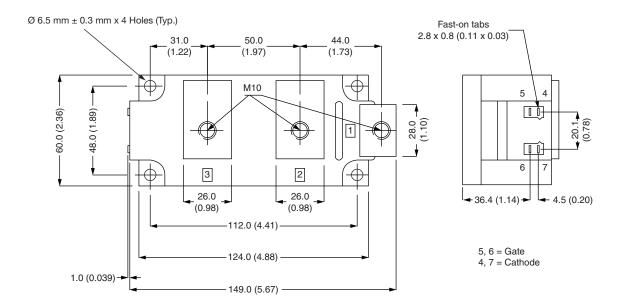
LINKS TO RELATED DOCUMENTS				
Dimensions	www.vishay.com/doc?95283			



Super MAGN-A-PAK Thyristor/Diode

DIMENSIONS in millimeters (inches)







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