

# MCPC Compatible USB Port Multimedia Switch Supports USB, UART, Audio, ID, MIC, and Load Switch

Check for Samples: [TSU6721YFF](#)

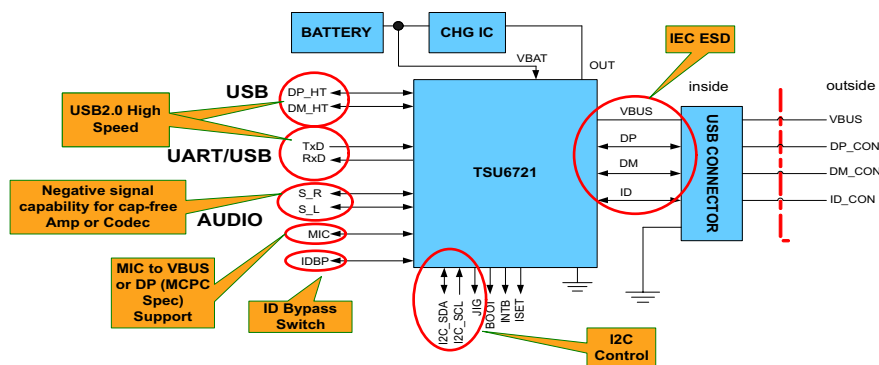
## FEATURES

- **Switch Matrix**
  - USB and UART Switch support USB 2.0 HS
  - Audio Switch with Negative Signal Capability
  - ID Bypass Switch
  - VBUS to MIC Switch
  - DP to MIC Switch to Support MCPC
- **Load Switch**
  - 100 mΩ Load Switch
  - OTG Support
  - 28 V VBUS Rating with Over-voltage Protection
  - Programmable Overcurrent Limiter/Protection
- **Charger Detection**
  - USB BCDv1.2 compliant
  - VBUS Detection
  - Data Contact Detection
  - Primary and Secondary Detection
- **Compatible Accessories**
  - USB Chargers (DCP, CDP)
  - Apple Charger
  - USB Data Port
  - Audio Headset with MIC and Remote
  - Docking Support
  - Factory Cable
- **Additional Features**
  - I2C Interface with Host Processor
  - Switches Controlled by Automatic Detection or Manual Control
  - Interrupts Generated for Plug/Unplug
  - Decoupling FET Switch to VBUS Added to Reduce Degradation on MIC Line
  - Support Control Signals used In Manufacturing (JIG, BOOT)
- **ESD Performance Tested Per JESD 22**
  - 4000-V Human-Body Model (A114-B, Class II)
  - 1500-V Charged-Device Model (C101)
- **IEC ESD Performance**
  - ±8 kV Contact Discharge (IEC 61000-4-2) for VBUS/DP/DM/ID to GND

## APPLICATIONS

- Cell Phones and Smart Phones
- Tablet PCs
- Digital Cameras and Camcorders
- GPS Navigation Systems
- Micro USB Interface with USB/UART/AUDIO

## APPLICATION DIAGRAM



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ORDERING INFORMATION

For package and ordering information, see the Package Option Addendum at the end of this document.

## DESCRIPTION

TSU6721 is a high performance USB port multimedia switch featuring automatic switching and accessory detection. The device connects a common USB port to pass audio, USB data, charging, On The Go (OTG) and factory mode signals. The audio path has negative signal capability includes left (mono/stereo), right (stereo) as well as microphone signals. Furthermore, TSU6721 is compatible with the MCPC specification.

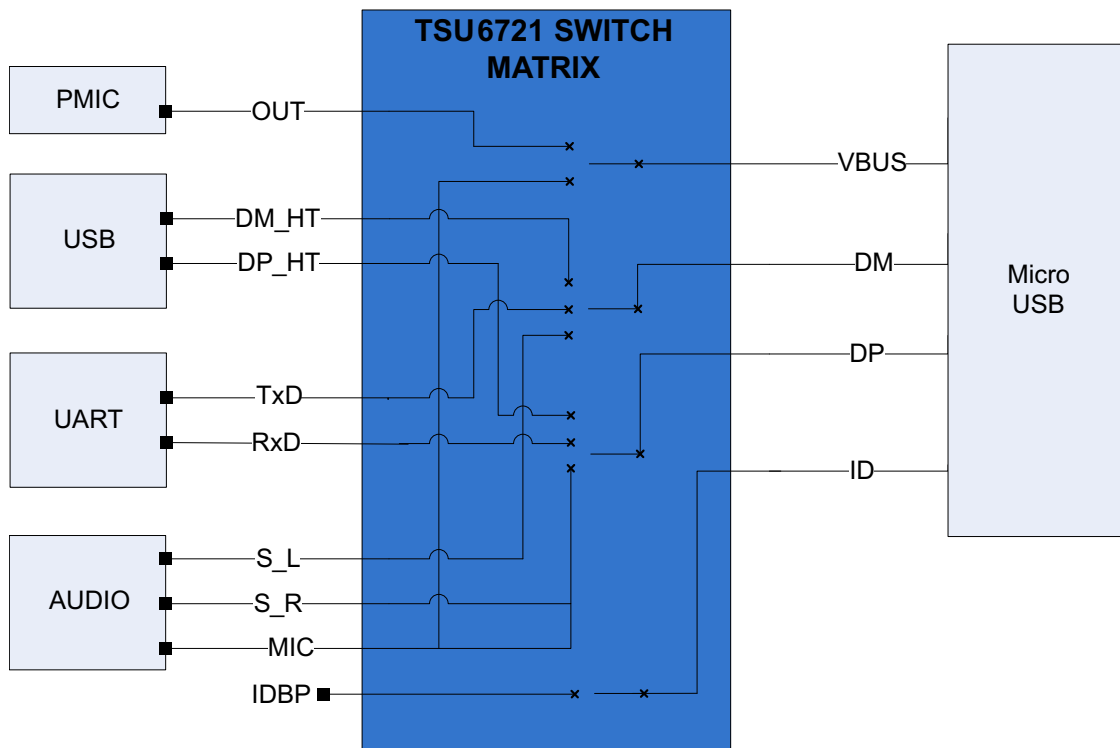
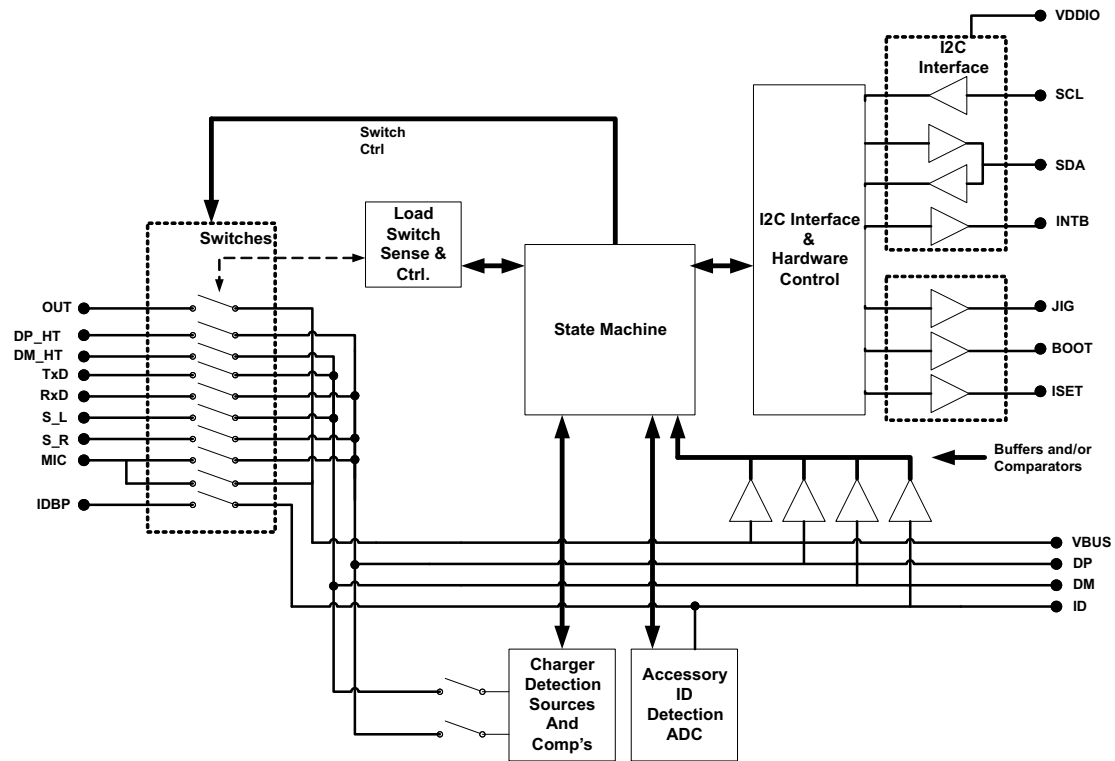
TSU6721 features impedance detection which supports the detection of various accessories that are attached through DP, DM and ID pins of the USB connector. The switch is controlled by automatic switching or manually through I<sup>2</sup>C.

TSU6721 has an integrated low resistive Load Switch that is used to isolate the charger from the external connector. OverVoltage Protection and programmable OverCurrent Limiter/Protection are additional features included to the Load Switch.

The charger detection satisfies USB charger specification v1.2. In addition to DCP, CDP and SDP, the device also detects Apple Chargers.

Power for this device is supplied through VBAT of the system or through VBUS when attached. TSU6721 supports factory mode testing when a USB/UART JIG cable is used in development and manufacturing.

## BLOCK DIAGRAM

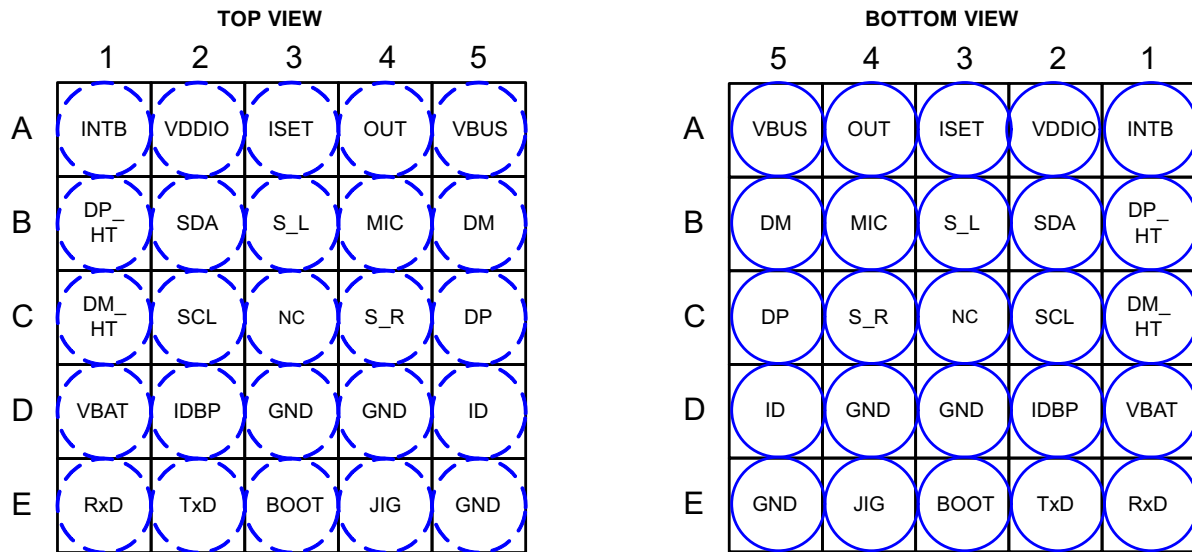


# TSU6721YFF

SCDS345 – JUNE 2013

[www.ti.com](http://www.ti.com)

## PIN OUT



## PIN FUNCTIONS

BALL NO.	PIN NAME	TYPE	DESCRIPTION
D1	VBAT	–	3.0 – 4.4V Battery supply voltage
A2	VDDIO	–	1.8 ~ 3.3V Logic Supply
A5	VBUS	I	USB connector VBUS
A4	OUT	O	Phone charger output
E5, D3, D4	GND	–	Ground
B1	DP-HT	I/O	USB data plus
C1	DM-HT	I/O	USB data minus
D2	IDBP	I/O	USB ID data
E1	RxD	I/O	UART receive data
E2	TxD	I/O	UART transmit data
C3	NC	–	Not connected internally
B4	MIC	I/O	Microphone signal
C4	S_R	I/O	Stereo headset right sound
B3	S_L	I/O	Mono or stereo headset left sound
C2	SCL	I	I2C clock
B2	SDA	I/O	I2C data
C5	DP	I/O	Common USB connector plus I/O port
B5	DM	I/O	Common USB connector minus I/O port
D5	ID	I/O	Common USB connector ID I/O port
A1	INTB	O	Interrupt signal when peripheral is plugged/unplugged. Push-pull output
A3	ISSET	O	High current charger detected. Open-drain output
E4	JIG	O	GPIO factory output. Open-drain output
E3	BOOT	O	GPIO factory output. Push-pull output

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
VBUS	Supply voltage from USB connector		−0.5	28	V
VBAT	Supply voltage from battery		−0.5	6	V
VDDIO	Logic supply voltage		−0.5	4.6	V
VBUS_OUT	Phone charger output		−0.5	7	V
DP	DP Connector voltage		−0.5	VBAT+0.5	V
DM	DM Connector voltage		−0.5	VBAT+0.5	V
ID	ID Connector voltage		−0.5	VBAT+0.5	V
IDBP	ID Host Side voltage		−0.5	VBAT+0.5	V
VAUDIO	Switch I/O voltage range	Audio Switch (S_L, S_R)	−1.5	VBAT+0.5	V
VMIC		Mic Switch (MIC)	−0.5	VBAT+0.5	
VUSB/VUART		USB/UART Switch	−0.5	VBAT+0.5	
VJIG & VISET	JIG and ISET voltage		−0.5	VBAT+0.5	V
VLOGIC_O	Voltage applied to logic output (SCL, SDA, INTB, BOOT)		−0.5	VDDIO	V
IBUS	Peak input current on VBUS pin (12.5% duty cycle)			2.0	A
	Peak input current on VBUS pin (3% duty cycle, 4ms on-time)			2.5	
IBUS_OUT	Peak input current on VBUS pin (12.5% duty cycle)			2.0	A
	Peak input current on VBUS pin (3% duty cycle, 4ms on-time)			2.5	
I <sub>ISET</sub> & I <sub>JIG</sub>	ISET and JIG pins peak current			50	mA
IK	Analog port diode current		−50	50	mA
ISW-DC	ON-state continuous switch current		−60	60	mA
ISW-_ PEAK	ON-state peak switch current		−150	150	mA
IIK	Digital logic input clamp current	VDDIO < 0		−50	mA
ILOGIC_O	Continuous current through logic output (SCL, SDA, INTB, BOOT)		−50	50	mA
IGND	Continuous current through GND			100	mA
Tstg	Storage temperature range		−65	150	°C

## THERMAL IMPEDANCE RATINGS

		VALUE	UNIT
$\theta_{JA}$	Package thermal impedance	98.8	°C/W

## SUMMARY OF TYPICAL CHARACTERISTICS

AMBIENT TEMPERATURE = 25°C	USB/UART PATH	AUDIO PATH	MIC PATH
Number of channels	2	1	1
ON-state resistance ( $r_{on}$ )	6 $\Omega$ / 7 $\Omega$ (USB/UART)	2.5 $\Omega$	40 $\Omega$
ON-state resistance match ( $\Delta r_{on}$ )	0.2 $\Omega$ / 1.5 $\Omega$	0.15 $\Omega$	N/A
ON-state resistance flatness ( $r_{on(flat)}$ )	1.4 $\Omega$ / 1.4 $\Omega$	0.15 $\Omega$	N/A
Turn-on/Turn-off time ( $t_{ON}/t_{OFF}$ )	130 $\mu$ s/ 100 $\mu$ s	200 $\mu$ s/100 $\mu$ s	260 $\mu$ s /180 $\mu$ s
Bandwidth (BW)	510 MHz	450MHz	250 MHz
OFF isolation ( $O_{ISO}$ )	−26 dB at 250 MHz	−100 dB	−95 dB
Crosstalk ( $X_{TALK}$ )	−32 dB at 250 MHz	−85 dB	−85 dB
Total Harmonic Distortion (THD)	N/A	0.05%	0.46%
Leakage current ( $I_{IO(ON)}$ )	50 nA	200 nA	5 nA

# TSU6721YFF

SCDS345 –JUNE 2013

[www.ti.com](http://www.ti.com)

## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	MIN	MAX	UNITS
V <sub>BUS</sub>	VBUS voltage	4.0	6.5	V
V <sub>BAT</sub>	VBAT voltage	3.0	4.4	V
V <sub>DDIO</sub>	VDDIO voltage	1.65	3.6	V
ID_Cap	ID capacitance		3	nF
USB_I/O	USB path signal range	0	3.6	V
UART_I/O	UART path signal range	0	2.7	V
Audio_I/O	Audio path signal range	–1.5	1.5	V
MIC_I/O	MIC path signal range	0	2.3	V
Temperature	Operating Temperature	–40	85	°C

## ELECTRICAL SPECIFICATIONS

### DIGITAL SIGNALS – I<sup>2</sup>C INTERFACE (SCL and SDA)

T<sub>A</sub> = –40°C to 85°C, Typical values are at T<sub>A</sub> = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
V <sub>DDIO</sub> Logic and I/O supply voltage		1.65	3.6	V
V <sub>IH</sub> High-level input voltage		V <sub>DDIO</sub> × 0.7	V <sub>DDIO</sub>	V
V <sub>IL</sub> Low-level input voltage		0	V <sub>DDIO</sub> × 0.3	V
V <sub>OH</sub> SDA High-level output voltage	I <sub>OH</sub> = –3 mA	V <sub>DDIO</sub> × 0.7		V
V <sub>OL</sub> SDA Low-level output voltage	I <sub>OL</sub> = 3 mA	0	0.4	V
f <sub>SCL</sub> SCL frequency			400	kHz

### JIG AND ISET FAST-MODE CHARGER OUTPUT (OPEN-DRAIN OUTPUT)

T<sub>A</sub> = –40°C to 85°C, Typical values are at T<sub>A</sub> = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
VOL_JIG Low-level output voltage	I <sub>OL</sub> = 10 mA, VBAT = 3.0 V	0	0.5	V
VOL_ISET Low-level output voltage	I <sub>OL</sub> = 10 mA, VBAT = 3.0 V	0	0.7	V

### INTB AND BOOT (PUSH-PULL OUTPUT)

T<sub>A</sub> = –40°C to 85°C, Typical values are at T<sub>A</sub> = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
V <sub>OH</sub> High-level output voltage	I <sub>OH</sub> = –4 mA, VDDIO = 1.65 V	1.16	V <sub>DDIO</sub>	V
V <sub>OL</sub> Low-level output voltage	I <sub>OL</sub> = 4 mA, VDDIO = 1.65 V	0	0.33	V

## TOTAL SWITCH CURRENT CONSUMPTION

T<sub>A</sub> = –40°C to 85°C, Typical values are at T<sub>A</sub> = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
IBAT(Standby) VBAT Standby Current Consumption	VBUS = 0 V, Idle state		36	50	μA
IBAT(Operating) VBAT Operating Current Consumption	VBUS = 0 V, USB switches ON		60	80	μA
IVBUS VBUS Operating Current Consumption	No load on OUT pin, VBUS = 5 V		135	155	μA

## VBUS CAP SWITCH CHARACTERISTICS

T<sub>A</sub> = –40°C to 85°C, Typical values are at T<sub>A</sub> = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
RDS-VBUSCAP VBUS CAP switch resistance	VBUS = 5 V, IOUT = –20 mA		90		Ω

## VOLTAGE PROTECTION

 $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ , Typical values are at  $T_A = 25^{\circ}\text{C}$  (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>VBUS_UVLO</sub>	V <sub>BUS</sub> under voltage+	Voltage is Rising, device power-up	3.0	3.25	3.6	V
	V <sub>BUS</sub> under voltage–	Voltage is Falling, device reset	2.7	3	3.3	
V <sub>VBUS_VALID</sub>	V <sub>BUS</sub> interrupt threshold	Voltage is Rising		3.6		V
V <sub>VBAT_UVLO</sub>	V <sub>BAT</sub> under voltage+	Voltage is Rising, device power-up	2.5	2.8	3.1	V
	V <sub>BAT</sub> under voltage–	Voltage is Falling, device reset	2.3	2.6	2.9	

## LOAD SWITCH CHARACTERISTICS

 $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ , Typical values are at  $T_A = 25^{\circ}\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
RDS-VBUSSWITCH	VBUS switch resistance	VBUS = 5 V, IOUT = 100 mA		90		150	mΩ
tONa	Turn-ON time automatic mode	RL = 36 Ω, CL = 400 pF, Vbus rising > 3.6V		175			ms
tOFFa	Turn-OFF time automatic mode	RL = 36 Ω, CL = 400 pF, Vbus falling < 3.6V		2.5			ms
tONm	Turn-ON time manual mode	RL = 36 Ω, CL = 400 pF, From receipt of I2C ACK bit		230			μs
tOFFm	Turn-OFF time manual mode	RL = 36 Ω, CL = 400 pF, From receipt of I2C ACK bit		180			μs
IOCP	Programmable overcurrent protection	VBUS = 5.5V	I2C reg0x22h, Bit [2:0] = 000	0.8	1.0	1.2	A
			I2C reg0x22h, Bit [2:0] = 001 (default)	1.3	1.5	1.7	
			I2C reg0x22h, Bit [2:0] = 010	2.0			
			I2C reg0x22h, Bit [2:0] = 011	2.0			
IOCL	Programmable overcurrent limiter	VBUS = 5.5V	I2C reg0x21h, Bit [7:5] = 000	1.25	1.5	1.75	A
			I2C reg0x21h, Bit [7:5] = 001 (default)	1.67	2.0	2.33	
			I2C reg0x21h, Bit [7:5] = 010	2.5			
			I2C reg0x21h, Bit [7:5] = 011	2.5			
VBUS OVERVOLTAGE PROTECTION (OVP)							
VBUS VOVP	Input overvoltage protection threshold	VBUS increasing from 6 V to 8 V		6.8	7	7.2	V
VBUS tOFF(OVP)	OVP delay	Delay from VBUS > VOVP to Load switch OFF		200			μs
VBUS VHYS-OVP	Hysteresis on OVP	VBUS decreasing from 8 V to 6 V		140			mV
VBUS tON(OVP)	Recovery time from input overvoltage condition	Delay from VBUS < VOVP-VHYS, to Load switch ON		9			ms
OTP rOTP	OTP Rising Turn Off	Temperature rising until load switch shut off		130			°C
OTP fOTP	OTP Falling Turn On	Temperature falling after OTP shutoff until switch turn on		120			°C

# TSU6721YFF

SCDS345 –JUNE 2013

[www.ti.com](http://www.ti.com)

## AUDIO SWITCH ELECTRICAL CHARACTERISTICS<sup>(1)(2)</sup>

 $V_{BAT} = 3.0\text{ V to }4.4\text{ V}$ ,  $V_{DDIO} = 2.8\text{ V}$ ,  $T_A = -40^{\circ}\text{C to }85^{\circ}\text{C}$ , Typical values are at  $T_A = 25^{\circ}\text{C}$  (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>ANALOG SWITCH</b>							
$V_{AUDIO}$	Audio signal range			-1.5		3	V
$r_{ON}$	ON-state resistance	S_L or S_R, DM or DP	$V_I = \pm 0.8\text{ V}$ , $I_O = -20\text{ mA}$ , $V_{BAT} = 3.0\text{ V}$		2.5	5	$\Omega$
$\Delta r_{ON}$	ON-state resistance match between channels		$V_I = 0.8\text{ V}$ , $I_I = -20\text{ mA}$ , $V_{BAT} = 3.0\text{ V}$		0.15	0.5	$\Omega$
$r_{ON(Flat)}$	ON-state resistance flatness		$V_I = \pm 0.8\text{ V}$ , $I_O = -20\text{ mA}$ , $V_{BAT} = 3.0\text{ V}$		0.15	0.5	$\Omega$
$I_{IO(OFF)}$	$V_I$ or $V_O$ OFF leakage current		$(V_I = -0.8\text{ V}$ , $V_O = 0.8\text{ V})$ or $(V_I = 0.8\text{ V}$ , $V_O = -0.8\text{ V})$ , $V_{BAT} = 4.4\text{ V}$ , Switch OFF		200	500	nA
$I_{IO(ON)}$	VO ON leakage current		$V_I = \text{OPEN}$ , $V_O = -0.8\text{ V}$ or $0.8\text{ V}$ , $V_{BAT} = 4.4\text{ V}$ , Switch ON		10	300	nA
<b>DYNAMIC</b>							
$t_{ON}$	Turn-ON time	From receipt of I <sup>2</sup> C ACK bit	$V_I$ or $V_O = V_{BAT}$ , $R_L = 100\ \Omega$ , $C_L = 35\text{ pF}$		200		$\mu\text{s}$
$t_{OFF}$	Turn-OFF time				100		
$C_{I(OFF)}$	VI OFF capacitance		DC bias = 0 V or 1.6 V f = 10 MHz, Switch OFF		5.5		pF
$C_{O(OFF)}$	VO OFF capacitance				10		pF
$C_{I(ON)}$ , $C_{O(ON)}$	VI, VO ON capacitance		DC bias = 0 V or 1.6 V f = 10 MHz, Switch ON		13		pF
BW	Bandwidth		$R_L = 50\ \Omega$ , Switch ON		450		MHz
$O_{ISO}$	OFF Isolation		f = 20 kHz, $R_L = 50\ \Omega$ , Switch OFF		-100		dB
$X_{TALK}$	Crosstalk		f = 20 kHz, $R_L = 50\ \Omega$		-85		dB
THD	Total harmonic distortion		$R_L = 16\ \Omega$ , $C_L = 20\text{ pF}$ , f = 20 Hz–20 kHz, 1.6 V <sub>pp</sub> output		0.05		%
			$R_L = 16\ \Omega$ , $C_L = 20\text{ pF}$ , f = 20 Hz–20 kHz, 3 V <sub>pp</sub> output		0.1		%

(1)  $V_I$  is equal to the asserted voltage on S\_R and S\_L pins.  $V_O$  is equal to the asserted voltage on DP and DM pins.  $I_I$  is equal to the current on the S\_R and S\_L pins.  $I_O$  is equal to the current on the DP and DM pins

(2) Audio Switch is intended for signals to be asserted on S\_R/S\_L pins and pass to DM/DP



## MIC SWITCH ELECTRICAL CHARACTERISTICS<sup>(1)</sup>

$V_{BAT} = 3.0\text{ V}$  to  $4.4\text{ V}$ ,  $V_{DDIO} = 2.8\text{ V}$ ,  $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ , Typical values are at  $T_A = 25^{\circ}\text{C}$  (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
V <sub>MICIO</sub>	Analog signal range			0	V <sub>BAT</sub>		V
r <sub>ON</sub>	ON-state resistance	MIC, VBUS	V <sub>I</sub> = 2.3 V, I <sub>O</sub> = −20 mA, V <sub>BAT</sub> = 3.0 V	40	52		Ω
		MIC, DP	V <sub>I</sub> = 2.3 V, I <sub>I</sub> = −5 mA, V <sub>BAT</sub> = 3.0 V	15	25		Ω
I <sub>IO(OFF)</sub>	V <sub>I</sub> or V <sub>O</sub> OFF leakage current		V <sub>I</sub> = 0.3 V, V <sub>O</sub> = 2.3 V or (V <sub>I</sub> = 2.3 V, V <sub>O</sub> = 0.3 V), V <sub>BAT</sub> = 4.4 V, Switch OFF	5	500		nA
DYNAMIC							
t <sub>ON</sub>	Turn-ON time	From receipt of I <sup>2</sup> C ACK bit	V <sub>I</sub> or V <sub>O</sub> = V <sub>BAT</sub> , R <sub>L</sub> = 100 Ω, C <sub>L</sub> = 35 pF	260			μs
t <sub>OFF</sub>	Turn-OFF time			180			
C <sub>I(OFF)</sub>	VI OFF capacitance		DC bias = 0 V or 3.6 V, f = 10 MHz, Switch OFF	130			pF
C <sub>O(OFF)</sub>	VO OFF capacitance			10.5			
C <sub>I(ON)</sub> , C <sub>O(ON)</sub>	VI, VO ON capacitance		DC bias = 0 V or 3.6 V f = 10 MHz, Switch ON	140			pF
BW	Bandwidth, MIC to VBUS		R <sub>L</sub> = 50 Ω, Switch ON	40			MHz
	Bandwidth, MIC to DP		R <sub>L</sub> = 50 Ω, Switch ON	250			
O <sub>ISO</sub>	OFF Isolation		f = 20 kHz, R <sub>L</sub> = 50 Ω, Switch OFF	−95			dB
X <sub>TALK</sub>	Crosstalk		f = 20 kHz, R <sub>L</sub> = 50 Ω, to audio output	−85			dB
THD	Total harmonic distortion		R <sub>L</sub> = 600 Ω, C <sub>L</sub> = 20 pF, f = 20 Hz–20 kHz , V <sub>in</sub> = 0.1 V <sub>pp</sub> centered at V <sub>BAT</sub> /2	0.05	0.65		%

(1)  $V_I$  is equal to the asserted voltage on VBUS/DP pin.  $V_O$  is equal to the asserted voltage on MIC pin.  $I_I$  is equal to the current on the VBUS/DP pin.  $I_O$  is equal to the current on the MIC pin.

# TSU6721YFF

SCDS345 –JUNE 2013

[www.ti.com](http://www.ti.com)

## USB & UART SWITCH ELECTRICAL CHARACTERISTICS

 $V_{BAT} = 3\text{ V to }4.4\text{ V}$ ,  $V_{DDIO} = 2.8\text{ V}$ ,  $T_A = -40^{\circ}\text{C to }85^{\circ}\text{C}$ , Typical values are at  $T_A = 25^{\circ}\text{C}$  (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>ANALOG SWITCH</b>							
$V_{USBIO}$	Analog signal range			0		3.6	V
$V_{UARTIO}$	Analog signal range			0		2.7	
$r_{ON}$	ON-state resistance	DM_HT,DM DP_HT,DP	$V_I = 0\text{ V to }3.6\text{ V}$ , $I_O = -20\text{ mA}$ , $V_{BAT} = 3.0\text{ V}$		6	11	$\Omega$
		TxD, DM RxD, DP	$V_I = 0\text{ V to }3.6\text{ V}$ , $I_O = -20\text{ mA}$ , $V_{BAT} = 3.0\text{ V}$		7	14.3	
$r_{ON}$	ON-state resistance	ID, IDBP	$V_I = 0\text{ V to }3.6\text{ V}$ , $I_O = -20\text{ mA}$ , $V_{BAT} = 3.0\text{ V}$		30		$\Omega$
$\Delta r_{ON}$	ON-state resistance match between channels	DM_HT,DM DP_HT,DP	$V_I = 0.4\text{ V}$ , $I_O = -20\text{ mA}$ , $V_{BAT} = 3.0\text{ V}$		0.2	1	$\Omega$
		TxD, DM RxD, DP	$V_I = 0.4\text{ V}$ , $I_O = -20\text{ mA}$ , $V_{BAT} = 3.0\text{ V}$		1.5	3	
$r_{ON(flat)}$	ON-state resistance flatness	DM_HT, DP_HT, TxD, RxD, DM, DP	$V_I = 0\text{ V to }3.6\text{ V}$ , $I_O = -20\text{ mA}$ , $V_{BAT} = 3.0\text{ V}$		1.4	3.2	$\Omega$
$I_{IO(OFF)}$	VI or VO OFF leakage current	DM_HT, DP_HT, TxD, RxD, DM, DP	$V_I = 0.3\text{ V}$ , $V_O = 2.7\text{ V}$ or $V_I = 2.7\text{ V}$ , $V_O = 0.3\text{ V}$ , $V_{BAT} = 4.4\text{ V}$ , Switch OFF		45	200	nA
$I_{IO(ON)}$	VO ON leakage current	DM_HT, DP_HT, TxD, RxD, DM, DP	$V_I = \text{OPEN}$ , $V_O = 0.3\text{ V}$ or $2.7\text{ V}$ , $V_{BAT} = 4.4\text{ V}$ , Switch ON		50	200	nA
<b>DYNAMIC</b>							
$t_{ON}$	Turn-ON time	From receipt of $I^2C$ ACK bit	$V_I$ or $V_O = V_{BAT}$ , $R_L = 100\ \Omega$ , $C_L = 35\text{ pF}$	130			$\mu\text{s}$
$t_{OFF}$	Turn-OFF time			100			
$C_{I(OFF)}$	VI OFF capacitance		DC bias = $0\text{ V}$ or $1.6\text{ V}$ , $f = 10\text{ MHz}$ , Switch OFF	4			pF
$C_{O(OFF)}$	VO OFF capacitance			7			pF
$C_{I(ON)}, C_{O(ON)}$	VI, VO ON capacitance		DC bias = $0\text{ V}$ or $3.6\text{ V}$ $f = 10\text{ MHz}$ , Switch ON	9			pF
BW	Bandwidth		$R_L = 50\ \Omega$ , Switch ON	510			MHz
$O_{ISO}$	OFF Isolation		$f = 240\text{ kHz}$ , $R_L = 50\ \Omega$ , Switch OFF	-26			dB
$X_{TALK}$	Crosstalk		$f = 240\text{ kHz}$ , $R_L = 50\ \Omega$	-32			dB

## GENERAL OPERATION

The TSU6721 is a multimedia switch that connects a common USB connector to USB, UART or audio signals. The device also has a MIC switch that connects to either VBUS or DP. It has an integrated load switch to support charging. The load switch has OverVoltage Protection as well as OverCurrent Limiting Protection. In addition, the TSU6721 also has an ID bypass switch to transmit ID signal from the connector to the host. It has an internal FET switch that disconnects the coupling capacitor connected to the VBUS line.

### Standby Mode

Standby mode is the default mode upon power up and occurs when no accessory has been detected. During this mode, the VBUS and ID lines are continually monitored through comparators to determine when an accessory is inserted. Power consumption is minimal during standby mode.

### Load Switch

The integrated load switch provides both overvoltage/undervoltage and overcurrent limiting protection:

#### Overvoltage Protection

When the input voltage rises above VOVP, the internal load switch is turned off. The response is very rapid, with the FET turning off in less than 1 $\mu$ s tOFF(OVP). The OVP\_EN interrupt bit is set high when an overvoltage condition is detected. When the input voltage returns below VOVP-VHYS\_OVP and remains above VUVLO, the VBUS switch is turned on again after a deglitch time of tON(OVP). This deglitch time ensures that the input supply has stabilized before turning the switch on. When the OVP condition is cleared, the OVP\_OCP\_DIS interrupt bit is set high.

#### Undervoltage Protection

When VBUS is not present and VBAT is less than 2.5V, VBAT and VBUS voltages are below the undervoltage threshold and TSU6721 is powered off.

#### Overcurrent Limiting Protection

The TSU6721 also provides overcurrent limiting protection. When current increases beyond the I<sub>OCP</sub> threshold, a time-out delay is initiated. After the delay has expired, and the current is still greater than I<sub>OCP</sub>, then load switch is disabled. The maximum current that flows through the load switch is controlled by the I<sub>OCL</sub> limit. This feature provides control on the VBUS charging current and minimizes the chance of internal circuitry damage caused by overcurrent event. The overcurrent level can be programmed through I2C.

### Power Supervisor

TSU6721 uses VBAT as the primary supply voltage. VBUS is the secondary supply. VDDIO is used for I2C communication.

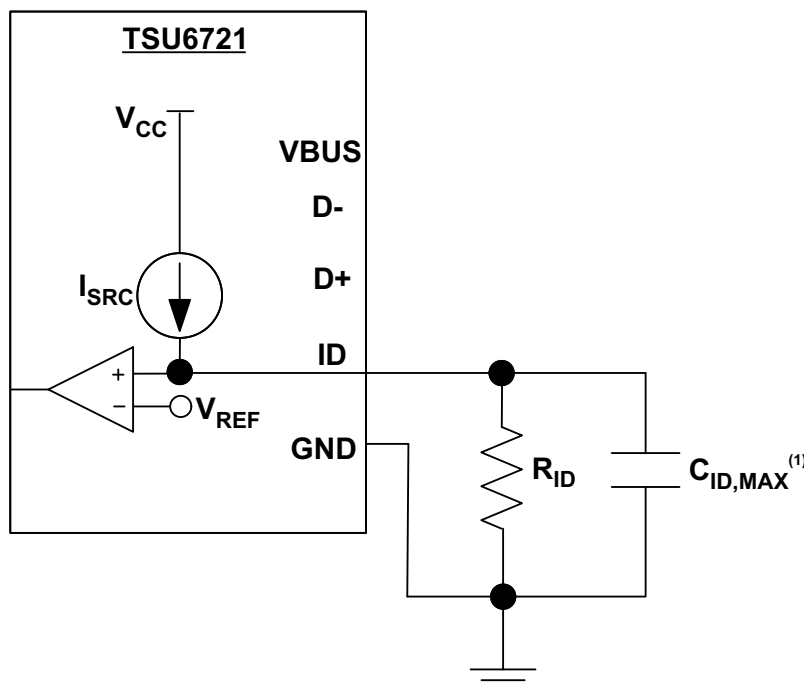
**Table 1. Supply Voltage States**

VBAT	VBUS	VDDIO	DETECTION	LOAD SWITCH	I2C	COMMENTS
Yes	No	No	Enabled	Not Enabled	Not Enabled	VBAT is supply
Yes	Yes	No	Enabled	Enabled	Not enabled	VBAT is supply. LOAD SWITCH controlled by VBUS
Yes	No	Yes	Enabled	Not Enabled	Enabled	VBAT is supply
Yes	Yes	Yes	Enabled	Enabled	Enabled	VBAT is supply. LOAD SWITCH controlled by VBUS
No	Yes	No	Enabled	Enabled	Not Enabled	VBUS is supply. LOAD SWITCH controlled by VBUS
No	Yes	Yes	Not valid			
No	No	Yes	Not valid			
No	No	No	Power Down Reset			

## ACCESSORY ID DETECTION

If VBUS is high and the attachment is a non-compliant charger (see [Table 5](#)), the impedance on the ID pin is then determined. If VBUS is low and an accessory is attached, then an ADC for impedance sensing is used on the ID pin to identify which accessory is attached and/or what kind of remote control key button is pushed.

The TSU6721 features impedance detection for identification of various accessories that might be attached to the micro-USB port. Each accessory is identified by a unique resistor value connected between the ID pin and Ground. During impedance detection a current source is applied to the ID pin. The current source is then applied to the ID pin while an internal voltage reference is incremented till it matches the ID pin voltage. This produces a 5-bit ADC value that corresponds to the ID resistance found. Once an ID resistance is identified, a current source is continuously applied to determine when the resistance is detached.



(1) Maximum ID\_Cap capacitance as noted in [RECOMMENDED OPERATING CONDITIONS](#)

**Figure 1. Impedance Detection Circuitry**

### Impedance Buckets for Each Accessory and Remote Control Key Button

In order to implement ID detection, each accessory and remote control key button of audio accessory should contain below ID impedance resistor value which is 1% tolerance accuracy.

### Switch Matrix

MCPC accessory table is selected only when MCPC mode is enabled in Control Reg02h. VBUS to OUT Load Switch is enabled anytime VBUS is applied to the USB connector.

**Table 2. Accessory ID and Switch States**

ACCESSORY	ID	Res (%)	ADC Value	SWITCH STATE					STATUS OUTPUT		
				DP/DM			VBUS	ID	ISET	JIG	BOOT
				USB	UART	Audio	MIC	ID_HT			
OTG	0	–	00000	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF
Video	75	5%	00000	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF
MHL	1K	5%	00000	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
Send_End Button	2K	10%	00001	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF
Stereo Headset RC S1 Button	2.604K	5%	00010	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF
Stereo Headset RC S2 Button	3.208K	5%	00011	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF
Stereo Headset RC S3 Button	4.014K	5%	00100	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF
Stereo Headset RC S4 Button	4.82K	5%	00101	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF
Stereo Headset RC S5 Button	6.03K	5%	00110	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF
Stereo Headset RC S6 Button	8.03K	5%	00111	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF
Stereo Headset RC S7 Button	10.03K	5%	01000	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF
Stereo Headset RC S8 Button	12.03K	5%	01001	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF
Stereo Headset RC S9 Button	14.46K	5%	01010	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF
Stereo Headset RC S10 Button	17.26K	5%	01011	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF
Stereo Headset RC S11 Button	20.5K	5%	01100	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF
Stereo Headset RC S12 Button	24.07K	5%	01101	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF
Audio Device Type 3	28.7K	5%	01110	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF
Reserved Accessory #1	34K	5%	01111	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF
Reserved Accessory #2	40.2K	5%	10000	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF
Reserved Accessory #3	49.9K	5%	10001	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF
Reserved Accessory #4	64.9K	5%	10010	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF
Audio Device Type 2	80.27K	5%	10011	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF
Phone Powered Device	102K	5%	10100	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF
TTY Converter	121K	5%	10101	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF
UART Cable	150K	5%	10110	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF
Type 1 Charger	200K	5%	10111	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF
Factory Mode - Boot Off USB	255K	5%	11000	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF
Factory Mode - Boot On USB	301K	5%	11001	ON	OFF	OFF	OFF	OFF	OFF	ON	ON
Audio/Video Cable	365K	5%	11010	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF
A/V + VBUS	365K	5%	11010	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF
Type 2 Charger	442K	5%	11011	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF
Factory Mode - Boot Off UART	523K	5%	11100	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF
Factory Mode - Boot On UART	619K	5%	11101	OFF	ON	OFF	OFF	OFF	OFF	ON	ON
Stereo Audio Device Type 1	1000.07K	10%	11110	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF
Mono Audio Device Type 1	1002K	10%	11110	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF

**Table 3. Accessory ID and Switch States MCPC Mode**

ACCESSORY	ID	RES (%)	ADC VALUE	SWITCH STATE					STATUS OUTPUT		
				DP/DM			VBUS	ID	ISET	JIG	BOOT
				USB	UART	AUDIO	MIC	ID_HT			
Send_End_SW	47K	5%	10000	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF
			10001					OFF	OFF	OFF	
Send_End_SW with VBUS	47K	5%	10000	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF
			10001					OFF	OFF	OFF	
Maintenance	180K	5%	10110	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
			10111					OFF	OFF	OFF	
Mode 1 Stereo	47K + 240K	5%	11000	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF
			11001								
Mode 1 Stereo with VBUS	47K + 240K	5%	11000	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF
			11001								
Reserved	390K	5%	11010	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
			11011								
Mode 3 Monaural	47K + 510K	5%	11100	DM to S_L; DP to MIC			OFF	OFF	OFF	OFF	OFF
			11101								
Mode 3 Monaural with VBUS	47K + 510K	5%	11100	DM to S_L; DP to MIC			OFF	OFF	OFF	OFF	OFF
			11101								
Mode 2 Monaural	47K + 750K	5%	11110	DM to S_L; DP OPEN			ON	OFF	OFF	OFF	OFF
Mode 2 Monaural with VBUS	47K + 750K	5%	11110	DM to S_L; DP OPEN			OFF	OFF	OFF	OFF	OFF

## CHARGER DETECTION

**Table 4. Chargers Detected and Switch States**

ACCESSORY	ID	RES (%)	ADC VALUE	SWITCH STATE					STATUS OUTPUT		
				DP/DM			VBUS	ID	ISET	JIG	BOOT
				USB	UART	AUDIO					
No ID	–	–	11111	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
Apple Charger	–	–	11111	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
Non-standard Charger	–	–	11111	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
USB Standard Downstream Port	–	–	11111	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF
USB Charging Downstream Port	–	–	11111	ON	OFF	OFF	OFF	ON	ON	OFF	OFF
Dedicated Charging Port	–	–	11111	ON	OFF	OFF	OFF	ON	ON	OFF	OFF

Table 5 lists the configurations of the DP\_CON (D+) and DM\_CON (D-) that are internal to the various device types.

**Table 5. Charger Detection Table**

DEVICE TYPE	VBUS	DP_CON (D+)	DM_CON (D-)
Standard Downstream Port	>4 V	Pull-down R 15k to GND	Pull-down R 15k
Charging Downstream Port	>4 V	Pull-down R 15k to GND	$V_{DM\_SRC} = 0.6V$
Dedicated Charging Port	>4 V	Short to D–	Short to D+
Apple Charger	>4 V	$2.0 < V_{DP} < 2.8$	$2.0 < V_{DM} < 2.8$
U200	>4 V	$V_{DP} = 1.34$	$V_{DM} = 1.34$
Non-compliant USB Charger Any Device	>4 V	Open	Open

### Power-On Reset

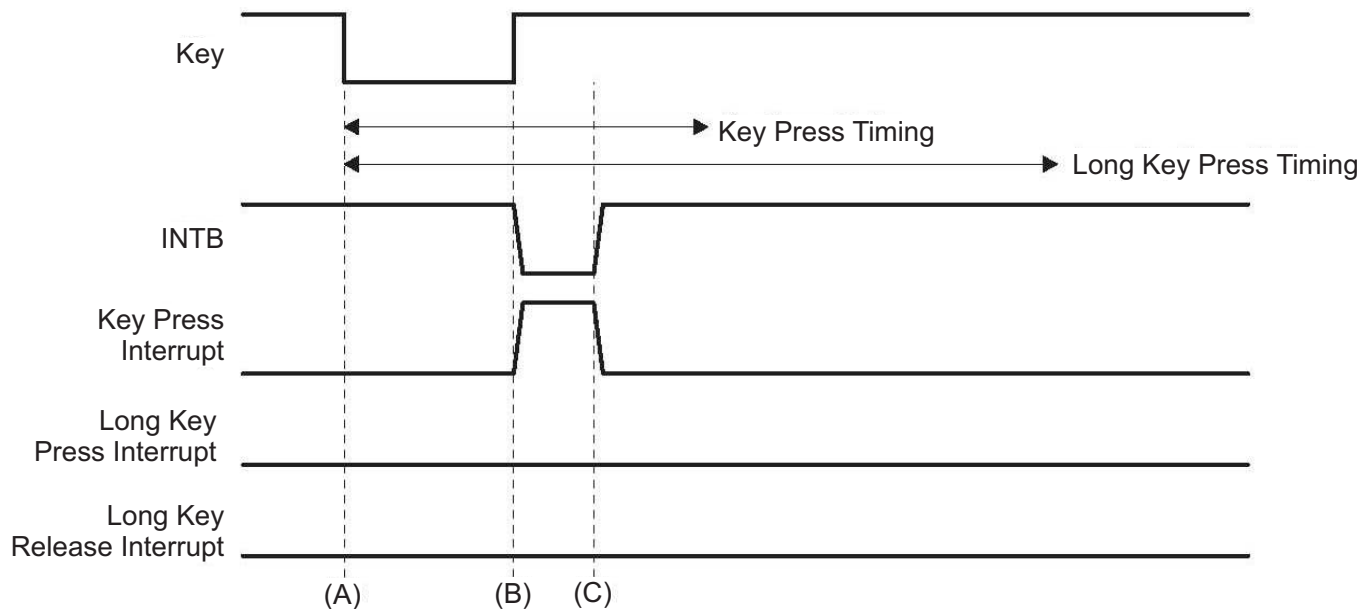
When power (from 0 V) is applied to  $V_{BAT}$ , an internal power-on reset holds the TSU6721 in a reset condition until  $V_{BAT}$  has reached  $V_{POR}$ . At that point, the reset condition is released, and the TSU6721 registers and I<sup>2</sup>C state machine initialize to their default states.

After the initial power-up phase,  $V_{BAT}$  must be lowered to below 0.2 V and then back up to the operating voltage ( $V_{DDIO}$ ) for a power-reset cycle.

### Software Reset

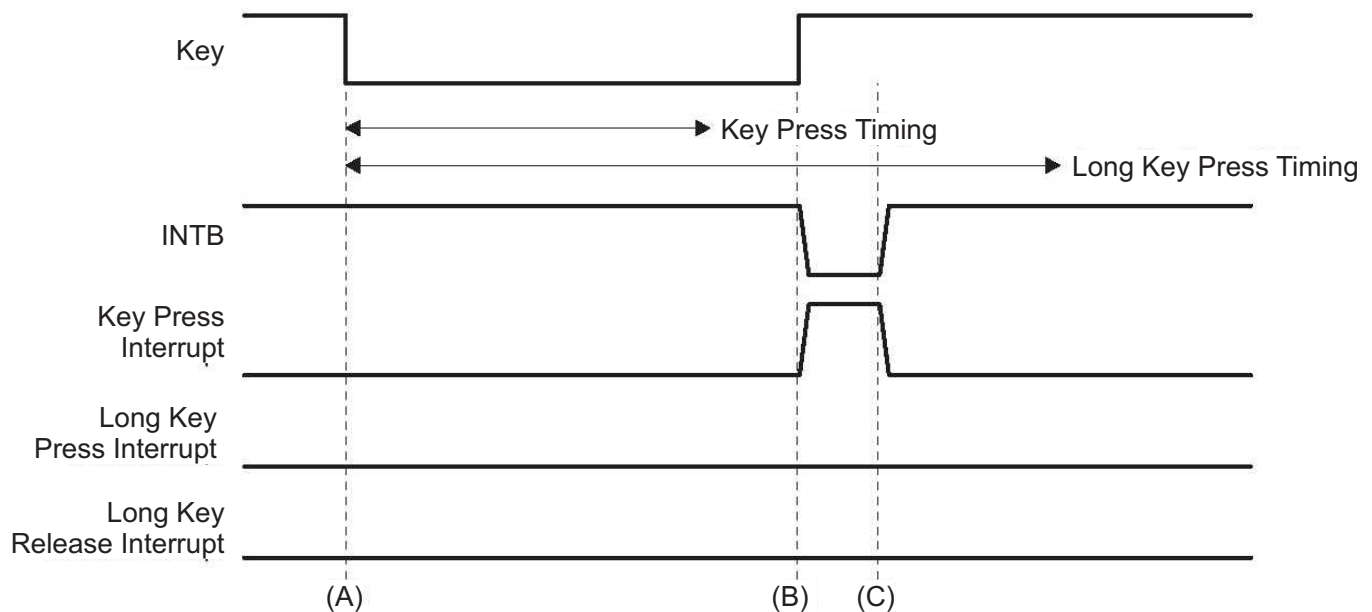
The TSU6721 has software a reset feature. Set the reset bit in the I2C register high to reset TSU6721. After resetting, INTB will keep low until INT\_Mask bit of Control register (0x02) is cleared.

## Key Press Identification



- Key press
- Released key press → Set KP Interrupt → Set error bit in Button register → INTB pulled low
- I<sup>2</sup>C read of INT register → Clear KP interrupt → INTB goes back high

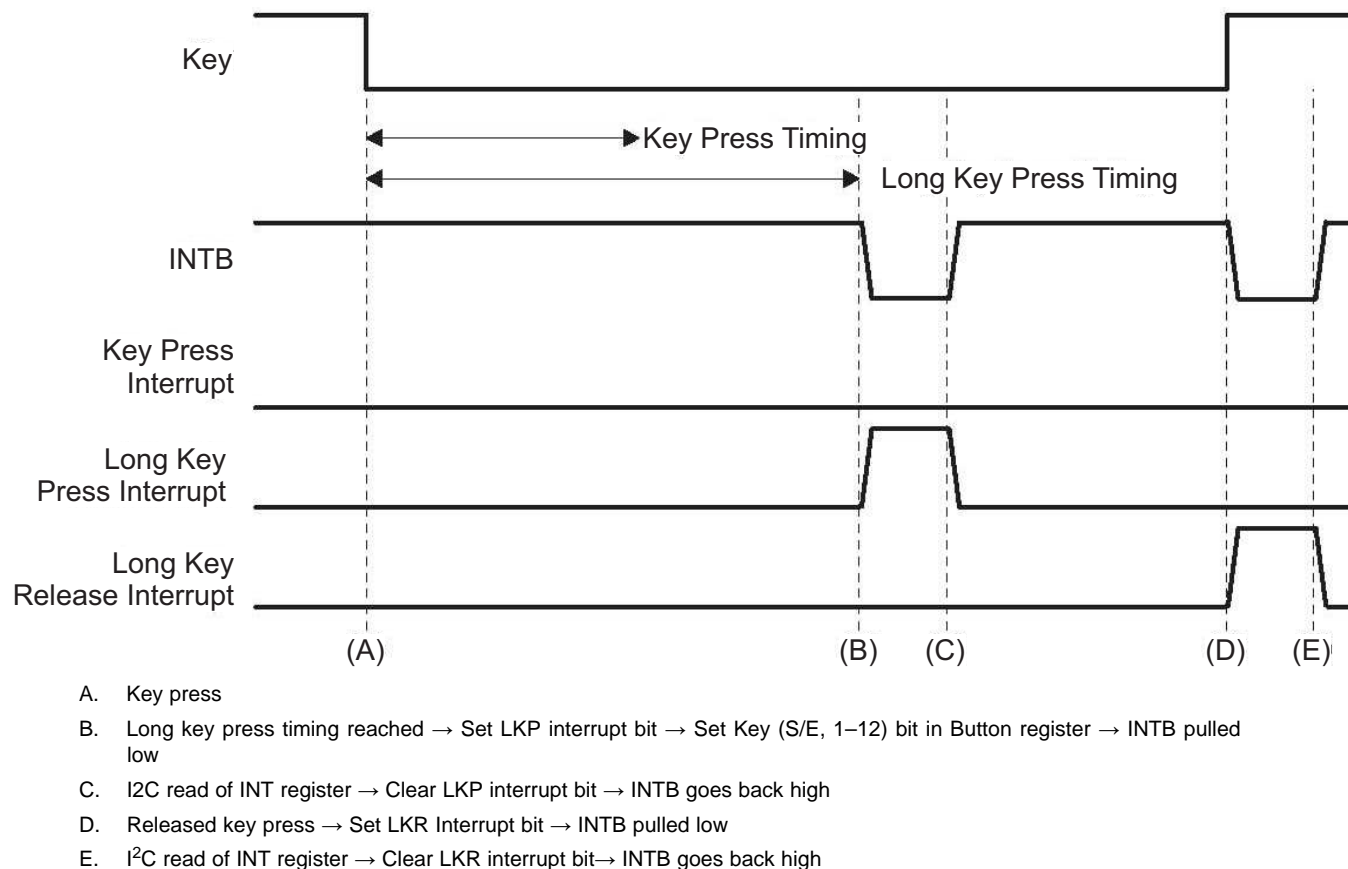
**Figure 2. Short Key Press**



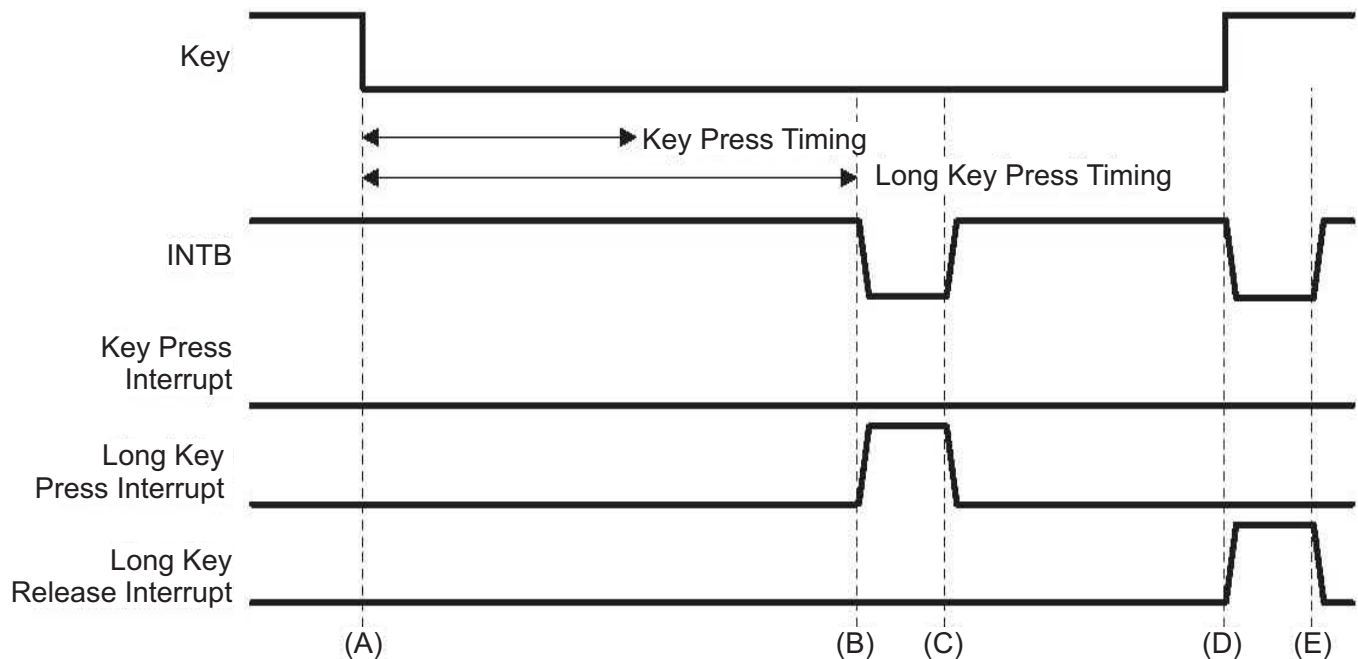
- Key press
- Released key press → Set KP Interrupt → Set Key (S/E, 1–12) bit in Button register → INTB pulled low .
- I<sup>2</sup>C read of INT register → Clear KP interrupt → INTB goes back high.

**Figure 3. Normal Key Press**



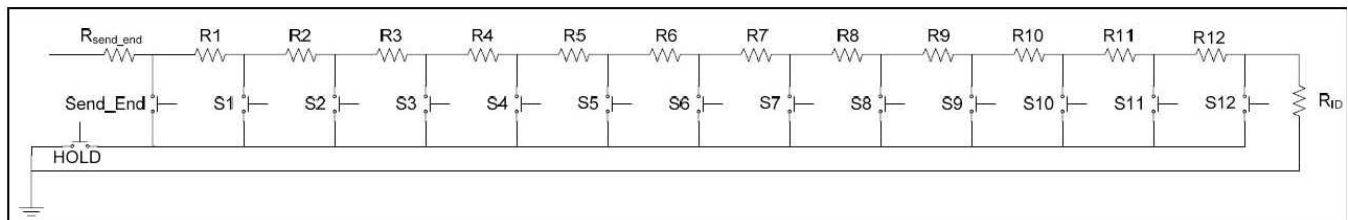


**Figure 4. Long Key Press**



- A. Key press detected when accessory attached
- B. Long key press timing reached → Set SK interrupt bit → Set Key (S/E, 1–12) bit in Button register → INTB pulled low
- C. I<sup>2</sup>C read of INT register → Clear SK interrupt bit → INTB goes back high
- D. Released key press detected when accessory ID resistor is 1 MΩ → Set SKR Interrupt bit → INTB pulled low
- E. I<sup>2</sup>C read of INT register → Clear SKR interrupt bit → INTB goes back high

**Figure 5. Stuck Key Press**

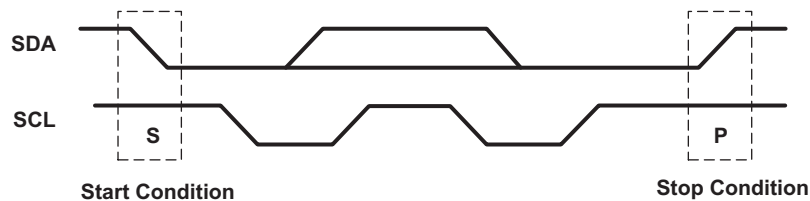


**Figure 6. Audio/Remote Controller Accessory**

## STANDARD I<sup>2</sup>C INTERFACE DETAILS

The bidirectional I<sup>2</sup>C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

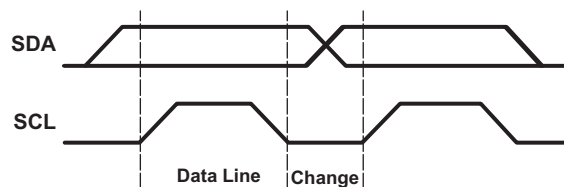
I<sup>2</sup>C communication with this device is initiated by the master sending a START condition, a high-to-low transition on the SDA input/output while the SCL input is high (see [Figure 7](#)). After the start condition, the device address byte is sent, MSB first, including the data direction bit (R/W). This device does not respond to the general call address. After receiving the valid address byte, this device responds with an ACK, a low on the SDA input/output during the high of the ACK-related clock pulse.



**Figure 7. Definition of Start and Stop Conditions**

The data byte follows the address ACK. The R/W bit is kept low for transfer from the master to the slave. The data byte is followed by an ACK sent from this device. Data are output only if complete bytes are received and acknowledged. The output data is valid at time (tpv) after the low-to-high transition of SCL, during the clock cycle for the ACK.

On the I<sup>2</sup>C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (START or STOP) (see Figure 8).

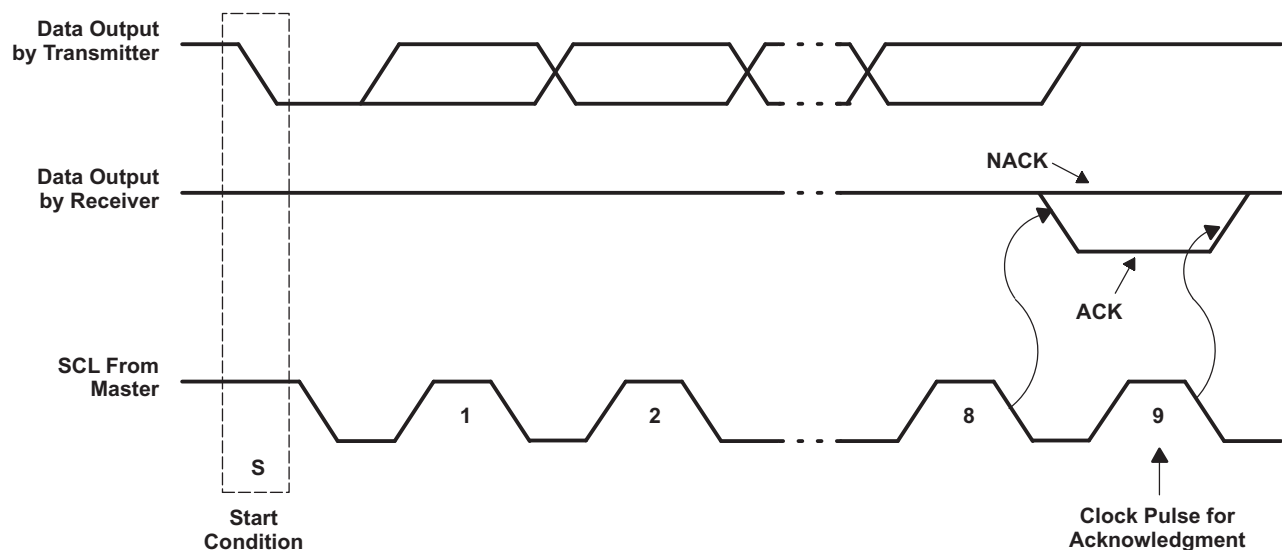


**Figure 8. Bit Transfer**

A Stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master (see Figure 7).

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit.

A slave receiver that is addressed must generate an ACK after the reception of each byte. The device that acknowledges has to pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period (see Figure 9). Setup and hold times must be taken into account.



**Figure 9. Acknowledgment on I<sup>2</sup>C Bus**

# TSU6721YFF

SCDS345 –JUNE 2013

www.ti.com

## Writes

Data is transmitted to the TSU6721 by sending the device slave address and setting the LSB to a logic 0 (see Figure 10 for device address). The command byte is sent after the address and determines which register receives the data that follows the command byte. The next byte is written to the specified register on the rising edge of the ACK clock pulse.

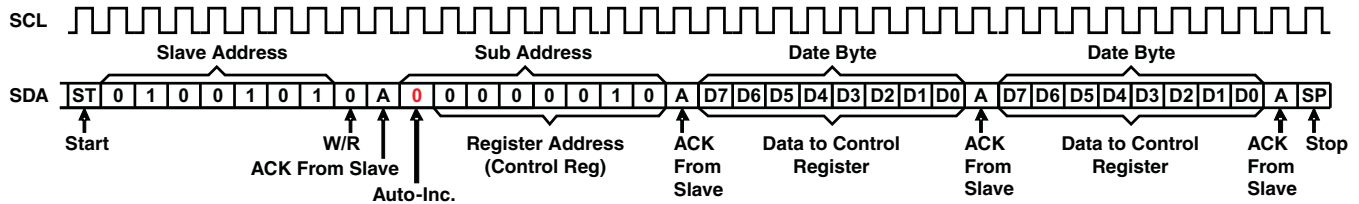


Figure 10. Repeated Data Write to a Single Register

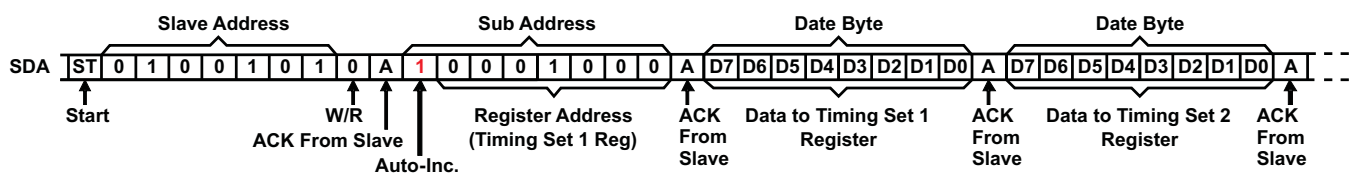


Figure 11. Burst Data Write to Multiple Registers

## Reads

The bus master first must send the TSU6721 slave address with the LSB set to logic 0. The command byte is sent after the address and determines which register is accessed. After a restart, the device slave address is sent again but, this time, the LSB is set to logic 1. Data from the register defined by the command byte then is sent by the TSU6721. Data is clocked into the SDA output shift register on the rising edge of the ACK clock pulse. See Figure 12.

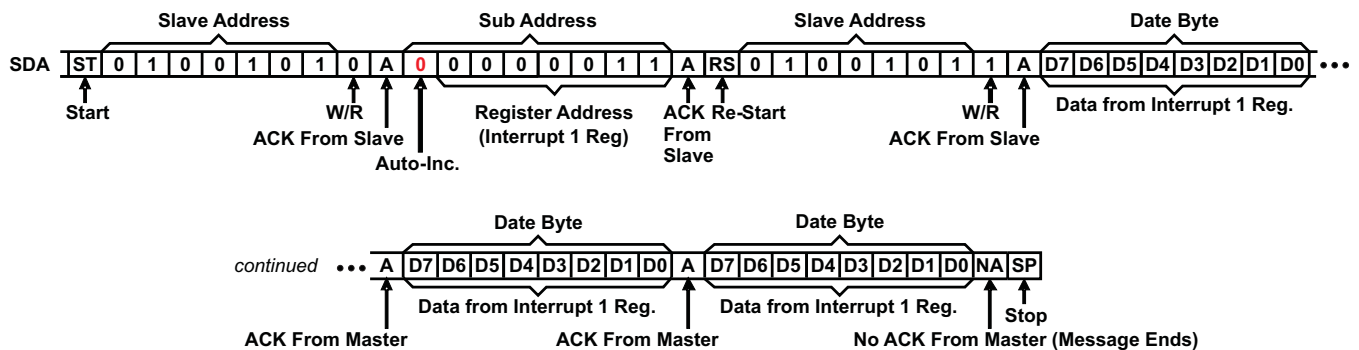


Figure 12. Repeated Data Read from a Single Register – Combined Mode

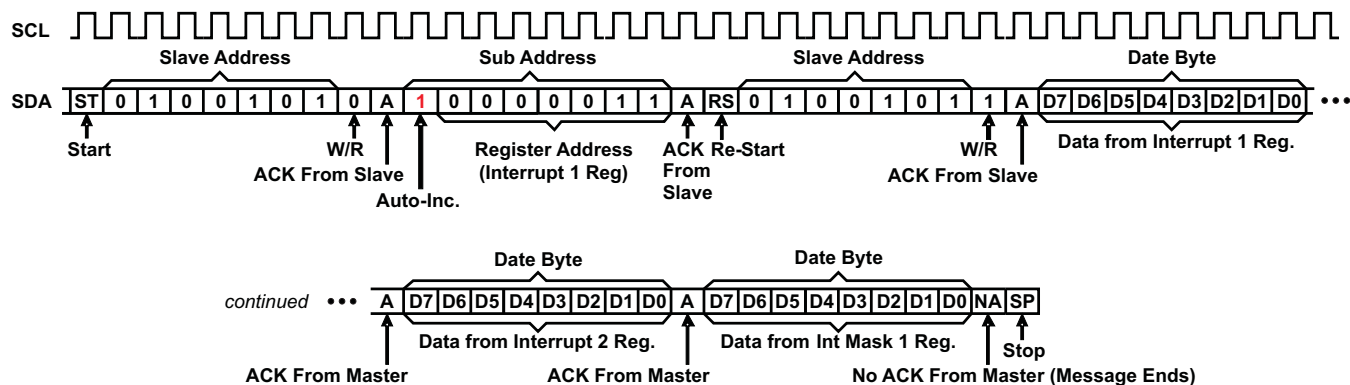


Figure 13. Burst Data Read from Multiple Registers – Combined Mode

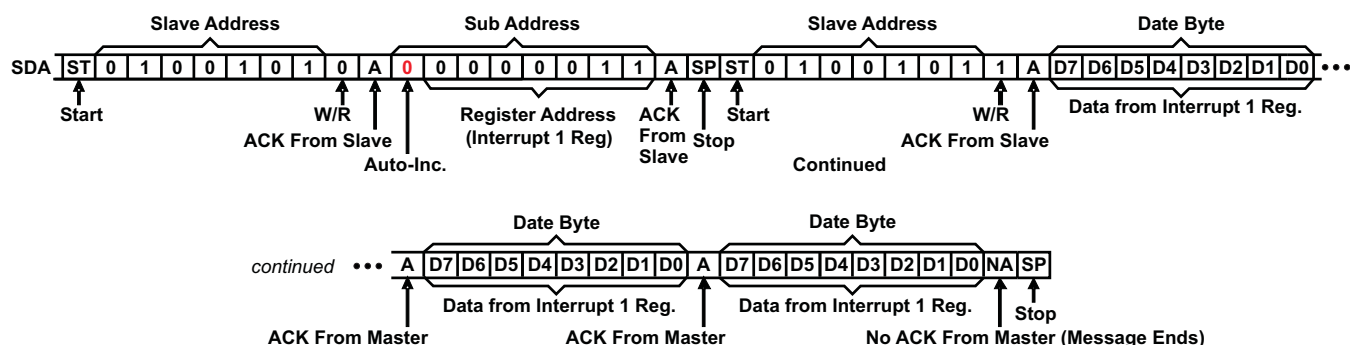


Figure 14. Repeated Data Read from a Single Register – Split Mode

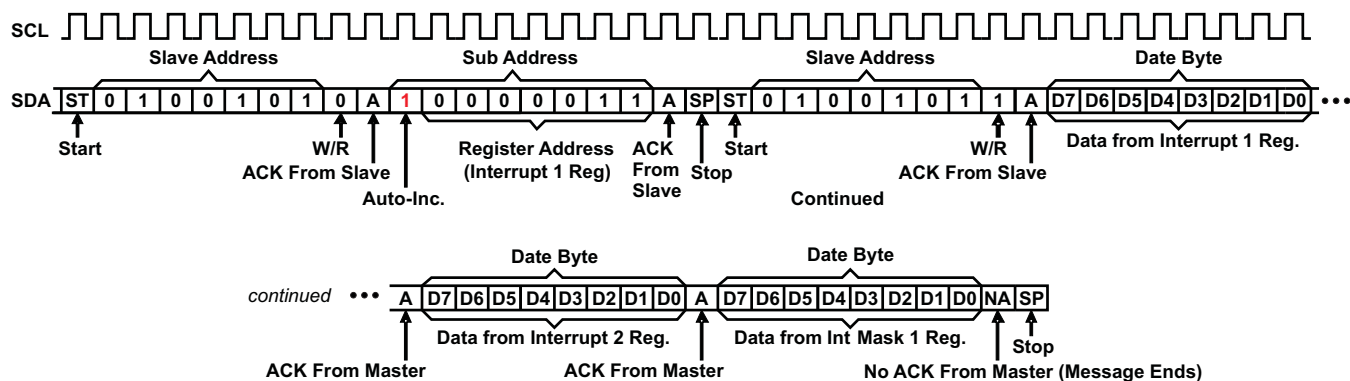


Figure 15. Burst Data Read from Multiple Registers – Split Mode

**Notes (Applicable to Figure 10 – Figure 15):**

- SDA is pulled low on Ack. from slave or Ack. from master.
- Register writes always require sub-address write before first data byte.
- Repeated data writes to a single register continue indefinitely until Stop or Re-Start.
- Repeated data reads from a single register continue indefinitely until No Ack. from master.
- Burst data writes start at the specified register address, then advance to the next register address, even to the read-only registers. For these registers, data write appears to occur, though no data are changed by the writes. After register 14h is written, writing resumes to register 01h and continues until Stop or Re-Start.
- Burst data reads start at the specified register address, then advance to the next register address. Once register 14h is read, reading resumes from register 01h and continues until No Ack. from master.

# TSU6721YFF

SCDS345 –JUNE 2013

[www.ti.com](http://www.ti.com)

## I<sup>2</sup>C REGISTER MAP

ADDRESS	REGISTER	TYPE	RESET VALUE	BIT 7	BIT 6	BIT 5	BIT4	BIT 3	BIT 2	BIT1	BIT0
01h	Device ID	R	00010010	Version ID					Vendor ID		
02h	Control	R/W	xx011111			MCPC Mode	Switch Open	Raw Data	Manual S/W	Wait	INT Mask
03h	Interrupt 1	R	00000000	OVP_OCP_OTP_DIS	OCP_EN	OVP_EN	LKR	LKP	KP	Detach	Attach
04h	Interrupt 2	R	00000000	VBUS	OTP_EN	CONNECT	Stuck_Key_RCV	Stuck_Key	ADC_Change	Reserved_Attach	A/V_Change
05h	Interrupt Mask 1	R/W	00000000	OVP_OCP_OTP_DIS	OCP_EN	OVP_EN	LKR	LKP	KP	Detach	Attach
06h	Interrupt Mask 2	R/W	00000000	VBUS	OTP_EN	CONNECT	Stuck_Key_RCV	Stuck_Key	ADC_Change	Reserved_Attach	A/V_Change
07h	ADC	R	xxx11111				ADC Value				
08h	Timing Set 1	R/W	00000000	Key Press				Device Sleep			
09h	Timing Set 2	R/W	00000000	Switching Wait				Long Key Press			
0Ah	Device Type 1	R	00000000	USB OTG	DCP	CDP	Type1/Type 2 Charger	UART	USB	Audio Type2	Audio Type1
0Bh	Device Type 2	R	00000000	Audio Type3	A/V	TTY	PPD	JIG_UART_OFF	JIG_UART_ON	JIG_USB_OFF	JIG_USB_ON
0Ch	Button 1	R	00000000	7	6	5	4	3	2	1	Send_End
0Dh	Button 2	R	x0000000		Unknown	Error	12	11	10	9	8
13h	Manual S/W 1	R/W	00000000	DM Switching			DP Switching			VBUS Switching	
14h	Manual S/W 2	R/W	xxx00000				ISET	BOOT	JIG	ID Switching	
15h	Device Type 3	R	0000x000	Video	U200 Chg	Apple Chg	A/V VBUS		VBUS non-standard	VBUS Debounce	MHL
1Bh	Reset	W	xxxxxxx0								Reset
20h	Timer Setting	R/W	00010101	ISET Enable Time	Load Switch Enable Time	BCDv1.2 Timer			ADC Start Time		
21h	OCL/OCP Setting 1	R/W	001010x1	OCL Protection Level Setting			OCP Timeout Delay Setting				BCDv1.2 Enable
22h	OCL/OCP Setting 2	R/W	xxx11001				OC Enable		OCP Protection Level Setting		
23h	Device Type 4	R/W	xxxxx111						MCPC ID Resistor Value		

### Notes:

- Do not use blank register bits.
- Write "0" to the blank register bits.
- Values read from the blank register bits are not defined and invalid.
- When reading I2C table after an interrupt first read register Interrupt 1 (03h) followed by Interrupt 2 (04h).
- Interrupt 1 (03h) and Interrupt 2 (04h) should not be read when INT Mask = 0.
- I2C should not be accessed within 5 ms of device power-up.

### Slave Address

NAME	SIZE (BITS)	DESCRIPTION							
		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Slave address	8	0	1	0	0	1	0	1	R/W

**Device ID**

Address: 01h

Reset Value: 00010010

Type: Read

BIT NO.	NAME	SIZE (BITS)	DESCRIPTION
2-0	Vendor ID	3	A unique number for vendor 010b for Texas Instruments
7-3	Version ID	5	A unique number for chip version 00010b for TSU6721

**Control**

Address: 02h

Reset Value: xx011111

Type: Read/Write

BIT NO.	NAME	SIZE (BITS)	DESCRIPTION
0	INT Mask	1	0: Unmask interrupt 1: Mask interrupt
1	Wait	1	0: Wait until host re-sets this bit(WAIT bit) high 1: Wait until Switching timer is expired defined in Timing Set 2
2	Manual S/W	1	0: Manual Switching 1: Automatic Switching
3	RAW Data	1	0: Report the status changes on ID to Host 1: Don't report the status changes on ID
4	Switch Open	1	0: Open all Switches (Including load switch) 1: Automatic Switching by accessory status
5	MCPC Mode	1	0: Non-MCPC Mode 1: MCPC Mode
7-6	Unused	2	

# TSU6721YFF

SCDS345 –JUNE 2013

[www.ti.com](http://www.ti.com)

## Interrupt 1

Address: 03h

Reset Value: 00000000

Type: Read and Clear

BITS	NAME	SIZE (BITS)	DESCRIPTION
0	Attach	1	1: Accessory is attached
1	Detach	1	1: Accessory is detached
2	KP	1	1: Key press
3	LKP	1	1: Long key press
4	LKR	1	1: Long key release
5	OVP_EN	1	1: OVP enabled
6	OCP_EN	1	1: OCP enabled
7	OVP_OCP_OTP_DISABLE	1	1: OVP_OCP_OTP disabled (device is out of OVP, OCP or OTP)

## Interrupt 2

Address: 04h

Reset Value: 00000000

Type: Read and Clear

BITS	NAME	SIZE (BITS)	DESCRIPTION
0	A/V_Change	1	1: Accessory Change is detected when A/V cable is attached
1	Reserved_Attach	1	1: Reserved Device is attached
2	ADC_Change	1	1: ADC value is changed when RAW data is enabled
3	Stuck_Key	1	1: Stuck Key is detected
4	Stuck_Key_RCV	1	1: Stuck Key is recovered
5	Connect	1	1: Switch is connected (closed)
6	OTP_EN	1	1: Over Temperature Protection enabled
7	VBUS	1	1: VBUS detected



### Interrupt Mask 1

Address: 05h

Reset Value: 00000000

Type: Read/Write

BIT NO.	NAME	SIZE (BITS)	DESCRIPTION
0	Attach	1	0: Unmask Attach Interrupt 1: Mask Attach Interrupt
1	Detach	1	0: Unmask Key press Interrupt 1: Mask Detach Interrupt
2	KP	1	0: Unmask Key press Interrupt 1: Mask Key press Interrupt
3	LKP	1	0: Unmask Long key press Interrupt 1: Mask Long key press Interrupt
4	LKR	1	0: Unmask Long key release Interrupt 1: Mask Long key release Interrupt
5	OVP_EN	1	0: Unmask OVP_EN Interrupt 1: Mask OVP_EN Interrupt
6	OCP_EN	1	0: Unmask OCP_EN Interrupt 1: Mask OCP_EN Interrupt
7	OVP_OCP_OTP_DIS	1	0: Unmask OVP_OCP_OTP_DIS Interrupt 1: Mask OVP_OCP_OTP_DIS Interrupt

### Interrupt Mask 2

Address: 06h

Reset Value: 00000000

Type: Read/Write

BIT NO.	NAME	SIZE (BITS)	DESCRIPTION
0	A/V_Change	1	0: Unmask A/V_Change Interrupt 1: Mask A/V_Change Interrupt
1	Reserved_Attach	1	0: Unmask Reserved_Attach Interrupt 1: Mask Reserved_Attach Interrupt
2	ADC_Change	1	0: Unmask ADC_Change Interrupt 1: Mask ADC_Change Interrupt
3	Stuck_Key	1	0: Unmask Stuck_Key Interrupt 1: Mask Stuck_Key Interrupt
4	Stuck_Key_RCV	1	0: Unmask Stuck_Key_RCV Interrupt 1: Mask Stuck_Key_RCV Interrupt
5	Connect	1	0: Unmask Connect Interrupt 1: Mask Connect Interrupt
6	OTP_EN	1	0: Unmask OTP_EN Interrupt 1: Mask OTP_EN Interrupt
7	VBUS	1	0: Unmask VBUS Interrupt 1: Mask VBUS Interrupt

# TSU6721YFF

SCDS345 –JUNE 2013

[www.ti.com](http://www.ti.com)

## ADC Value

Address: 07h

Reset Value: xxx11111

Type: Read

BIT NO.	NAME	SIZE (BITS)	DESCRIPTION
4-0	ADC value	5	ADC value read from ID
7-5	Unused	3	

## Timing Set 1

Address: 08h

Reset Value: 00000000

Type: Read/Write

BIT NO.	NAME	SIZE (BITS)	DESCRIPTION
3-0	Device Sleep	4	Device Sleep duration
7-4	Key press	4	Normal key press duration

## Timing Set 2

Address: 09h

Reset Value: 00000000

Type: Read/Write

BIT NO.	NAME	SIZE (BITS)	DESCRIPTION
3-0	Long key press	4	Long key press duration
7-4	Switching wait	4	Waiting duration before switching

**Time Table**

SETTING VALUE	DEVICE SLEEP	KEY PRESS	LONG KEY PRESS	SWITCHING WAIT(1)
0000	50 ms	100 ms	300 ms	10 ms
0001	100 ms	200 ms	400 ms	30 ms
0010	150 ms	300 ms	500 ms	50 ms
0011	200 ms	400 ms	600 ms	70 ms
0100	300 ms	500 ms	700 ms	90 ms
0101	400 ms	600 ms	800 ms	110 ms
0110	500 ms	700 ms	900 ms	130 ms
0111	600 ms	800 ms	1000 ms	150 ms
1000	700 ms	900 ms	1100 ms	170 ms
1001	800 ms	1000 ms	1200 ms	190 ms
1010	900 ms	–	1300 ms	210 ms
1011	1000 ms	–	1400 ms	–
1100	–	–	1500 ms	–
1101	–	–	–	–
1110	–	–	–	–
1111	–	–	–	–

**Device Type 1**

Address: 0Ah

Reset Value: 00000000

Type: Read

BIT NO.	NAME	SIZE (BITS)	DESCRIPTION
0	Audio type 1	1	Audio device type 1
1	Audio type 2	1	Audio device type 2
2	USB	1	USB host
3	UART	1	UART
4	Type1/Type2	1	Type1/Type2 Charger
5	CDP	1	Charging Downstream Port (USB Host Hub Charger)
6	DCP	1	Dedicated Charging Port
7	USB OTG	1	USB on-the-go device

**Device Type 2**

Address: 0Bh

Reset Value: 00000000

Type: Read

BIT NO.	NAME	SIZE (BITS)	DESCRIPTION
0	JIG_USB_ON	1	Factory mode cable
1	JIG_USB_OFF	1	Factory mode cable
2	JIG_UART_ON	1	Factory mode cable
3	JIG_UART_OFF	1	Factory mode cable
4	PPD	1	Phone-powered device
5	TTY	1	TTY converter
6	A/V	1	A/V Cable
7	Audio Type 3	1	Audio device type 3

## TSU6721YFF

SCDS345 –JUNE 2013

[www.ti.com](http://www.ti.com)

### Button 1

Address: 0Ch

Reset Value: 00000000

Type: Read and Clear

BITS NO.	NAME	SIZE (BITS)	DESCRIPTION
0	Send_End	1	Send_End key is pressed
1	1	1	Number 1 key is pressed
2	2	1	Number 2 key is pressed
3	3	1	Number 3 key is pressed
4	4	1	Number 4 key is pressed
5	5	1	Number 5 key is pressed
6	6	1	Number 6 key is pressed
7	7	1	Number 7 key is pressed

### Button 2

Address: 0Dh

Reset Value: x0000000

Type: Read and Clear

BITS NO.	NAME	SIZE (BITS)	DESCRIPTION
0	8	1	Number 8 key is pressed
1	9	1	Number 9 key is pressed
2	10	1	Number 10 key is pressed
3	11	1	Number 11 key is pressed
4	12	1	Number 12 key is pressed
5	Error	1	Error key is pressed
6	Unknown	1	Unknown key is pressed
7	Unused	1	

**Manual S/W 1**

Address: 13h

Reset Value: 00000000

Type: Read/Write

BIT NO.	NAME	SIZE (BITS)	DESCRIPTION
1-0	V <sub>BUS</sub> Switching	2	00: Open all switch 01: V <sub>BUS</sub> is connected to V <sub>BUS_OUT</sub> (charger) 10: V <sub>BUS</sub> is connected to MIC
4-2	DP Switching	3	000: Open all switch 001: DP is connected to DP_HT of USB port 010: DP is connected to S_R 011: DP is connected to RxD of UART 100: Reserved 101: DP is connected to MIC 110-111: Reserved
7-5	DM Switching	3	000: Open all switch 001: DM is connected to DM_HT of USB port 010: DM is connected to S_L 011: DM is connected to TxD of UART 100-111: Reserved

**Manual S/W 2**

Address: 14h

Reset Value: xxx00000

Type: Read/Write

BIT NO.	NAME	SIZE (BITS)	DESCRIPTION
1-0	ID Switching	2	00: Open all switch 01: Reserved 10: ID is connected to IDBP 11: Reserved
2	JIG	1	0: Low (JIG OFF) 1: High (JIG ON)
3	BOOT	1	0: Low (BOOT OFF) 1: High (BOOT ON)
4	ISET	1	0: Low (ISET OFF) 1: High (ISET ON)
7-5	Unused	3	

## TSU6721YFF

SCDS345 –JUNE 2013

[www.ti.com](http://www.ti.com)

### Device Type 3

Address: 15h

Reset Value: x000x000

Type: Read

BIT NO.	NAME	SIZE (BITS)	DESCRIPTION
0	MHL	1	MHL device detected
1	VBUS Debounce	1	This bit goes high after the 8ms VBUS debounce time
2	VBUS Non-Standard	1	A non-standard charger device detected. This bit goes high after BCDv1.2 timer expires
3	Unused	1	
4	A/V VBUS	1	A/V Dock with VBUS connected
5	Apple Chg	1	Apple Charger
6	U200 Chg	1	U200 Charger
7	Video	1	75 Ohm video cable

### Reset

Address:1Bh

Reset Value: xxxxxxx0

Type: Write

BIT NO.	NAME	SIZE (BITS)	DESCRIPTION
0	Reset	1	Manual reset on device
7-1	Unused	6	

**Timer Setting**

Address: 20h

Reset Value:00010101

Type: Read and Write

BIT NO.	NAME	SIZE (BITS)	DESCRIPTION
2-0	ADC Start Time	3	000: 1ms 001: 2ms 010: 4ms 011: 8ms 100: 12ms 101: 16ms 110: 20ms 111: 24ms
5-3	BCDv1.2 Timer	3	000: 0.6s 001: 1.2s 010: 1.8s 011: 2.4s 100: 3s 101: 3.6s
6	Load Switch Enable Time	1	0: 150ms 1: 450ms
7	ISET Enable Time	1	0: 40ms 1:100ms

**OCP Setting 1**

Address: 21h

Reset Value:001010x1

Type: Read and Write

BIT NO.	NAME	SIZE (BITS)	DESCRIPTION
0	BCDv1.2 Enable	1	0: disabled 1: enabled
1	Unused	1	
4-2	OCP Timeout Delay	3	000: 1ms 001: 2ms 010: 4ms 011: 8ms 100: 12ms 101: 16ms
7-5	OCL Current Limiter Setting	1	000: 1.5A 001: 2.0A 010: 2.5A 011: 2.5A

## TSU6721YFF

SCDS345 –JUNE 2013

[www.ti.com](http://www.ti.com)

### OCP Setting 2

Address: 22h

Reset Value:xxx11001

Type: Read and Write

BIT NO.	NAME	SIZE (BITS)	DESCRIPTION
2-0	OCP Protection Level Setting	3	000: 1.0A 001: 1.5A 010: 2.0A 011: 2.0A
4-3	OC Enable	2	00: OCP & OCL disabled 01: OCP disabled & OCL enabled 10: Unused 11: OCP & OCL enabled
7-5	Unused	3	

### Device Type 4

Address: 23h

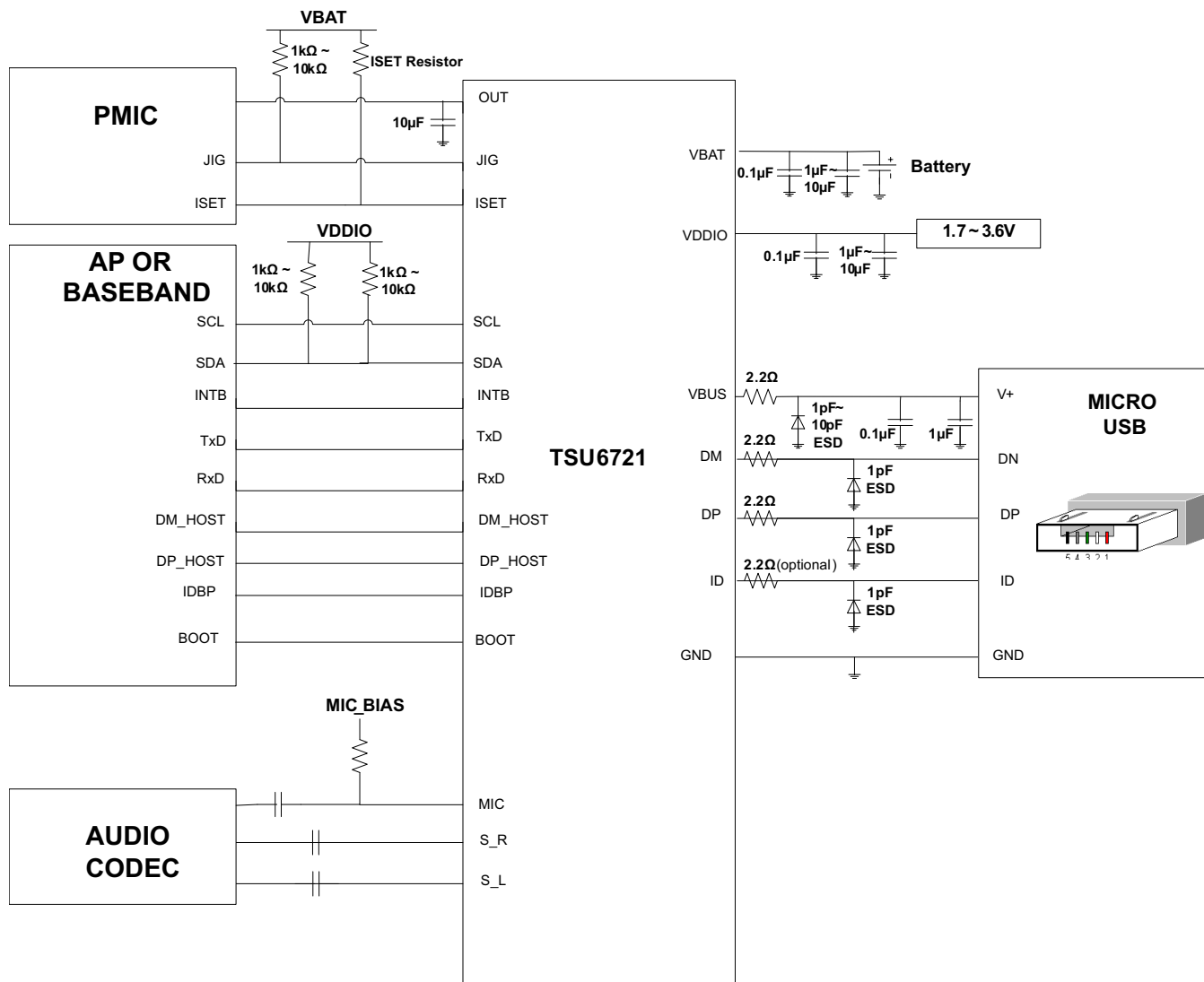
Reset Value:xxxxx111

Type: Read and Write

BIT NO.	NAME	SIZE (BITS)	DESCRIPTION
2-0	MCPC ID Resistor Value	3	000: 47k ohms 001: 180k ohms 010: 390k ohms 011: 287k ohms (Mode 1) 100: 557k ohms (Mode 3) 101: 797k ohms (Mode 2) 110: Error 111: Reset
7-3	Unused	5	



## APPLICATION SCHEMATIC



## CRITICAL COMPONENTS

PIN NAME	PIN NUMBER	CRITICAL COMPONENT
VBUS	A5, B5	2.2 $\Omega$
VDDIO	D3	1 $\mu$ F~10 $\mu$ F
		0.1 $\mu$ F
VBAT	C3	1 $\mu$ F~10 $\mu$ F
		Battery
		0.1 $\mu$ F
JIG	E3	1 k $\Omega$ ~10 k $\Omega$
MIC	B3	2.2 k $\Omega$
		10 $\mu$ F
ISSET	A2	Resistor determined by Battery Charger
S_R	D4	220 $\mu$ F <sup>(1)</sup>
S_L	C4	220 $\mu$ F <sup>(1)</sup>
OUT	A4, B4	10 $\mu$ F
SCL	A1	1 k $\Omega$ ~10 k $\Omega$
SDA	B1	1 k $\Omega$ ~10 k $\Omega$
DM	C5	2.2 $\Omega$
		ESD Protection Diode
DP	D5	2.2 $\Omega$
		ESD Protection Diode
ID	E5	2.2 $\Omega$ <sup>(1)</sup>
		ESD Protection Diode

(1) Optional Components

## SCHEMATIC GUIDELINES

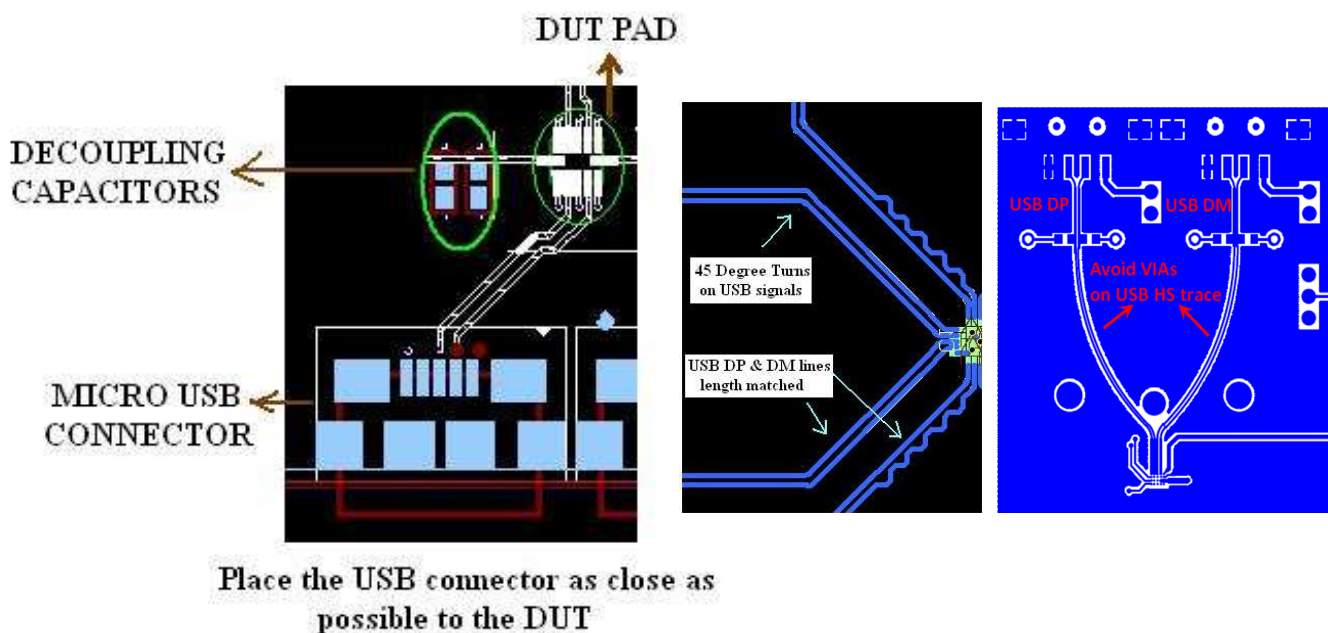
- VBUS, VDDIO, and VBAT require decoupling capacitors to reduce noise from circuit elements. The capacitors act as a shunt to block off the noise. The 0.1 $\mu$ F capacitor smoothes out high frequencies and has a lower series inductance. The 1 $\mu$ F~10 $\mu$ F and 1 $\mu$ F capacitors smooth out the lower frequencies and have a much higher series inductance. Placing both decoupling capacitors will provide better load regulation across the frequency spectrum.
- OUT requires a 10 $\mu$ F load capacitor to prevent sudden increases of voltage on the pin during charging
- JIG is an open-drain output and therefore requires a 1k $\Omega$  ~ 10k $\Omega$  pull-up resistor to VBAT
- ISSET is an open drain output. It can be used by the battery charger to set the input current limit with a series resistor (for example 75 $\Omega$  determined by the charger)
- SCL and SDA require 1k $\Omega$  ~ 10k $\Omega$  pull-up resistors to VDDIO to prevent floating inputs
- Depending on the codec used, S\_R and S\_L may require DC blocking capacitors as high as 220 $\mu$ F. The capacitor might not be needed if the codec has the capability to provide ground centered signals.
- Mic requires a 2.2k $\Omega$  pull-up resistor to MIC\_BIAS to provide DC bias for the microphone. Additionally the 10 $\mu$ F capacitor is required to block the DC signals from MIC\_BIAS to the Audio Codec
- VBUS, DM and DP are recommended to have an external resistor 2.2 $\Omega$  to provide extra ballasting to protect the chip and internal circuitry
  - For ID, if there is less stress on the ID pin then the external 2.2 $\Omega$  resistor is optional

9. DDM, DP, and ID are rated for 6kV IEC contact discharge protection. To prevent failure in case of an IEC contact discharge of 8kV or greater, it is recommended to have an external ESD Protection Diode (~1pF of capacitance allowed) rated for greater than 8kV IEC protection. It is also recommended to have an external ESD Protection Diode to prevent DP and DM from failure in the event of EOS related to electrical surge propagated downstream from the AC power supply
10. VBUS is rated for 6kV IEC contact discharge protection. To prevent failure in case of an IEC contact discharge of 8kV or greater, it is recommended to have an external ESD Protection Diode (~1pF of capacitance allowed) rated for greater than 8kV IEC protection. It is also recommended to have an external ESD Protection Diode to prevent VBUS from failure in the event of EOS related to electrical surge propagated downstream from the AC power supply.

## PCB ROUTING GUIDELINES

### Routing Guidelines for USB Signal Integrity

1. All the USB lines DP\_CON, DM\_CON, DP\_HT, DM\_HT, TxD and RxD
  - (a) Must have 45Ω single ended characteristic impedance
  - (b) Must have 90Ω differential ended impedance
  - (c) To fulfill USB 2.0 requirements
2. TSU6721 location
  - (a) Close to the USB connector as possible
  - (b) The distance between the USB controller and the device less than 1 inch
  - (c) Shorter length of the trace will reduce effect of stray noise and radiate less EMI
3. Minimize use of VIAs for USB related signals
  - (a) Differential transmission lines should be matched as close as possible
  - (b) No VIAs for optimum USB2.0 performance



## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TSU6721YFFR	ACTIVE	DSBGA	YFF	25	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TSU6721	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TSU6721YFFR	DSBGA	YFF	25	3000	180.0	8.4	2.17	2.17	0.57	4.0	8.0	Q1

## TAPE AND REEL BOX DIMENSIONS

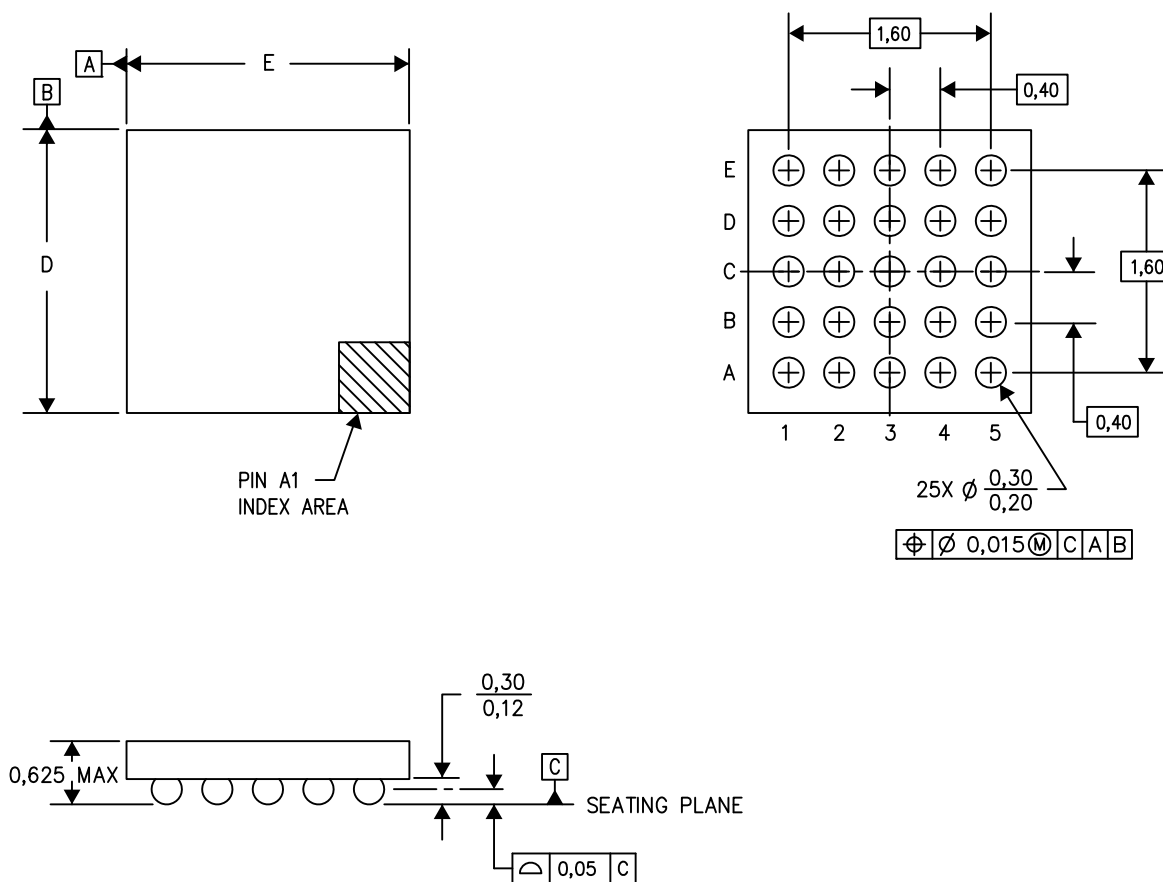


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TSU6721YFFR	DSBGA	YFF	25	3000	182.0	182.0	17.0

YFF (S-XBGA-N25)

DIE-SIZE BALL GRID ARRAY



D: Max = 2.096 mm, Min = 2.036 mm

E: Max = 2.096 mm, Min = 2.036 mm

4207625-10/AN 07/13

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. NanoFree™ package configuration.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

### Products

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
OMAP Applications Processors	<a href="http://www.ti.com/omap">www.ti.com/omap</a>
Wireless Connectivity	<a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a>

### Applications

Automotive and Transportation	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Communications and Telecom	<a href="http://www.ti.com/communications">www.ti.com/communications</a>
Computers and Peripherals	<a href="http://www.ti.com/computers">www.ti.com/computers</a>
Consumer Electronics	<a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>
Energy and Lighting	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Space, Avionics and Defense	<a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a>
Video and Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>

### TI E2E Community

[e2e.ti.com](http://e2e.ti.com)