

SP2T Switch with Impedance Detection Micro-USB Switch to Support USB, UART

Check for Samples: [TSU6111](#)

FEATURES

- **Dual SP2T**
 - USB & UART Path support USB 2.0 High Speed
- **Smart Detection**
 - Plug-in/Un-plug Detection
 - USB Charger Detection
 - Impedance Detection
 - Detection is Compatible to CEA-936A (4-Wire Protocol, UART interface)
- **Charger Detection**
 - USB BCDv1.1 Compliant
 - VBUS Detection
 - Data Contact Detection
 - Primary and Secondary Detection
- **Compatible Accessories**
 - USB Cable
 - UART Cable
 - USB Charger BCDv1.1
- **Additional Features**
 - I²C Interface with Host Processor
 - Support Control Signals Used In Manufacturing (JIG, BOOT)
 - Interrupt for Attach and Detach Accessory
- **Max Voltage**
 - 28v VBUS rating
- **ESD Performance Tested Per JESD 22**
 - 2000-V Human-Body Model (A114-B, Class II)
 - 1000-V Charged-Device Model (C101)
- **ESD Performance DP/DM/ID/VBUS to GND**
 - ±8kV Contact Discharge (IEC 61000-4-2)
- **Surge Protection on VBUS/DP/DM**
 - USB Connector Pins Without External Components

APPLICATIONS

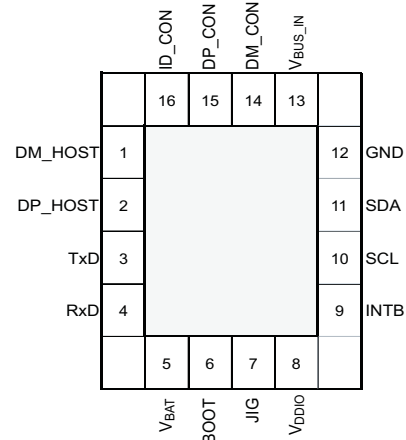
- Cell Phones and Smart Phones
- Tablet PCs
- Digital Cameras and Camcorders
- GPS Navigation Systems
- Micro USB interface with USB/UART

DESCRIPTION

The TSU6111 is a differential high performance automated SP2T switch with impedance detection. The switch features impedance detection which supports the detection of various accessories that are attached through DP, DM and ID. The charger detection satisfies USB charger specification v1.1. V_{BUS_IN} has 28V tolerance to avoid external protection.

Power for this device is supplied through V_{BAT} of the system or through V_{BUS_IN} when attached.

The switch is controlled by automatic detection logic or through I²C manually. JIG and BOOT pins are used when a USB, UART JIG cable is used to test in the development and manufacturing. TSU6111 has open-drain JIG output (active low).

QFN-RSV PIN-OUT


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



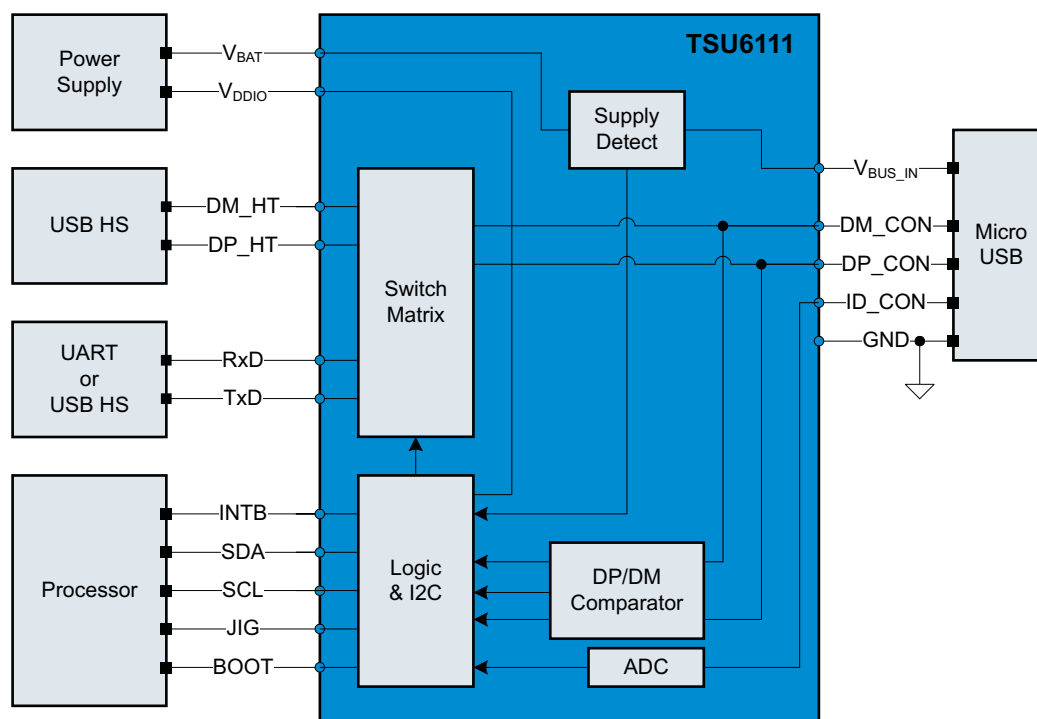
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION⁽¹⁾

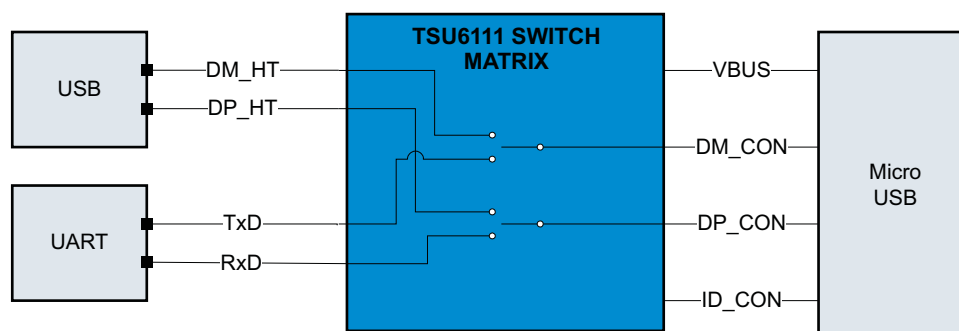
| T _A | PACKAGE ⁽²⁾ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|-------------------------|---------------|-----------------------|------------------|
| –40°C to 85°C | uQFN 0.4-mm pitch – RSV | Tape and Reel | TSU6111RSVR | ZTC |

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.
 (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

BLOCK DIAGRAM



SWITCH MATRIX



PIN FUNCTIONS

| PIN | | I/O | DESCRIPTION |
|-----|---------|-----|---|
| NO. | NAME | | |
| 1 | DM_HOST | I/O | USB DM connected to host |
| 2 | DP_HOST | I/O | USB DP connected to host |
| 3 | TxD | I/O | UART Tx |
| 4 | RxD | I/O | UART Rx |
| 5 | VBAT | I | Connected to battery |
| 6 | BOOT | O | BOOT mode out (push-pull) |
| 7 | JIG | O | JIG detection (TSU6111 open-drain active low) |
| 8 | VDDIO | O | I/O voltage reference |
| 9 | INTB | O | Interrupt to host (push-pull) |
| 10 | SCL | I | I2C clock |
| 11 | SDA | I/O | I2C data |
| 12 | GND | | Ground |
| 13 | VBUS_IN | I | VBUS connected to USB receptacle |
| 14 | DM_CON | I/O | USB DM connected to USB receptacle |
| 15 | DP_CON | I/O | USB DP connected to USB receptacle |
| 16 | ID_CON | I/O | USB ID connected to USB receptacle |

SUMMARY OF TYPICAL CHARACTERISTICS

| T_A = 25°C | USB Path |
|---|-------------------------|
| Number of channels | 2 |
| ON-state resistance (r_{on}) | 8 Ω |
| ON-state resistance match (Δr_{on}) | 0.5 Ω |
| ON-state resistance flatness ($r_{on(flat)}$) | 0.5 Ω |
| Turn-on/turn-off time (t_{ON}/t_{OFF}) | 95 μ s/ 3.5 μ s |
| Bandwidth (BW) | 920 MHz |
| OFF isolation (O_{ISO}) | –26 dB at 250 MHz |
| Crosstalk (X_{TALK}) | –32 dB at 250 MHz |
| Leakage current ($I_{IO(ON)}$) | 50 nA |

ABSOLUTE MAXIMUM RATINGS⁽¹⁾⁽²⁾

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|----------------------|---|--------------------|------|-----------------------|------|
| V _{BUS} | Supply voltage from USB connector | | –0.5 | 28 | V |
| V _{BAT} | Supply voltage from battery | | –0.5 | 6.0 | |
| V _{DDIO} | Logic supply voltage | | –0.5 | 4.6 | V |
| V _{USBIO} | Switch I/O voltage range | USB Switch | –0.5 | V _{BAT} +0.5 | V |
| V _{UARTIO} | Switch I/O voltage range | UART Switch | –0.5 | V _{BAT} +0.5 | V |
| I _K | Analog port diode current | | –50 | 50 | mA |
| I _{SW-DC} | ON-state continuous switch current | | –60 | 60 | mA |
| I _{SWPEAK} | ON-state peak switch current | | –150 | 150 | mA |
| I _{IK} | Digital logic input clamp current | V _L < 0 | | –50 | mA |
| I _{LOGIC_O} | Continuous current through logic output | | –50 | 50 | mA |
| I _{GND} | Continuous current through GND | | | 100 | mA |
| T _{stg} | Storage temperature range | | –65 | 150 | °C |

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
- (2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

THERMAL IMPEDANCE RATINGS

| | | | UNIT |
|-----|---------------------------|-------------|----------|
| θJA | Package thermal impedance | RSV package | 184 °C/W |

ELECTRICAL SPECIFICATION

over operating free-air temperature range (unless otherwise noted)

| PARAMETERS | | TEST CONDITIONS | MIN | MAX | UNIT |
|---|--|---|-------------------------|-------------------------|------|
| DIGITAL SIGNALS – I2C INTERFACE (SCL and SDA) | | | | | |
| V _{DDIO} | Logic and I/O supply voltage | | 1.65 | 3.6 | V |
| V _{IH} | High-level input voltage | | V _{DDIO} × 0.7 | V _{DDIO} | V |
| V _{IL} | Low-level input voltage | | 0 | V _{DDIO} × 0.3 | V |
| V _{OH} | High-level output voltage | I _{OH} = –3 mA | V _{DDIO} × 0.7 | | V |
| V _{OL} | Low-level output voltage | I _{OL} = 3 mA | | 0.4 | V |
| f _{SCL} | SCL frequency | | | 400 | kHz |
| JIG OUTPUT (TSU6111 – OPEN-DRAIN OUTPUT, ACTIVE LOW) | | | | | |
| V _{OL} | Low-level output voltage | I _{OL} = 10 mA, V _{BAT} = 3.0 V | | 0.5 | V |
| INTB AND BOOT (PUSH-PULL OUTPUT) | | | | | |
| V _{OH} | High-level output voltage | I _{OH} = –4 mA, V _{DDIO} = 1.65 V | 1.16 | | V |
| V _{OL} | Low-level output voltage | I _{OL} = 4 mA, V _{DDIO} = 1.65 V | | 0.33 | V |
| TOTAL SWITCH CURRENT CONSUMPTION | | | | | |
| I _{DD(Standby)} | V _{BAT} Standby current consumption | V _{BUS_IN} = 0 V, Idle state | | 30 | μA |
| I _{DD(Operating)} | V _{BAT} Operating current consumption | V _{BUS_IN} = 0 V, USB switches ON | | 75 | μA |

ELECTRICAL CHARACTERISTICS⁽¹⁾

V_{BAT} = 3 V to 4.4 V, V_{DDIO} = 2.8 V, T_A = –40°C to 85°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|---|-----|-----|------------------|------|
| ANALOG SWITCH | | | | | | |
| V _{USBIO} | Analog signal range | | 0 | | V _{BAT} | V |
| r _{ON} | ON-state resistance | DM_HT, DP_HT, DM_CON, DP_CON V _I = 0 V to 3.6 V, I _O = –2 mA, V _{BAT} = 3.0 V | | 8 | 15 | Ω |
| Δr _{ON} | ON-state resistance match between channels | DM_HT, DP_HT, DM_CON, DP_CON V _I = 0.4 V, I _O = –2 mA, V _{BAT} = 3.0 V | | 0.5 | 2 | Ω |
| r _{ON(flat)} | ON-state resistance flatness | DM_HT, DP_HT, DM_CON, DP_CON V _I = 0 V to 3.6 V, I _O = –2 mA, V _{BAT} = 3.0 V | | 0.5 | 2 | Ω |
| I _{IO(OFF)} | V _I or V _O OFF leakage current | V _I = 0.3 V, V _O = 2.7 V or V _I = 2.7 V, V _O = 0.3 V, V _{BAT} = 4.4 V, Switch OFF | | 45 | 200 | nA |
| I _{IO(ON)} | V _O ON leakage current | V _I = OPEN, V _O = 0.3 V or 2.7 V, V _{BAT} = 4.4 V, Switch ON | | 50 | 200 | nA |
| DYNAMIC | | | | | | |
| t _{ON} | Turn-ON time | From receipt of I ² C ACK bit V _I or V _O = V _{BAT} , R _L = 50 Ω, C _L = 35 pF | | 95 | | μs |
| t _{OFF} | Turn-OFF time | From receipt of I ² C ACK bit V _I or V _O = V _{BAT} , R _L = 50 Ω, C _L = 35 pF | | 3.5 | | μs |
| C _{I(OFF)} | V _I OFF capacitance | DC bias = 0 V or 3.6 V, f = 10 MHz, Switch OFF | | 4 | | pF |
| C _{O(OFF)} | V _O OFF capacitance | DC bias = 0 V or 3.6 V, f = 10 MHz, Switch OFF | | 7 | | pF |
| C _{I(ON)} , C _{O(ON)} | V _I , V _O ON capacitance | DC bias = 0 V or 3.6 V, f = 10 MHz, Switch ON | | 9 | | pF |
| BW | Bandwidth | R _L = 50 Ω, Switch ON | | 920 | | MHz |
| O _{ISO} | OFF Isolation | f = 240 MHz, R _L = 50 Ω, Switch OFF | | –26 | | dB |
| X _{TALK} | Crosstalk | f = 240 MHz, R _L = 50 Ω | | –32 | | dB |

(1) V_O is equal to the asserted voltage on DP_CON and DM_CON pins. V_I is equal to the asserted voltage on DP_HT and DM_HT pins. I_O is equal to the current on the DP_CON and DM_CON pins. I_I is equal to the current on the DP_HT and DM_HT pins.

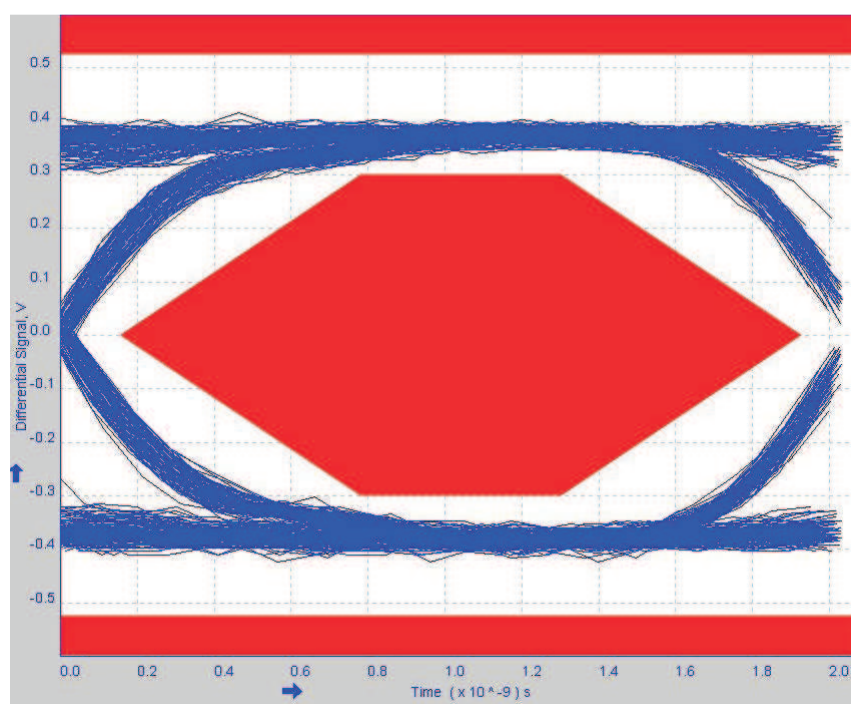
GENERAL OPERATION

The TSU6111 will automatically detect accessories plugged into the phone via the mini/micro USB 5 pin connector. The type of accessory detected will be stored in I2C registers within the TSU6111 for retrieval by the host. The TSU6111 has a network of switches that can be automatically opened and closed based on the accessory detection. See the [Table 1](#) for details of which switches are open during each mode of operation. For flexibility, the TSU6111 also offers a manual switching mode allowing the host processor to decide which switches should be opened and closed and execute the settings through the I²C interface.

STANDBY MODE

Standby mode is the default mode upon power up and occurs when no accessory has been detected. During this mode, the VBUS and ID lines are continually monitored through comparators to determine when an accessory is inserted. Power consumption is minimal during standby mode.

EYE DIAGRAM USB 2.0 HIGH SPEED



ACCESSORY ID DETECTION

If V_{BUS_IN} is high and the attachment is not a charger, then determine the impedance on the ID pin. If V_{BUS_IN} is low and an accessory is attached, then use an ADC for impedance sensing on the ID pin to identify which accessory is attached.

IMPEDANCE BUCKETS FOR EACH ACCESSORY

In order to implement ID detection, each accessory should contain below ID impedance resistor value which is 5% tolerance accuracy.

Table 1. Accessory ID and Switch States

| ACCESSORY | DETECTED IMPEDANCE ON ID | RESISTOR TOLERANCE (%) | ADC VALUE | SWITCH STATE | | FACTORY CABLE | |
|------------------------------------|--------------------------------|------------------------------|--------------|--------------|------|---------------|------|
| | | | | DP/DM | | JIG | BOOT |
| | | | | USB | UART | | |
| OTG | 0 | — | 00000 | ON | OFF | OFF | OFF |
| Send_End Button | 2K | 10% | 00001 | OFF | OFF | OFF | OFF |
| Audio Device Type 3 | 28.7K | 5% | 01110 | OFF | OFF | OFF | OFF |
| Reserved Accessory #1 | 34K | 5% | 01111 | OFF | OFF | OFF | OFF |
| Reserved Accessory #2 | 40.2K | 5% | 10000 | OFF | OFF | OFF | OFF |
| Reserved Accessory #3 | 49.9K | 5% | 10001 | OFF | OFF | OFF | OFF |
| Reserved Accessory #4 | 64.9K | 5% | 10010 | OFF | OFF | OFF | OFF |
| Audio Device Type 2 | 80.27K | 5% | 10011 | OFF | ON | OFF | OFF |
| Phone Powered Device | 102K | 5% | 10100 | OFF | ON | OFF | OFF |
| TTY Converter | 121K | 5% | 10101 | OFF | OFF | OFF | OFF |
| UART Cable | 150K | 5% | 10110 | OFF | ON | OFF | OFF |
| Type 1 Charger | 200K | 5% | 10111 | OFF | OFF | OFF | OFF |
| Factory Mode Cable - Boot Off USB | 255K | 5% | 11000 | ON | OFF | ON | OFF |
| Factory Mode Cable - Boot On USB | 301K | 5% | 11001 | ON | OFF | ON | ON |
| Audio/Video Cable | 365K | 5% | 11010 | OFF | OFF | OFF | OFF |
| Type 2 Charger | 442K | 5% | 11011 | OFF | OFF | OFF | OFF |
| Factory Mode Cable - Boot Off UART | 523K | 5% | 11100 | OFF | ON | ON | OFF |
| Factory Mode Cable - Boot On UART | 619K | 5% | 11101 | OFF | ON | ON | ON |
| Stereo Headset with Remote | 1000.07K | 10% | 11110 | OFF | OFF | OFF | OFF |
| Mono/Stereo Headset | 1002K | 10% | 11110 | OFF | OFF | OFF | OFF |
| No ID | — | — | 11111 | OFF | OFF | OFF | OFF |
| USB Standard Downstream Port | — | — | 11111 | ON | OFF | OFF | OFF |
| USB Charging Downstream Port | — | — | 11111 | ON | OFF | OFF | OFF |
| Dedicated Charging Port | — | — | 11111 | OFF | OFF | OFF | OFF |

Power-On Reset

When power (from 0 V) is applied to VBAT, an internal power-on reset holds the TSU6111 in a reset condition until V_{BAT} has reached V_{POR} . At that point, the reset condition is released, and the TSU6111 registers and I2C state machine initialize to their default states.

After the initial power-up phase, VBAT must be lowered to below 0.2 V and then back up to the operating voltage (V_{DDIO}) for a power-reset cycle.

Software Reset

The TSU6111 has software reset feature.

- Hold low both I²C_SCL and I²C_SDA more than 30ms will reset digital logic of the TSU6111.

After reset digital logic, INTB will keep low until INT_Mask bit of Control register (0x02) is cleared.

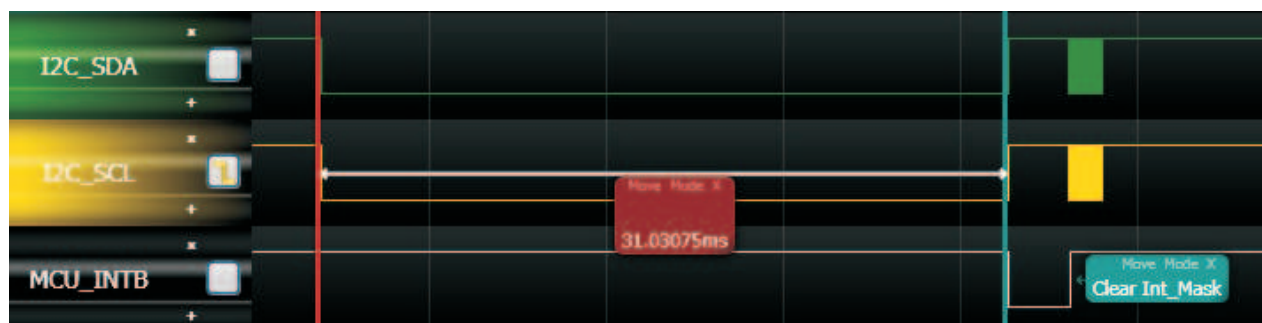


Figure 1. Software Reset

Standard I²C Interface Details

The bidirectional I²C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I²C communication with this device is initiated by the master sending a START condition, a high-to-low transition on the SDA input/output while the SCL input is high (see Figure 2). After the start condition, the device address byte is sent, MSB first, including the data direction bit (R/W). This device does not respond to the general call address. After receiving the valid address byte, this device responds with an ACK, a low on the SDA input/output during the high of the ACK-related clock pulse.

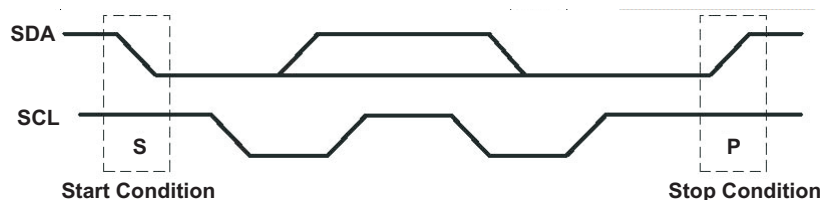


Figure 2. Definition of Start and Stop Conditions

The data byte follows the address ACK. The R/W bit is kept low for transfer from the master to the slave. The data byte is followed by an ACK sent from this device. Data are output only if complete bytes are received and acknowledged. The output data is valid at time (tpv) after the low-to-high transition of SCL, during the clock cycle for the ACK.

On the I²C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (START or STOP) (see Figure 3).

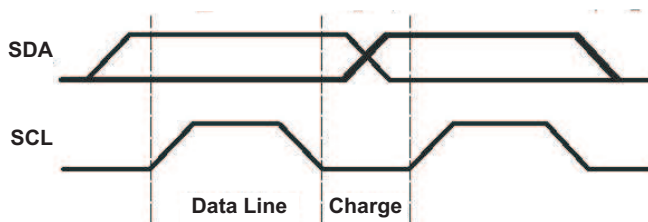


Figure 3. Bit Transfer

A Stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master (see Figure 2).

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit.

A slave receiver that is addressed must generate an ACK after the reception of each byte. The device that acknowledges has to pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period (see Figure 4). Setup and hold times must be taken into account.

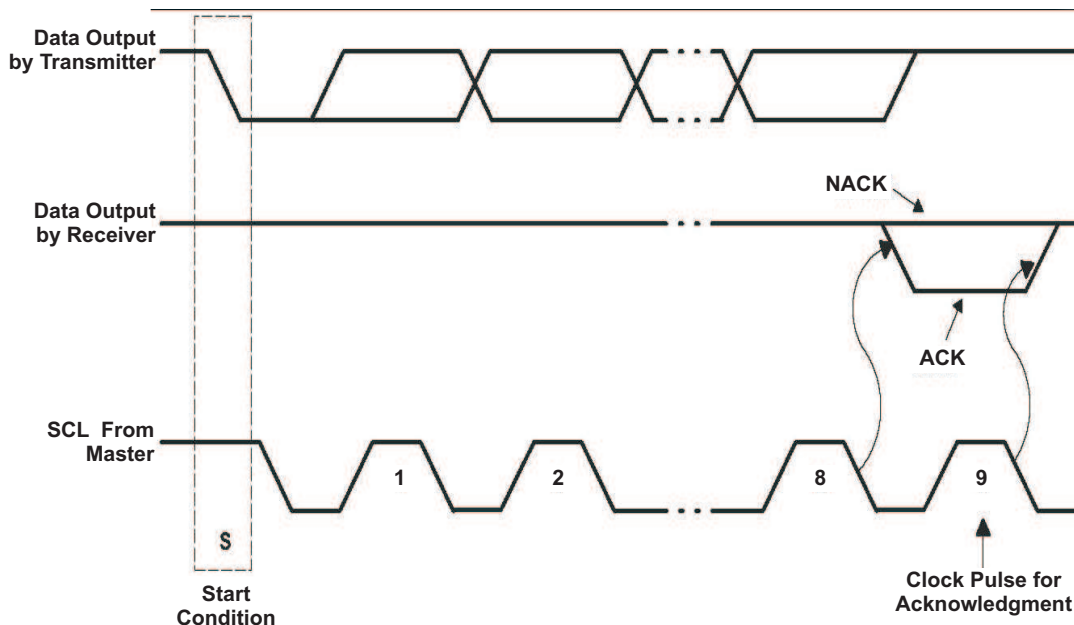


Figure 4. Acknowledgment on I²C Bus

Writes

Data is transmitted to the TSU6111 by sending the device slave address and setting the LSB to a logic 0 (see Figure 5 for device address). The command byte is sent after the address and determines which register receives the data that follows the command byte. The next byte is written to the specified register on the rising edge of the ACK clock pulse.

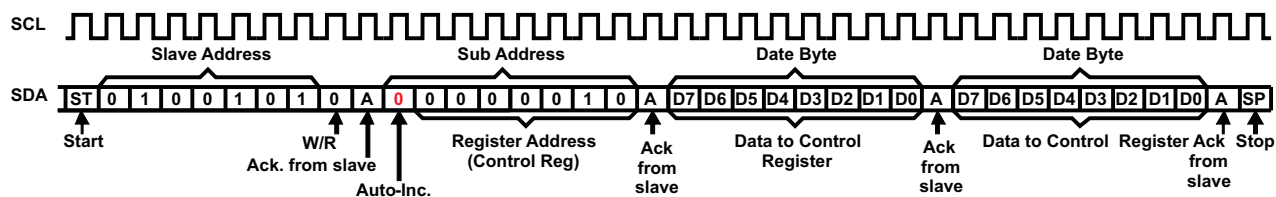


Figure 5. Repeated Data Write to a Single Register

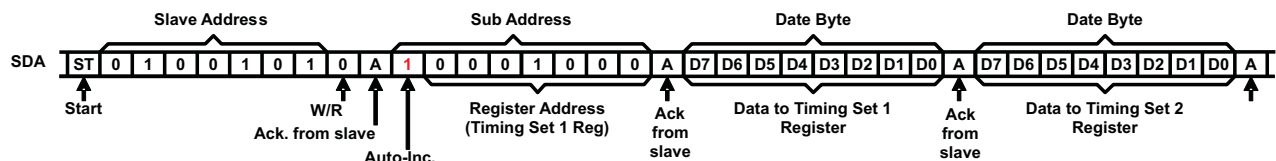


Figure 6. Burst Data Write to Multiple Registers

Reads

The bus master first must send the TSU6111 slave address with the LSB set to logic 0. The command byte is sent after the address and determines which register is accessed. After a restart, the device slave address is sent again but, this time, the LSB is set to logic 1. Data from the register defined by the command byte then is sent by the TSU6111. Data is clocked into the SDA output shift register on the rising edge of the ACK clock pulse. See Figure 7.

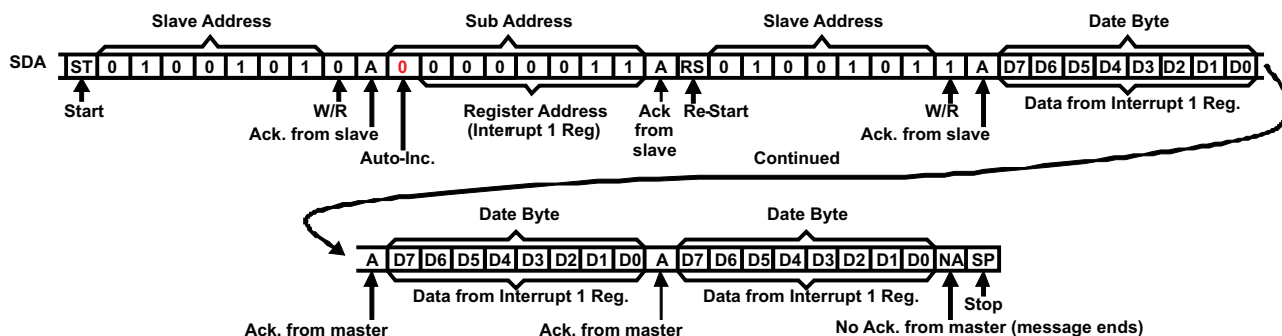


Figure 7. Repeated Data Read from a Single Register – Combined Mode

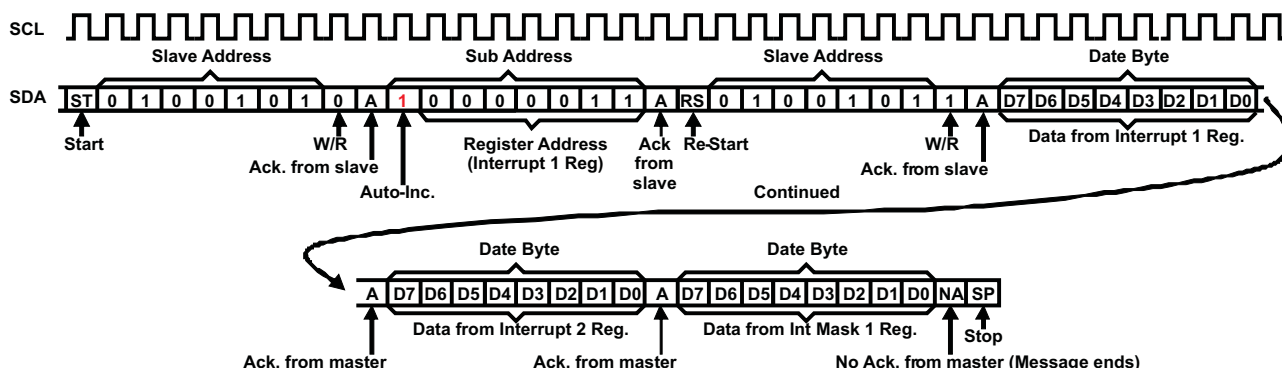


Figure 8. Burst Data Read from Multiple Registers – Combined Mode

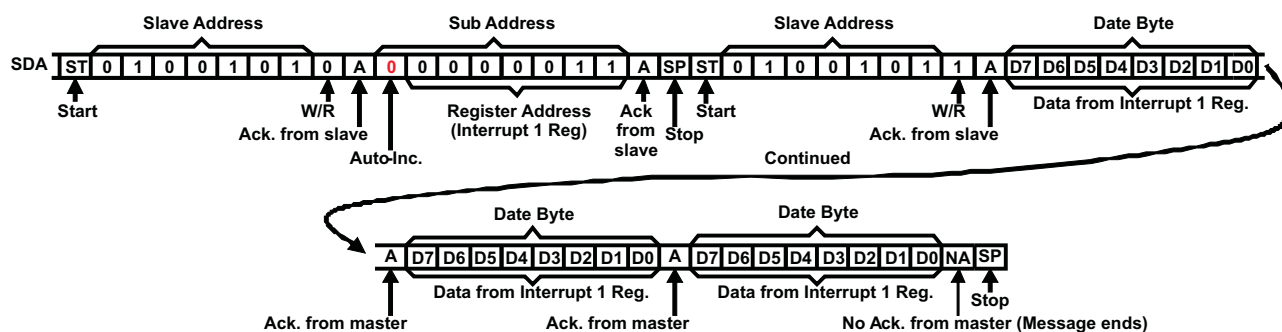


Figure 9. Repeated Data Read from a Single Register – Split Mode

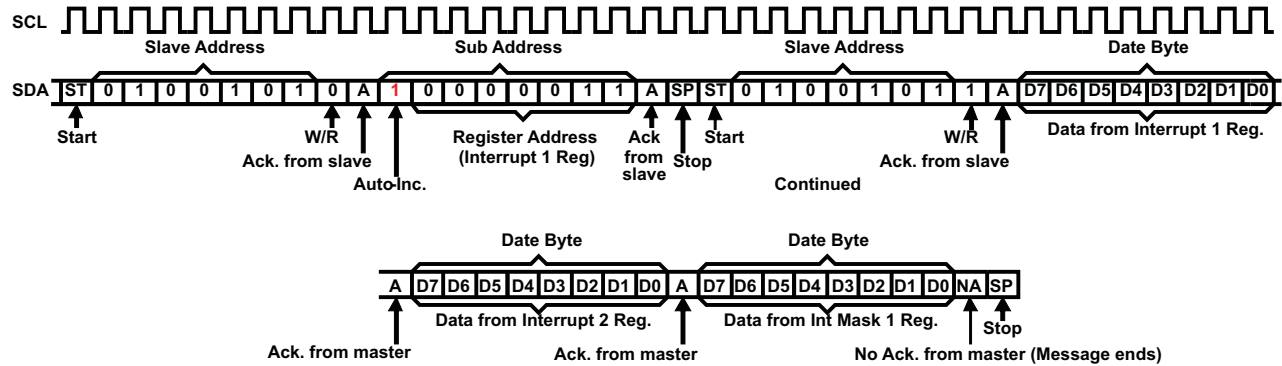


Figure 10. Burst Data Read from Multiple Registers – Split Mode

Notes (Applicable to Figure 5–Figure 10):

- SDA is pulled low on Ack. from slave or Ack. from master.
- Register writes always require sub-address write before first data byte.
- Repeated data writes to a single register continue indefinitely until Stop or Re-Start.
- Repeated data reads from a single register continue indefinitely until No Ack. from master.
- Burst data writes start at the specified register address, then advance to the next register address, even to the read-only registers. For these registers, data write appears to occur, though no data are changed by the writes. After register 14h is written, writing resumes to register 01h and continues until Stop or Re-Start.
- Burst data reads start at the specified register address, then advance to the next register address. Once register 14h is read, reading resumes from register 01h and continues until No Ack. from master.

I²C Register Map⁽¹⁾⁽²⁾⁽³⁾

| ADD R | REGISTER | TYPE | RESET VALUE | BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 |
|----------|---------------------|------|----------------|-----------------|---------|-------------|-------------------|------------------|-----------------|---------------------|------------------|
| 01h | Device ID | R | 00001010 | Version ID | | | | | Vendor ID | | |
| 02h | Control | R/W | xxx11111 | | | | Switch Open | Raw Data | Manual S/W | Wait | INT Mask |
| 03h | Interrupt 1 | R | 00000000 | OVP_OCP_ DIS | OCP_EN | OVP_EN | LKR | LKP | KP | Detach | Attach |
| 04h | Interrupt 2 | R | x0000000 | | OTP_EN | CONNE CT | Stuck_Key_RC V | Stuck_Key | ADC_Chang e | Reserved_Att ach | A/V_Charg ing |
| 05h | Interrupt Mask 1 | R/W | 00000000 | OVP_OCP_ DIS | OCP_EN | OVP_EN | LKR | LKP | KP | Detach | Attach |
| 06h | Interrupt Mask 2 | R/W | x0000000 | | OTP_EN | CONNE CT | Stuck_Key_RC V | Stuck_Key | ADC_Chang e | Reserved_Att ach | A/V_Charg ing |
| 07h | ADC | R | xxx11111 | ADC Value | | | | | | | |
| 08h | Timing Set 1 | R/W | 00000000 | | | | | Device Wake Up | | | |
| 09h | Timing Set 2 | R/W | 00000000 | Switching Wait | | | | | | | |
| 0Ah | Device Type 1 | R | 00000000 | USG OTG | DCP | CDP | Carkit | UART | USG | Audio Type2 | Audio Type1 |
| 0Bh | Device Type 2 | R | 00000000 | Audio Type3 | CHG A/V | TTY | PD | JIG_UART_ OFF | JIG_UART_ ON | JIG_USB_OF F | JIG_USB_ ON |
| 0Ch | Button 1 | R | 00000000 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | Send_End |
| 0Dh | Button 2 | R | x0000000 | | Unknown | Error | 12 | 11 | 10 | 9 | 8 |
| 13h | Manual S/W 1 | R/W | 000000xx | D– Switching | | | | | | | |
| 14h | Manual S/W 2 | R/W | xxxx00xx | | | | | BOOT_SW | JIG-ON | | |

- (1) Do not use blank register bits.
(2) Write “0” to the blank register bits.
(3) Values read from the blank register bits are not defined and invalid.

Slave Address

| NAME | SIZE (BITS) | DESCRIPTION | | | | | | | |
|---------------|-------------|-------------|-------|-------|-------|-------|-------|-------|-------|
| | | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| Slave address | 8 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | R/W |

Device ID

Address: 01h

Reset Value: 00001010

Type: Read

| BIT NO. | NAME | SIZE (BITS) | DESCRIPTION |
|---------|------------|-------------|--|
| 0-2 | Vendor ID | 3 | A unique number for vendor 010 for Texas Instruments |
| 3-7 | Version ID | 5 | A unique number for chip version 00001b for TSU6111 |

Control

Address: 02h

Reset Value: xxx11111

Type: Read/Write

| BIT NO. | NAME | SIZE (BITS) | DESCRIPTION |
|---------|-------------|-------------|--|
| 0 | INT Mask | 1 | 0: Unmask interrupt 1: Mask interrupt |
| 1 | Wait | 1 | 0: Wait until host re-sets this bit(WAIT bit) high 1: Wait until Switching timer is expired |
| 2 | Manual S/W | 1 | 0: Manual Switching 1: Automatic Switching |
| 3 | RAW Data | 1 | 0: Report the status changes on ID to Host 1: Don't report the status changes on ID |
| 4 | Switch Open | 1 | 0: Open all Switches 1: Automatic Switching by accessory status |
| 5-7 | Reserved | | |

Interrupt 1

Address: 03h

Reset Value: 00000000

Type: Read and Clear

| BIT NO. | NAME | SIZE (BITS) | DESCRIPTION |
|---------|-------------|-------------|--------------------------|
| 0 | Attach | 1 | 1: Accessory is attached |
| 1 | Detach | 1 | 1: Accessory is detached |
| 2 | KP | 1 | 1: Key press |
| 3 | LKP | 1 | 1: Long key press |
| 4 | LKR | 1 | 1: Long key release |
| 5 | OVP_EN | 1 | 1: OVP enabled |
| 6 | OCP_EN | 1 | 1: OCP enabled |
| 7 | OVP_OCP_DIS | 1 | 1: OCP_OCP disabled |

Interrupt 2

Address: 04h

Reset Value:x0000000

Type: Read and Clear

| BIT NO. | NAME | SIZE (BITS) | DESCRIPTION |
|---------|-----------------|-------------|--|
| 0 | A/V_Charging | 1 | 1: Charger detected when A/V cable is attached |
| 1 | Reserved_Attach | 1 | 1: Reserved Device is attached |
| 2 | ADC_Change | 1 | 1: ADC value is changed when RAW data is enabled |
| 3 | Stuck_Key | 1 | 1: Stuck Key is detected |
| 4 | Stuck_Key_RCV | 1 | 1: Stuck Key is recovered |
| 5 | Connect | 1 | 1: Switch is connected(closed) |
| 6 | OTP_EN | 1 | 1: Over Temperature Protection enabled |
| 7 | Reserved | | |

Interrupt Mask 1

Address: 05h

Reset Value:00000000

Type: Read/Write

| BIT NO. | NAME | SIZE (BITS) | DESCRIPTION |
|---------|-------------|-------------|--|
| 0 | Attach | 1 | 0: Unmask Attach Interrupt 1: Mask Attach Interrupt |
| 1 | Detach | 1 | 0: Unmask Key press Interrupt 1: Mask Detach Interrupt |
| 2 | KP | 1 | 0: Unmask Key press Interrupt 1: Mask Key press Interrupt |
| 3 | LKP | 1 | 0: Unmask Long key press Interrupt 1: Mask Long key press Interrupt |
| 4 | LKR | 1 | 0: Unmask Long key release Interrupt 1: Mask Long key release Interrupt |
| 5 | OVP_EN | 1 | 0: Unmask OVP_EN Interrupt 1: Mask OVP_EN Interrupt |
| 6 | OCP_EN | 1 | 0: Unmask OCP_EN Interrupt 1: Mask OCP_EN Interrupt |
| 7 | OVP_OCP_DIS | 1 | 0: Unmask OVP_OCP_DIS Interrupt 1: Mask OVP_OCP_DIS Interrupt |

Interrupt Mask 2

Address: 06h

Reset Value:x0000000

Type: Read/Write

| BIT NO. | NAME | SIZE (BITS) | DESCRIPTION |
|---------|-----------------|-------------|--|
| 0 | A/V_Charging | 1 | 0: Unmask A/V_Charging Interrupt 1: Mask A/V_Charging Interrupt |
| 1 | Reserved_Attach | 1 | 0: Unmask Reserved_Attach Interrupt 1: Mask Reserved_Attach Interrupt |
| 2 | ADC_Change | 1 | 0: Unmask ADC_Change Interrupt 1: Mask ADC_Change Interrupt |
| 3 | Stuck_Key | 1 | 0: Unmask Stuck_Key Interrupt 1: Mask Stuck_Key Interrupt |
| 4 | Stuck_Key_RCV | 1 | 0: Unmask Stuck_Key_RCV Interrupt 1: Mask Stuck_Key_RCV Interrupt |
| 5 | Connect | 1 | 0: Unmask Connect Interrupt 1: Mask Connect Interrupt |
| 6 | OTP_EN | 1 | 0: Unmask OTP_EN Interrupt 1: Mask OTP_EN Interrupt |
| 7 | Reserved | 1 | |

ADC Value

Address: 07h

Reset Value: xxx11111

Type: Read

| BIT NO. | NAME | SIZE (BITS) | DESCRIPTION |
|---------|----------|-------------|------------------------|
| 0-4 | AD value | 5 | ADC value read from ID |
| 53-7 | Reserved | 3 | |

Timing Set 1

Address: 08h

Reset Value: 00000000

Type: Read/Write

| BIT NO. | NAME | SIZE (BITS) | DESCRIPTION |
|---------|----------------|-------------|-------------------------|
| 0-3 | Device Wake Up | 4 | Device wake up duration |
| 4-7 | Reserved | 4 | |

Timing Set 2

Address: 09h

Reset Value: 00000000

Type: Read/Write

| BIT NO. | NAME | SIZE (BITS) | DESCRIPTION |
|---------|----------------|-------------|-----------------------------------|
| 0-3 | Reserved | 4 | |
| 4-7 | Switching wait | 4 | Waiting duration before switching |

Time Table⁽¹⁾

| SETTING VALUE | DEVICE WAKE UP | SWITCHING WAIT |
|---------------|----------------|----------------|
| 0000 | 50 ms | 10 ms |
| 0001 | 100 ms | 30 ms |
| 0010 | 150 ms | 50 ms |
| 0011 | 200 ms | 70 ms |
| 0100 | 300 ms | 90 ms |
| 0101 | 400 ms | 110 ms |
| 0110 | 500 ms | 130 ms |
| 0111 | 600 ms | 150 ms |
| 1000 | 700 ms | 170 ms |
| 1001 | 800 ms | 190 ms |
| 1010 | 900 ms | 210 ms |
| 1011 | 1000 ms | – |
| 1100 | – | – |
| 1101 | – | – |
| 1110 | – | – |
| 1111 | – | – |

(1) Maximum variation of these timing is $\pm 20\%$

Device Type 1

Address: 0Ah

Reset Value: 00000000

Type: Read

| BIT NO. | NAME | SIZE (BITS) | DESCRIPTION |
|---------|--------------|-------------|---|
| 0 | Audio type 1 | 1 | Audio device type 1 |
| 1 | Audio type 2 | 1 | Audio device type 2 |
| 2 | USB | 1 | USB host |
| 3 | UART | 1 | UART |
| 4 | Carkit | 1 | Carkit Charger Type 1 or 2 |
| 5 | CDP | 1 | Charging Downstream Port (USB Host Hub Charger) |
| 6 | DCP | 1 | Dedicated Charging Port |
| 7 | USB OTG | 1 | USB on-the-go device |

Device Type 2

Address: 0Bh

Reset Value:x0000000

Type: Read

| BIT NO. | NAME | SIZE (BITS) | DESCRIPTION |
|---------|--------------|-------------|----------------------|
| 0 | JIG_USB_ON | 1 | Factory mode cable |
| 1 | JIG_USB_OFF | 1 | Factory mode cable |
| 2 | JIG_UART_ON | 1 | Factory mode cable |
| 3 | JIG_UART_OFF | 1 | Factory mode cable |
| 4 | PPD | 1 | Phone-powered device |
| 5 | TTY | 1 | TTY converter |
| 6 | A/V | 1 | A/V cable |
| 7 | Audio type 3 | 1 | Audio device type 3 |

Button 1

Address: 0Ch

Reset Value: 00000000

Type: Read and Clear

| BIT NO. | NAME | SIZE (BITS) | DESCRIPTION |
|---------|----------|-------------|-------------------------|
| 0 | 8 | 1 | Send_End key is pressed |
| 1 | 9 | 1 | Number 1 key is pressed |
| 2 | 10 | 1 | Number 2 key is pressed |
| 3 | 11 | 1 | Number 3 key is pressed |
| 4 | 12 | 1 | Number 4 key is pressed |
| 5 | Error | 1 | Number 5 key is pressed |
| 6 | Unknown | 1 | Number 6 key is pressed |
| 7 | Reserved | 1 | Number 7 key is pressed |

Button 2

Address: 0Dh

Reset Value: x0000000

Type: Read and Clear

| BIT NO. | NAME | SIZE (BITS) | DESCRIPTION |
|---------|----------|-------------|--------------------------|
| 0 | Send_End | 1 | Number 8 key is pressed |
| 1 | 1 | 1 | Number 9 key is pressed |
| 2 | 2 | 1 | Number 10 key is pressed |
| 3 | 3 | 1 | Number 11 key is pressed |
| 4 | 4 | 1 | Number 12 key is pressed |
| 5 | 5 | 1 | Error key is pressed |
| 6 | 6 | 1 | Unknown key is pressed |
| 7 | 7 | 1 | |

Manual S/W 1

Address: 13h

Reset Value: 000000xx

Type: Read/Write

| BIT NO. | NAME | SIZE (BITS) | DESCRIPTION |
|---------|--------------|-------------|---|
| 0-1 | Unused | 2 | |
| 2-4 | D+ Switching | 3 | 000: Open all switch 001: D+ is connected to D+ of USB port 010: Open all switch 011: D+ is connected to RxD of UART |
| 5-7 | D– Switching | 3 | 000: Open all switch 001: D– is connected to D– of USB port 010: Open all switch 011: D– is connected to TxD of UART |

Manual S/W 2

Address: 14h

Reset Value: xxxx00xx

Type: Read/Write

| BIT NO. | NAME | SIZE (BITS) | DESCRIPTION |
|---------|--------|-------------|---|
| 0-1 | Unused | 2 | |
| 2 | JIG | 1 | TSU6111: 0: High Impedance 1: GND |
| 3 | BOOT | 1 | 0: Low 1: High |
| 4-7 | Unused | 4 | |

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| TSU6111RSVR | ACTIVE | UQFN | RSV | 16 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU Call TI | Level-1-260C-UNLIM | -40 to 85 | ZTC | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TSU6111RSVR | UQFN | RSV | 16 | 3000 | 177.8 | 12.4 | 2.0 | 2.8 | 0.7 | 4.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

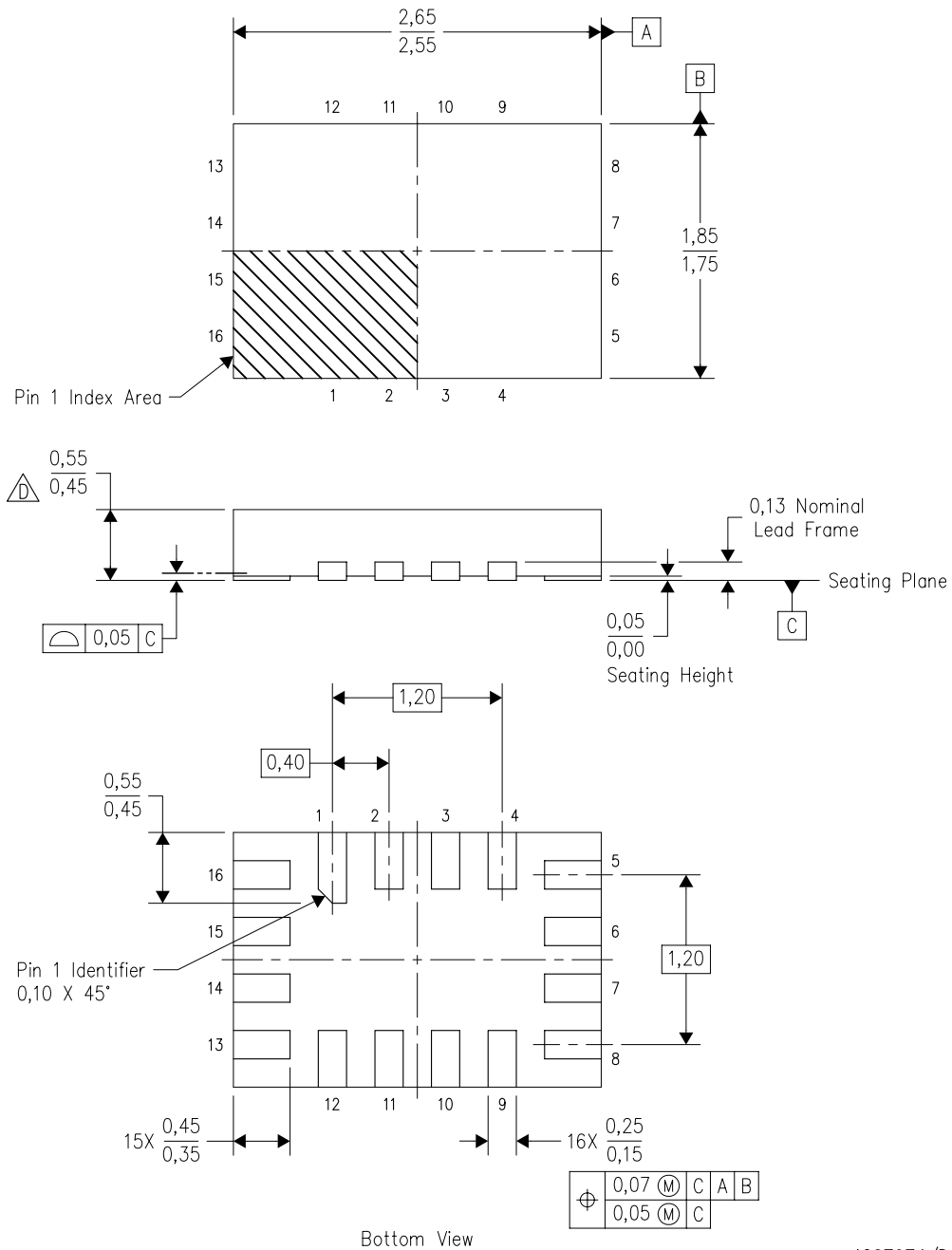


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TSU6111RSVR | UQFN | RSV | 16 | 3000 | 202.0 | 201.0 | 28.0 |

RSV (R-PUQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD

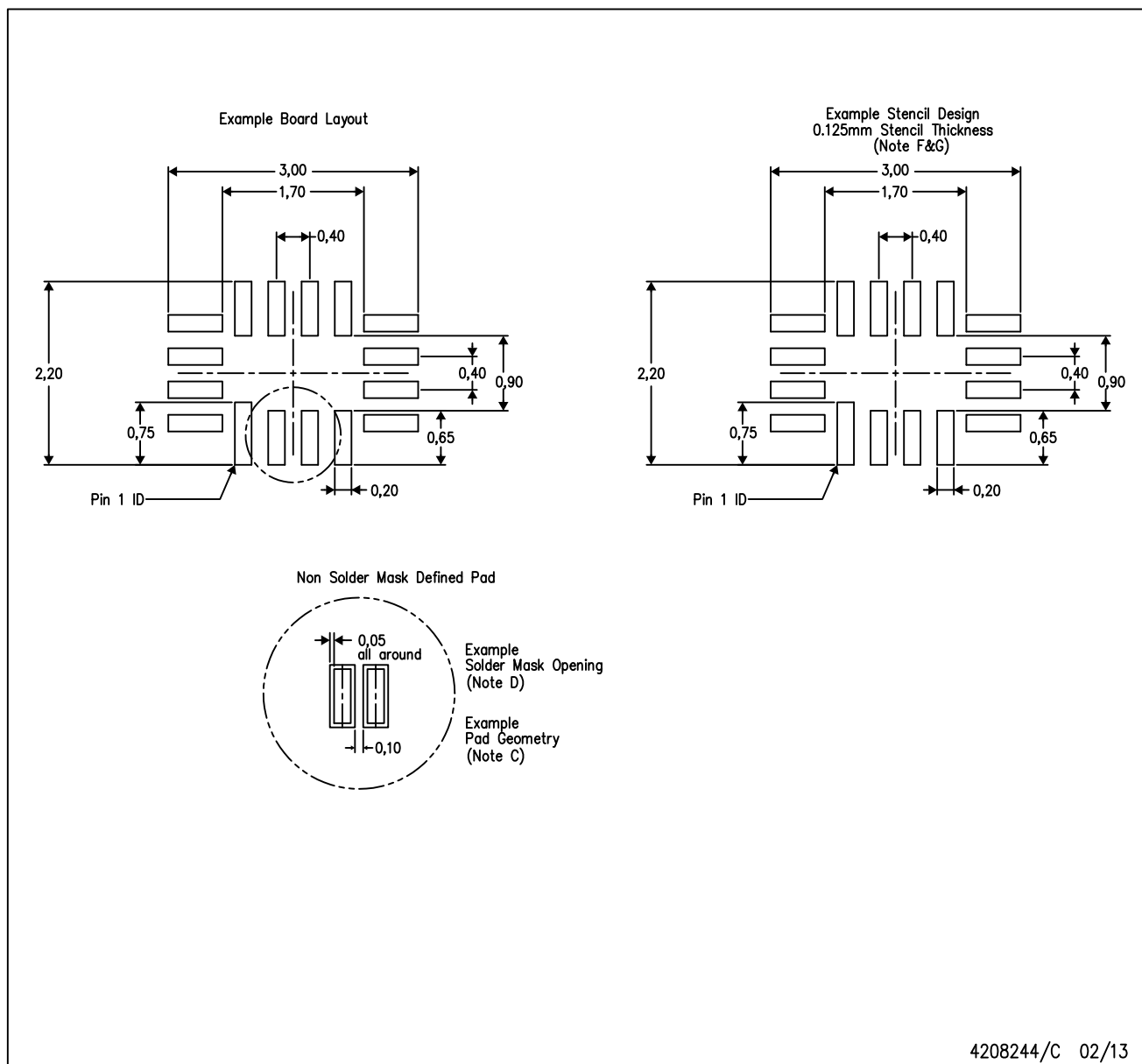


4207974/D 12/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 - This package complies to JEDEC MO-288 variation UFHE, except minimum package thickness.

RSV (R-PUQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
 - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
 - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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