

3-V TO 5.5-V MULTICHANNEL RS-232 LINE DRIVER/RECEIVER WITH ± 15 -kV ESD PROTECTION

Check for Samples: [TRSF3223E](#)

FEATURES

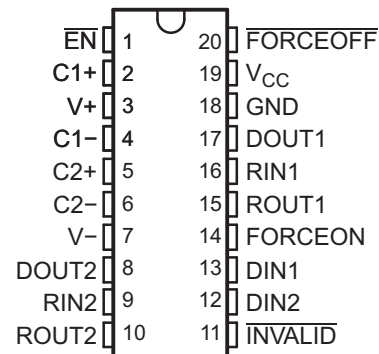
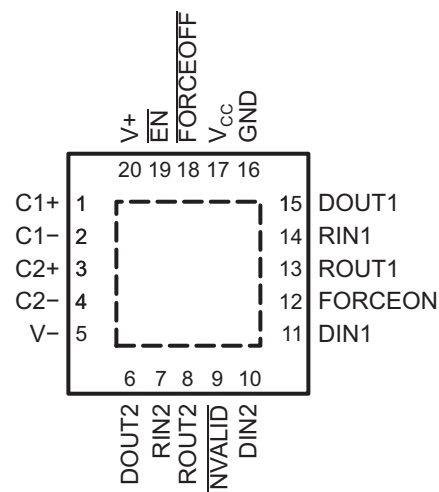
- **ESD Protection for RS-232 Bus Pins**
 - ± 15 -kV Human-Body Model (HBM)
 - ± 8 -kV IEC 61000-4-2, Contact Discharge
 - ± 15 -kV IEC 61000-4-2, Air-Gap Discharge
- **Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU v.28 Standards**
- **Operates With 3-V to 5.5-V V_{CC} Supply**
- **Operates up to 1000 kbit/s**
- **Two Drivers and Two Receivers**
- **Low Standby Current . . . 1 μ A Typ**
- **External Capacitors . . . 4 \times 0.1 μ F**
- **Accepts 5-V Logic Input With 3.3-V Supply**

APPLICATIONS

- **Battery-Powered Systems**
- **PDAs**
- **Notebooks**
- **Laptops**
- **Palmtop PCs**
- **Hand-Held Equipment**

DESCRIPTION/ ORDERING INFORMATION

The TRSF3223E consists of two line drivers, two line receivers, and a dual charge-pump circuit with ± 15 -kV ESD protection pin to pin (serial-port connection pins, including GND). This device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. The TRSF3223E operates at typical data signaling rates up to 1000 kbit/s.

DB, DW, OR PW PACKAGE
(TOP VIEW)

RGW PACKAGE
(TOP VIEW)


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Flexible control options for power management are available when the serial port is inactive. The auto-powerdown feature functions when FORCEON is low and FORCEOFF is high. During this mode of operation, if the device does not sense a valid RS-232 signal, the driver outputs are disabled. If FORCEOFF is set low and EN is high, both drivers and receivers are shut off, and the supply current is reduced to 1 mA. Disconnecting the serial port or turning off the peripheral drivers causes auto-powerdown to occur. Auto-powerdown can be disabled when FORCEON and FORCEOFF are high. With auto-powerdown enabled, the device is automatically activated when a valid signal is applied to any receiver input. The INVALID output is used to notify the user if an RS-232 signal is present at any receiver input. INVALID is high (valid data) if any receiver input voltage is greater than 2.7 V or less than –2.7 V, or has been between –0.3 V and 0.3 V for less than 30 μ s. INVALID is low (invalid data) if the receiver input voltage is between –0.3 V and 0.3 V for more than 30 μ s. Refer to Figure 4 for receiver input levels.

Table 1. ORDERING INFORMATION

| T _A | PACKAGE ^{(1) (2)} | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|----------------------------|--------------|-----------------------|------------------|
| 0°C to 70°C | SOIC – DW | Tube of 25 | TRSF3223ECDW | TRSF3223EC |
| | | Reel of 2000 | TRSF3223ECDWR | |
| | SSOP – DB | Tube of 70 | TRSF3223ECDB | RT23EC |
| | | Reel of 2000 | TRSF3223ECDBR | |
| | TSSOP – PW | Tube of 70 | TRSF3223ECPW | RT23EC |
| | | Reel of 2000 | TRSF3223ECPWR | |
| –40°C to 85°C | SOIC – DW | Tube of 25 | TRSF3223EIDW | TRSF3223EI |
| | | Reel of 2000 | TRSF3223EIDWR | |
| | SSOP – DB | Tube of 70 | TRSF3223EIDB | RT23EI |
| | | Reel of 2000 | TRSF3223EIDBR | |
| | TSSOP – PW | Tube of 70 | TRSF3223EIPW | RT23EI |
| | | Reel of 2000 | TRSF3223EIPWR | |
| | QFN – RGW | Reel of 3000 | TRSF3223EIRGWR | RT23EI |

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

FUNCTION TABLES

Each Driver⁽¹⁾

| INPUTS | | | | OUTPUT DOUT | DRIVER STATUS |
|--------|---------|----------|---------------------------|----------------|--|
| DIN | FORCEON | FORCEOFF | VALID RIN RS-232 LEVEL | | |
| X | X | L | X | Z | Powered off |
| L | H | H | X | H | Normal operation with auto-powerdown disabled |
| H | H | H | X | L | |
| L | L | H | Yes | H | Normal operation with auto-powerdown enabled |
| H | L | H | Yes | L | |
| L | L | H | No | Z | Powered off by auto-powerdown feature |
| H | L | H | No | Z | |

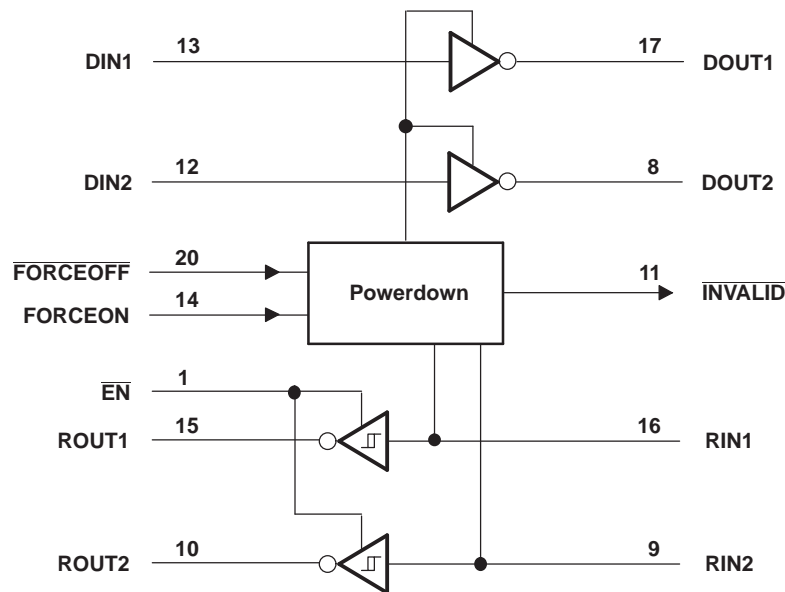
(1) H = high level, L = low level, X = irrelevant, Z = high impedance

Each Receiver⁽¹⁾

| INPUTS | | | OUTPUT ROUT |
|--------|------------------------|---------------------------|----------------|
| RIN | $\overline{\text{EN}}$ | VALID RIN RS-232 LEVEL | |
| L | L | X | H |
| H | L | X | L |
| X | H | X | Z |
| Open | L | No | H |

- (1) H = high level, L = low level, X = irrelevant,
Z = high impedance (off),
Open = input disconnected or connected driver off

LOGIC DIAGRAM (POSITIVE LOGIC)



Pin numbers are for the DB, DW, and PW packages.

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|------------------|---|---|-------|-----------------------|------|
| V _{CC} | Supply voltage range | | −0.3 | 6 | V |
| V+ | Positive-output supply voltage range ⁽²⁾ | | −0.3 | 7 | V |
| V− | Negative-output supply voltage range ⁽²⁾ | | 0.3 | −7 | V |
| V+ − V− | Supply voltage difference ⁽²⁾ | | | 13 | V |
| V _I | Input voltage range | Driver ($\overline{\text{FORCEOFF}}$, FORCEON, $\overline{\text{EN}}$) | −0.3 | 6 | V |
| | | Receiver | −25 | 25 | |
| V _O | Output voltage range | Driver | −13.2 | 13.2 | V |
| | | Receiver ($\overline{\text{INVALID}}$) | −0.3 | V _{CC} + 0.3 | |
| θ _{JA} | Package thermal impedance ⁽³⁾ ⁽⁴⁾ | DB package | | 70 | °C/W |
| | | DW package | | 58 | |
| | | PW package | | 83 | |
| T _J | Operating virtual junction temperature | | | 150 | °C |
| T _{stg} | Storage temperature range | | −65 | 150 | °C |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network GND.
- (3) Maximum power dissipation is a function of T_J(max), θ_{JA} , and T_A. The maximum allowable power dissipation at any allowable ambient temperature is P_D = (T_J(max) – T_A)/ θ_{JA} . Operating at the absolute maximum T_J of 150°C can affect reliability.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

See Figure 6

| | | | MIN | NOM | MAX | UNIT |
|-----------------|---|--|-------------------------|-----|-----|------|
| Supply voltage | | V _{CC} = 3.3 V | 3 | 3.3 | 3.6 | V |
| | | V _{CC} = 5 V | 4.5 | 5 | 5.5 | |
| V _{IH} | Driver and control high-level input voltage | DIN, $\overline{\text{EN}}$, $\overline{\text{FORCEOFF}}$, FORCEON | V _{CC} = 3.3 V | | 2 | V |
| | | | V _{CC} = 5 V | | 2.4 | |
| V _{IL} | Driver and control low-level input voltage | DIN, $\overline{\text{EN}}$, $\overline{\text{FORCEOFF}}$, FORCEON | | | 0.8 | V |
| V _I | Driver and control input voltage | DIN, $\overline{\text{EN}}$, $\overline{\text{FORCEOFF}}$, FORCEON | | | 0 | V |
| | Receiver input voltage | | | | 5.5 | |
| T _A | Operating free-air temperature | TRSF3223EC | | | 0 | °C |
| | | TRSF3223EI | | | –40 | |
| | | | | | 70 | |
| | | | | | 85 | |

- (1) Test conditions are C1–C4 = 0.1 μ F at V_{CC} = 3.3 V \pm 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at V_{CC} = 5 V \pm 0.5 V.

Electrical Characteristics⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP ⁽²⁾ | MAX | UNIT |
|-----------------|-----------------------|-------------------------|---|-----|--------------------|-----|------|
| I _I | Input leakage current | EN, FORCEOFF, FORCEON | | | ±0.01 | ±1 | μA |
| I _{CC} | Supply current | Auto-powerdown disabled | V _{CC} = 3.3 V or 5 V, T _A = 25°C, No load, FORCEOFF and FORCEON at V _{CC} | | 0.3 | 1 | mA |
| | | Powered off | No load, FORCEOFF at GND | | 1 | 10 | μA |
| | | Auto-powerdown enabled | No load, FORCEOFF at V _{CC} , FORCEON at GND, All RIN are open or grounded | | 1 | 10 | |

- (1) Test conditions are C1–C4 = 0.1 μ F at V_{CC} = 3.3 V \pm 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at V_{CC} = 5 V \pm 0.5 V.
- (2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

DRIVER SECTION

Electrical Characteristics⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5)

| PARAMETER | TEST CONDITIONS | MIN | TYP ⁽²⁾ | MAX | UNIT |
|---|--|-----|--------------------|-----|------|
| V _{OH} High-level output voltage | DOUT at R _L = 3 kΩ to GND | 5 | 5.4 | | V |
| V _{OL} Low-level output voltage | DOUT at R _L = 3 kΩ to GND | –5 | –5.4 | | V |
| I _{IH} High-level input current | V _I = V _{CC} | | ±0.01 | ±1 | μA |
| I _{IL} Low-level input current | V _I at GND | | ±0.01 | ±1 | μA |
| I _{OS} Short-circuit output current ⁽³⁾ | V _{CC} = 3.6 V, V _O = 0 V | | ±35 | ±60 | mA |
| | V _{CC} = 5.5 V, V _O = 0 V | | | | |
| r _o Output resistance | V _{CC} , V ₊ , and V _– = 0 V, V _O = ±2 V | 300 | 10M | | Ω |
| I _{OZ} Output leakage current | FORCEOFF = GND, V _{CC} = 3 V to 3.6 V, V _O = ±12 V | | | ±25 | μA |
| | FORCEOFF = GND, V _{CC} = 4.5 V to 5.5 V, V _O = ±12 V | | | ±25 | |

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(3) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

Switching Characteristics⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5)

| PARAMETER | TEST CONDITIONS | MIN | TYP ⁽²⁾ | MAX | UNIT |
|--|---|--|--------------------|-----|--------|
| Maximum data rate (see Figure 1) | R _L = 3 kΩ, One DOUT switching | C _L = 1000 pF | 250 | | kbit/s |
| | | C _L = 250 pF, V _{CC} = 3 V to 4.5 V | 1000 | | |
| | | C _L = 1000 pF, V _{CC} = 4.5 V to 5.5 V | 1000 | | |
| t _{sk(p)} Pulse skew ⁽³⁾ | C _L = 150 pF to 2500 pF, R _L = 3 kΩ to 7 kΩ, See Figure 2 | | 300 | | ns |
| SR(tr) Slew rate, transition region (see Figure 1) | R _L = 7 kΩ, C _L = 150 pF to 1000 pF | | 8 | 90 | V/μs |
| | | C _L = 1000 pF | 12 | 60 | |
| | R _L = 3 kΩ, C _L = 150 pF to 250 pF | | 24 | 150 | |

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(3) Pulse skew is defined as |t_{PLH} – t_{PHL}| of each channel of the same device.

RECEIVER SECTION

Electrical Characteristics⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 6)

| PARAMETER | TEST CONDITIONS | MIN | TYP ⁽²⁾ | MAX | UNIT |
|--|--|-----------------------|-----------------------|-----|------|
| V _{OH} High-level output voltage | I _{OH} = –1 mA | V _{CC} – 0.6 | V _{CC} – 0.1 | | V |
| V _{OL} Low-level output voltage | I _{OL} = 1.6 mA | | | 0.4 | V |
| V _{IT+} Positive-going input threshold voltage | V _{CC} = 3.3 V | | 1.6 | 2.4 | V |
| | V _{CC} = 5 V | | 1.9 | 2.4 | |
| V _{IT–} Negative-going input threshold voltage | V _{CC} = 3.3 V | 0.6 | 1.1 | | V |
| | V _{CC} = 5 V | 0.6 | 1.4 | | |
| V _{hys} Input hysteresis (V _{IT+} – V _{IT–}) | | | 0.5 | | V |
| I _{OZ} Output leakage current | $\overline{\text{EN}} = V_{\text{CC}}$ | | ±0.05 | | µA |
| r _i Input resistance | V _I = ±3 V to ±25 V | 3 | 5 | | kΩ |

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

Switching Characteristics⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | TYP ⁽²⁾ | UNIT |
|--|--|--------------------|------|
| t _{PLH} Propagation delay time, low- to high-level output | C _L = 150 pF, See Figure 3 | 150 | ns |
| t _{PHL} Propagation delay time, high- to low-level output | C _L = 150 pF, See Figure 3 | 150 | ns |
| t _{en} Output enable time | C _L = 150 pF, R _L = 3 kΩ, See Figure 4 | 200 | ns |
| t _{dis} Output disable time | C _L = 150 pF, R _L = 3 kΩ, See Figure 4 | 200 | ns |
| t _{sk(p)} Pulse skew ⁽³⁾ | See Figure 3 | 50 | ns |

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(3) Pulse skew is defined as |t_{PLH} – t_{PHL}| of each channel of the same device.

AUTO-POWERDOWN SECTION

Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5)

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|------------------|---|---|----------------|-----|------|
| $V_{T+(valid)}$ | Receiver input threshold for $\overline{INVALID}$ high-level output voltage | FORCEON = GND, $\overline{FORCEOFF} = V_{CC}$ | | 2.7 | V |
| $V_{T-(valid)}$ | Receiver input threshold for $\overline{INVALID}$ high-level output voltage | FORCEON = GND, $\overline{FORCEOFF} = V_{CC}$ | –2.7 | | V |
| $V_{T(invalid)}$ | Receiver input threshold for $\overline{INVALID}$ low-level output voltage | FORCEON = GND, $\overline{FORCEOFF} = V_{CC}$ | –0.3 | 0.3 | V |
| V_{OH} | $\overline{INVALID}$ high-level output voltage | $I_{OH} = 1\text{ mA}$, $\overline{FORCEOFF} = V_{CC}$ FORCEON = GND, | $V_{CC} - 0.6$ | | V |
| V_{OL} | $\overline{INVALID}$ low-level output voltage | $I_{OL} = 1.6\text{ mA}$, $\overline{FORCEOFF} = V_{CC}$ FORCEON = GND, | | 0.4 | V |

Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5)

| PARAMETER | | TYP ⁽¹⁾ | UNIT |
|---------------|---|--------------------|------|
| t_{valid} | Propagation delay time, low- to high-level output | 1 | μs |
| $t_{invalid}$ | Propagation delay time, high- to low-level output | 30 | μs |
| t_{en} | Supply enable time | 100 | μs |

(1) All typical values are at $V_{CC} = 3.3\text{ V}$ or $V_{CC} = 5\text{ V}$, and $T_A = 25^\circ\text{C}$.

PARAMETER MEASUREMENT INFORMATION

- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

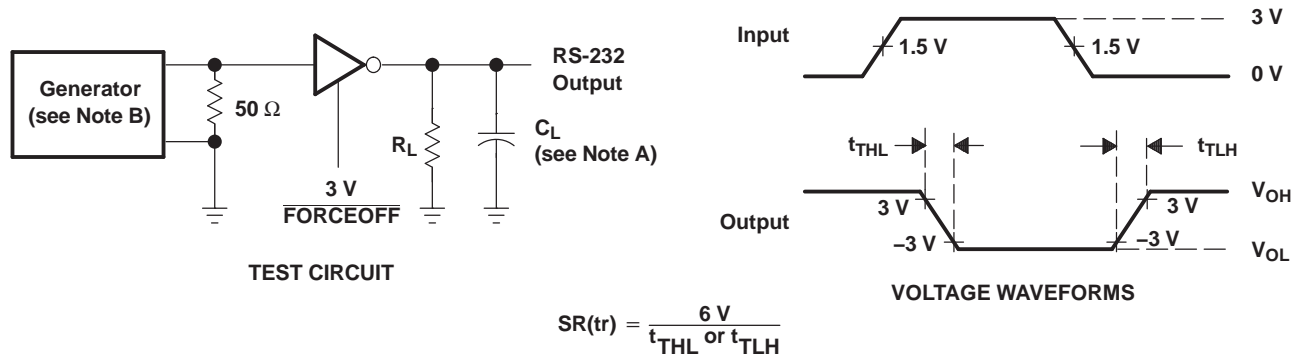


Figure 1. Driver Slew Rate

- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

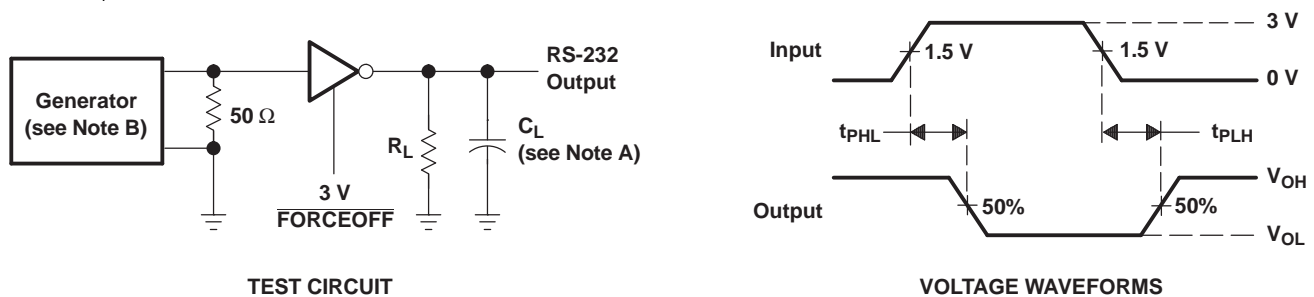


Figure 2. Driver Pulse Skew

- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

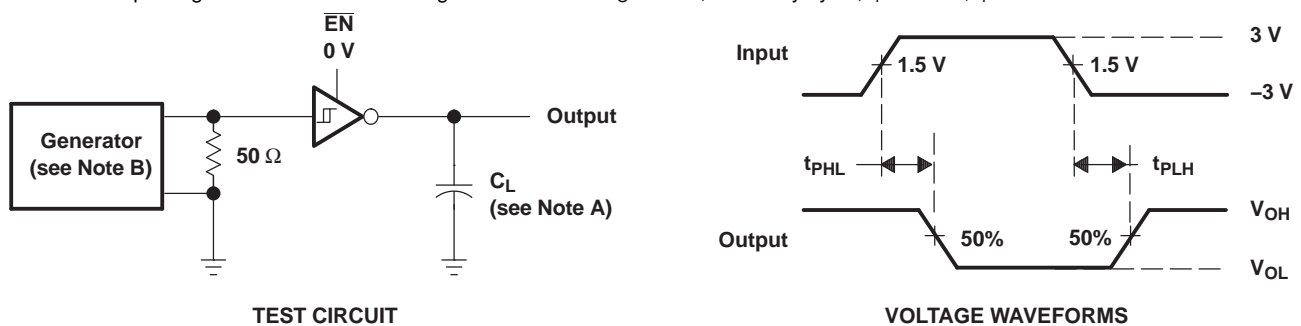


Figure 3. Receiver Propagation Delay Times

- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

PARAMETER MEASUREMENT INFORMATION (continued)

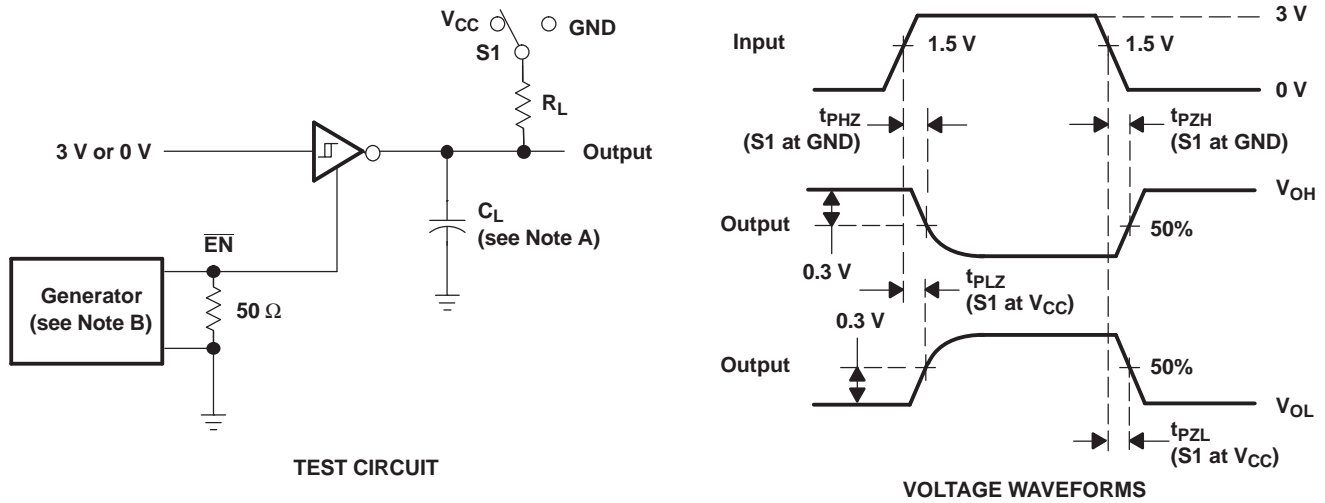
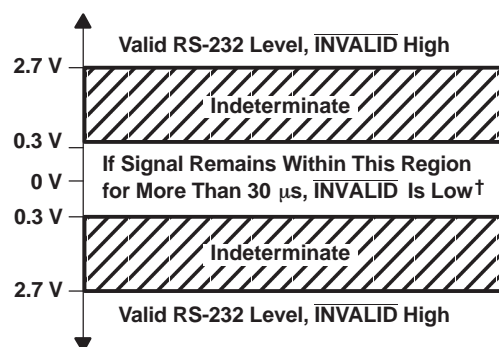
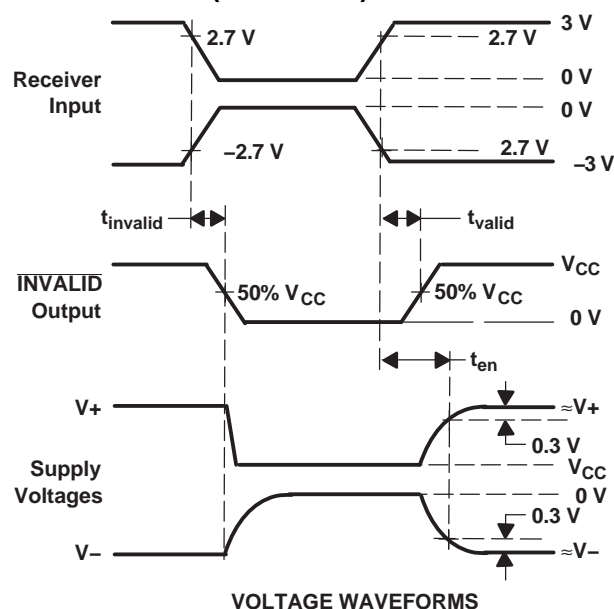
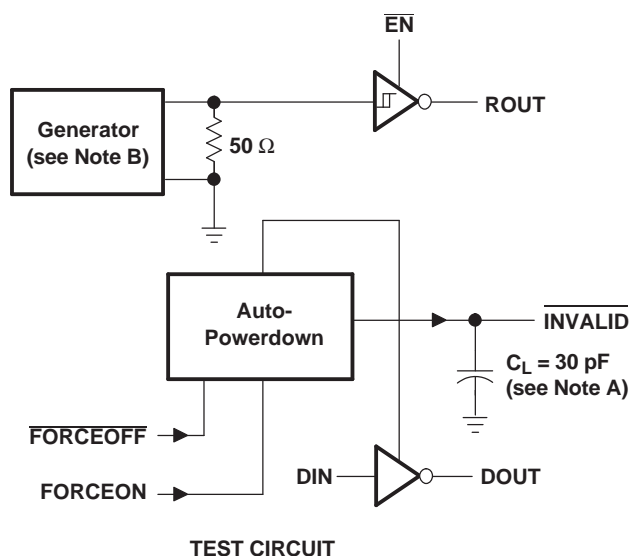


Figure 4. Receiver Enable and Disable Times

- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

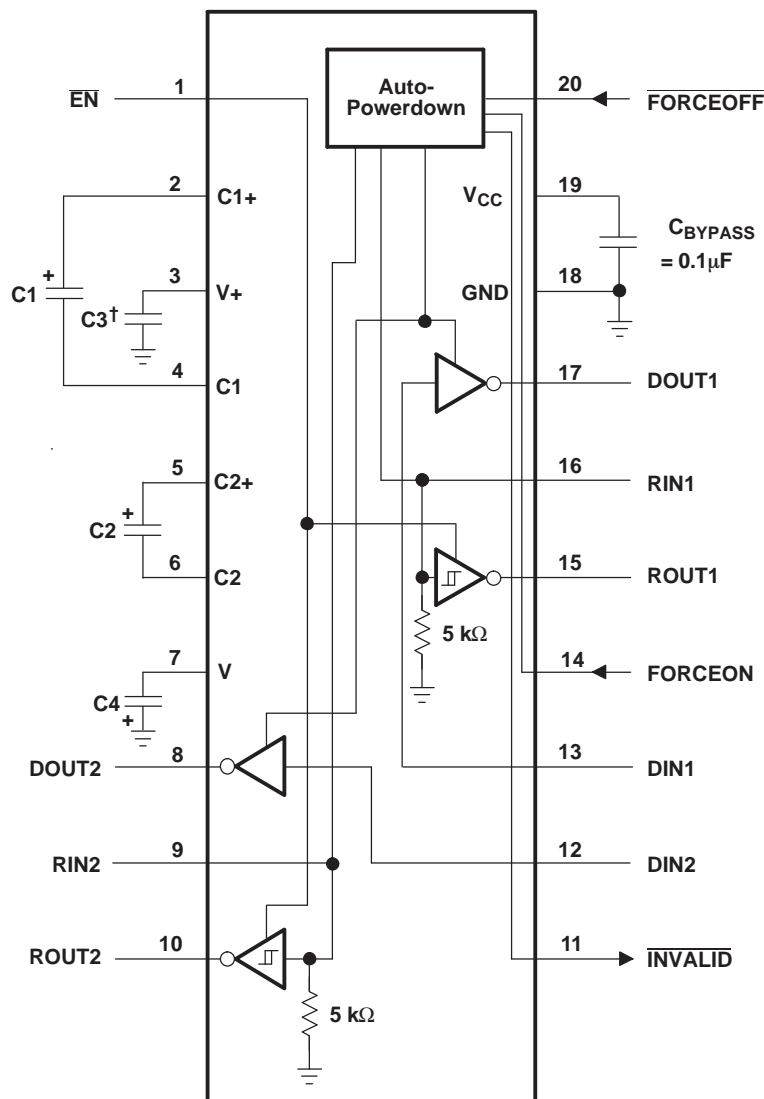
PARAMETER MEASUREMENT INFORMATION (continued)



† Auto-powerdown disables drivers and reduces supply current to 1 μ A

Figure 5. $\overline{\text{INVALID}}$ Propagation Delay Times and Supply Enabling Time

APPLICATION INFORMATION



† C3 can be connected to V_{CC} or GND.

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

V_{CC} vs CAPACITOR VALUES

| V _{CC} | C1 | C2, C3, and C4 |
|-----------------|----------|----------------|
| 3.3 V ± 0.3 V | 0.1 μF | 0.1 μF |
| 5 V ± 0.5 V | 0.047 μF | 0.33 μF |
| 3 V to 5.5 V | 0.1 μF | 0.47 μF |

Figure 6. Typical Operating Circuit and Capacitor Values

REVISION HISTORY

| Changes from Original (August 2007) to Revision A | Page |
|---|-------------------|
| • Added RGW package to datasheet. | 1 |
| • Deleted RHL package from datasheet. | 1 |

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| TRSF3223ECDBR | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | RT23EC | Samples |
| TRSF3223ECDBRG4 | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | RT23EC | Samples |
| TRSF3223ECPW | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | RT23EC | Samples |
| TRSF3223ECPWG4 | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | RT23EC | Samples |
| TRSF3223ECPWR | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | RT23EC | Samples |
| TRSF3223ECPWRG4 | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | RT23EC | Samples |
| TRSF3223EIDBR | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | RT23EI | Samples |
| TRSF3223EIDBRG4 | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | RT23EI | Samples |
| TRSF3223EIDWR | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TRSF3223EI | Samples |
| TRSF3223EIDWRG4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TRSF3223EI | Samples |
| TRSF3223EIPW | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | RT23EI | Samples |
| TRSF3223EIPWG4 | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | RT23EI | Samples |
| TRSF3223EIPWR | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | RT23EI | Samples |
| TRSF3223EIPWRG4 | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | RT23EI | Samples |
| TRSF3223EIRGWR | ACTIVE | VQFN | RGW | 20 | 3000 | Pb-Free (RoHS) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | RT23EI | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TRSF3223ECDBR | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |
| TRSF3223ECPWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| TRSF3223EIDBR | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |
| TRSF3223EIDWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| TRSF3223EIPWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| TRSF3223EIRGWR | VQFN | RGW | 20 | 3000 | 330.0 | 12.4 | 5.3 | 5.3 | 1.5 | 8.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS

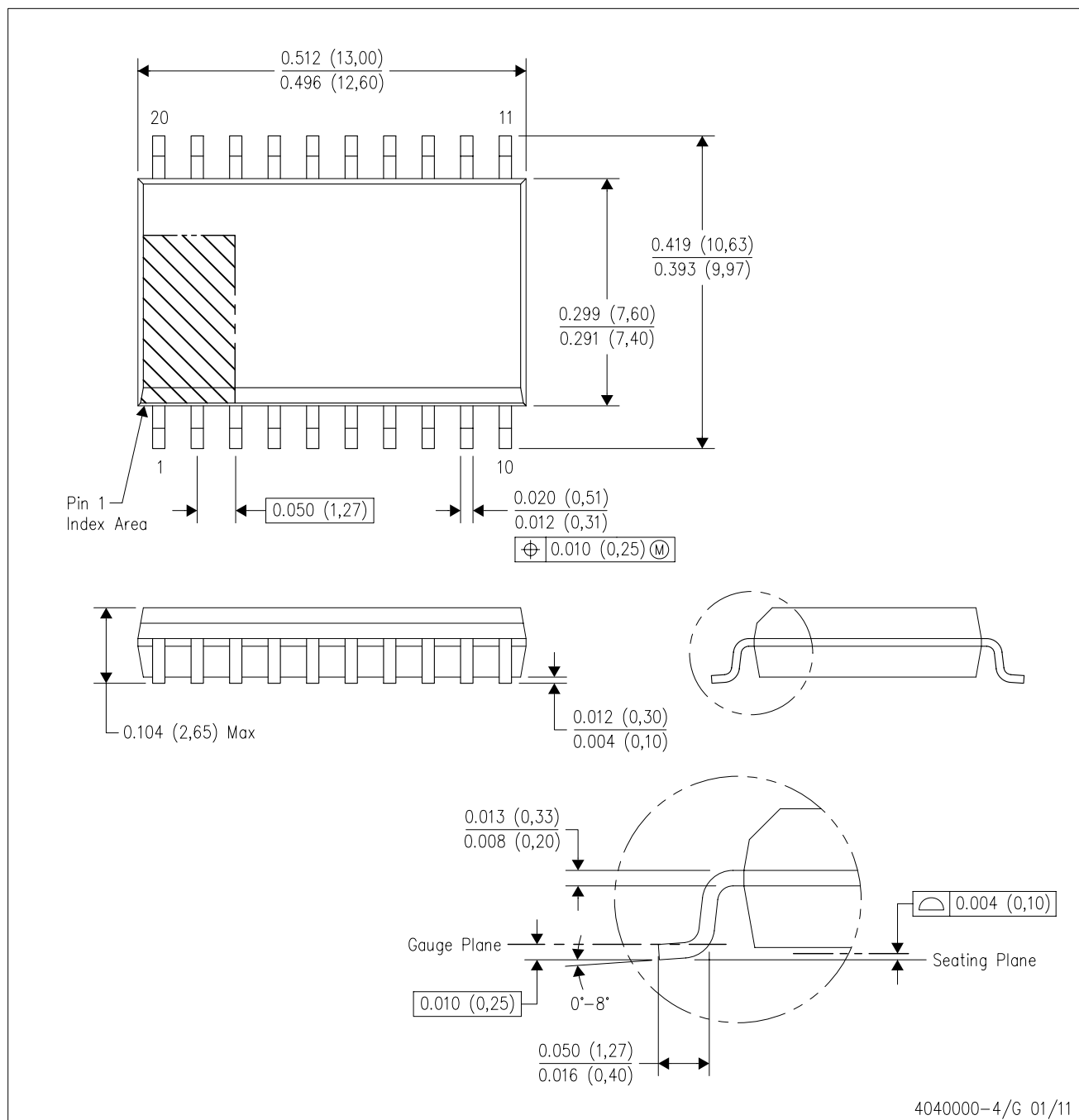


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TRSF3223ECDBR | SSOP | DB | 20 | 2000 | 367.0 | 367.0 | 38.0 |
| TRSF3223ECPWR | TSSOP | PW | 20 | 2000 | 367.0 | 367.0 | 38.0 |
| TRSF3223EIDBR | SSOP | DB | 20 | 2000 | 367.0 | 367.0 | 38.0 |
| TRSF3223EIDWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| TRSF3223EIPWR | TSSOP | PW | 20 | 2000 | 367.0 | 367.0 | 38.0 |
| TRSF3223EIRGWR | VQFN | RGW | 20 | 3000 | 367.0 | 367.0 | 35.0 |

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013 variation AC.

DW (R-PDSO-G20)

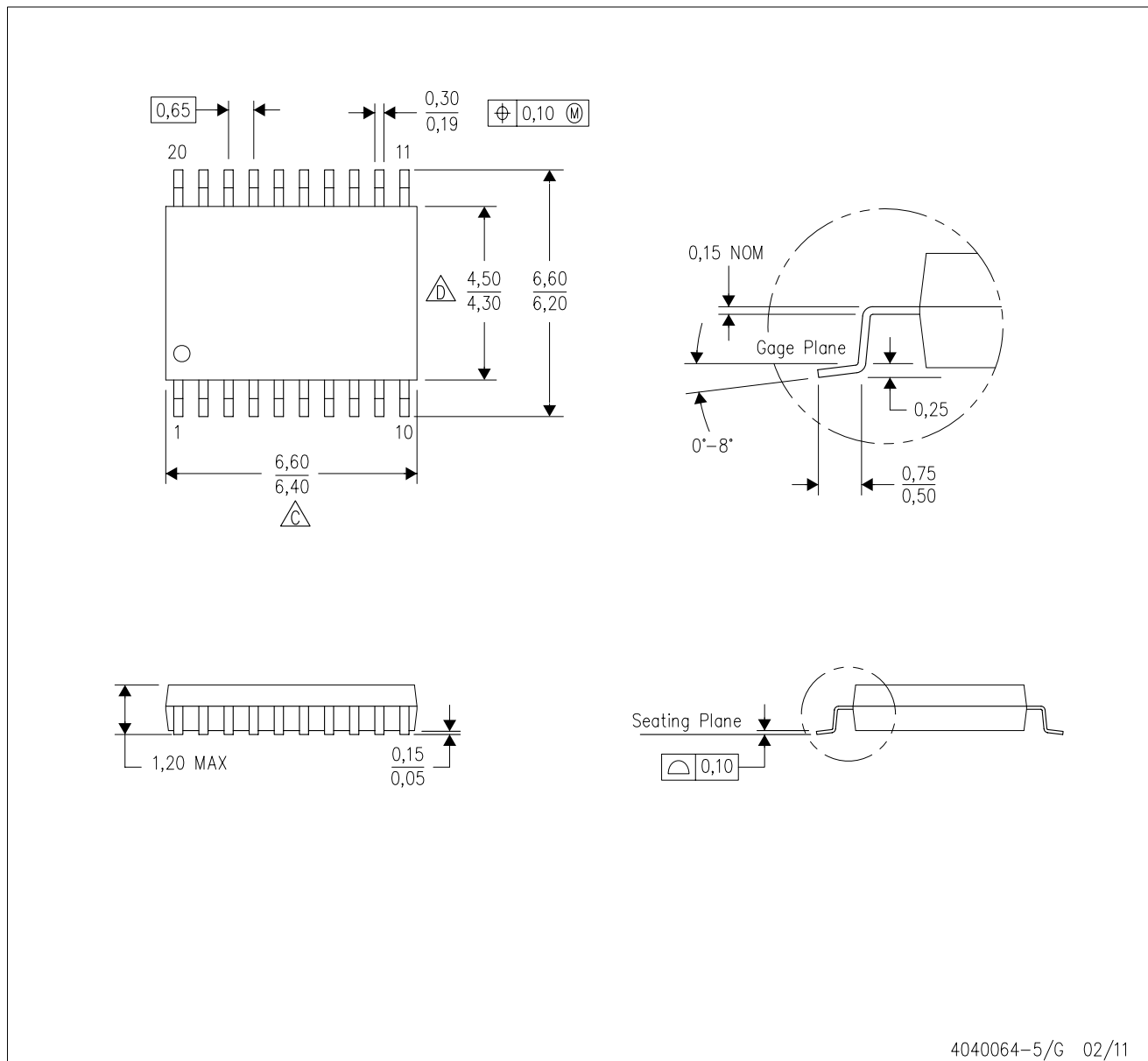
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

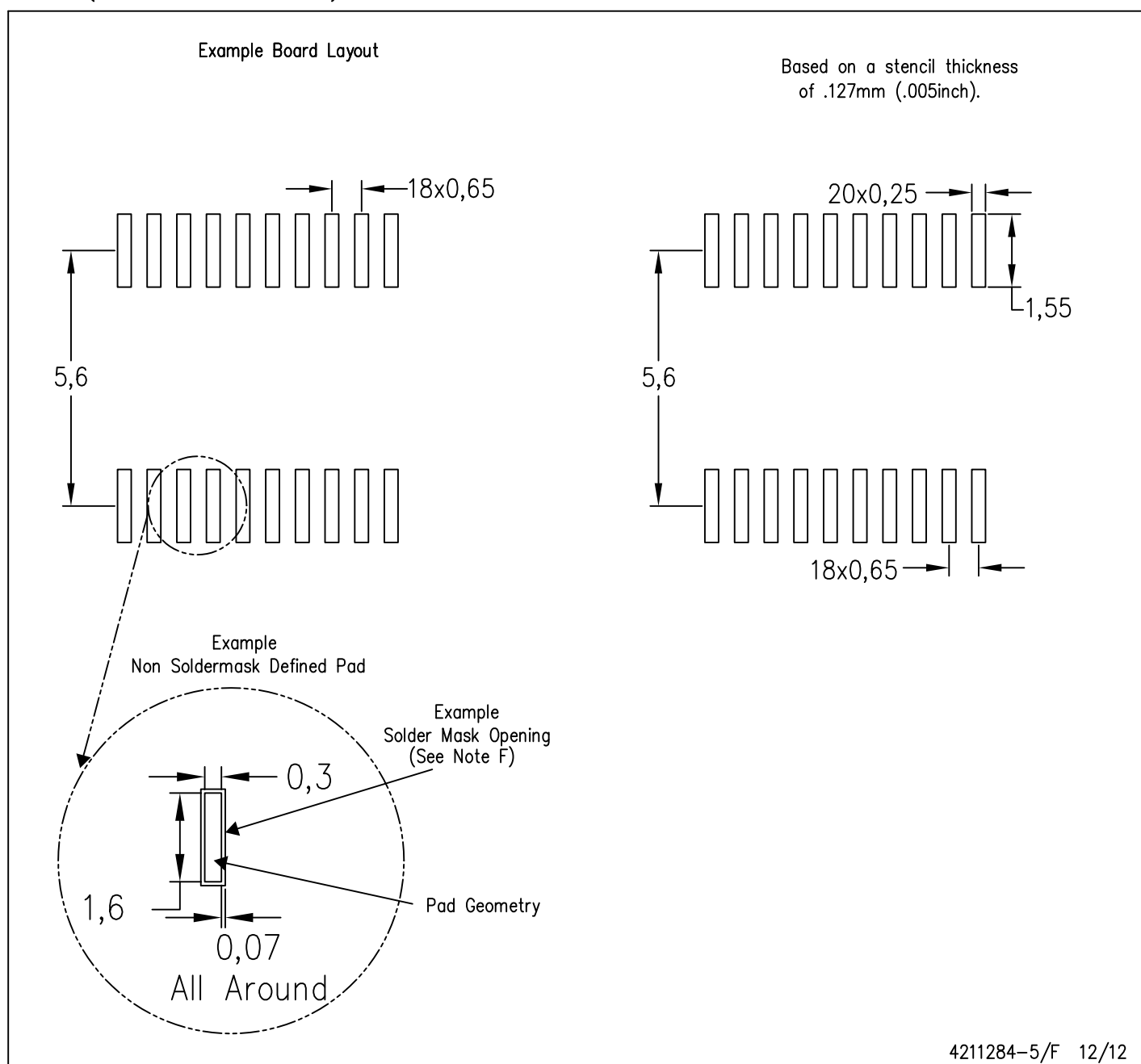
PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



4040064-5/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

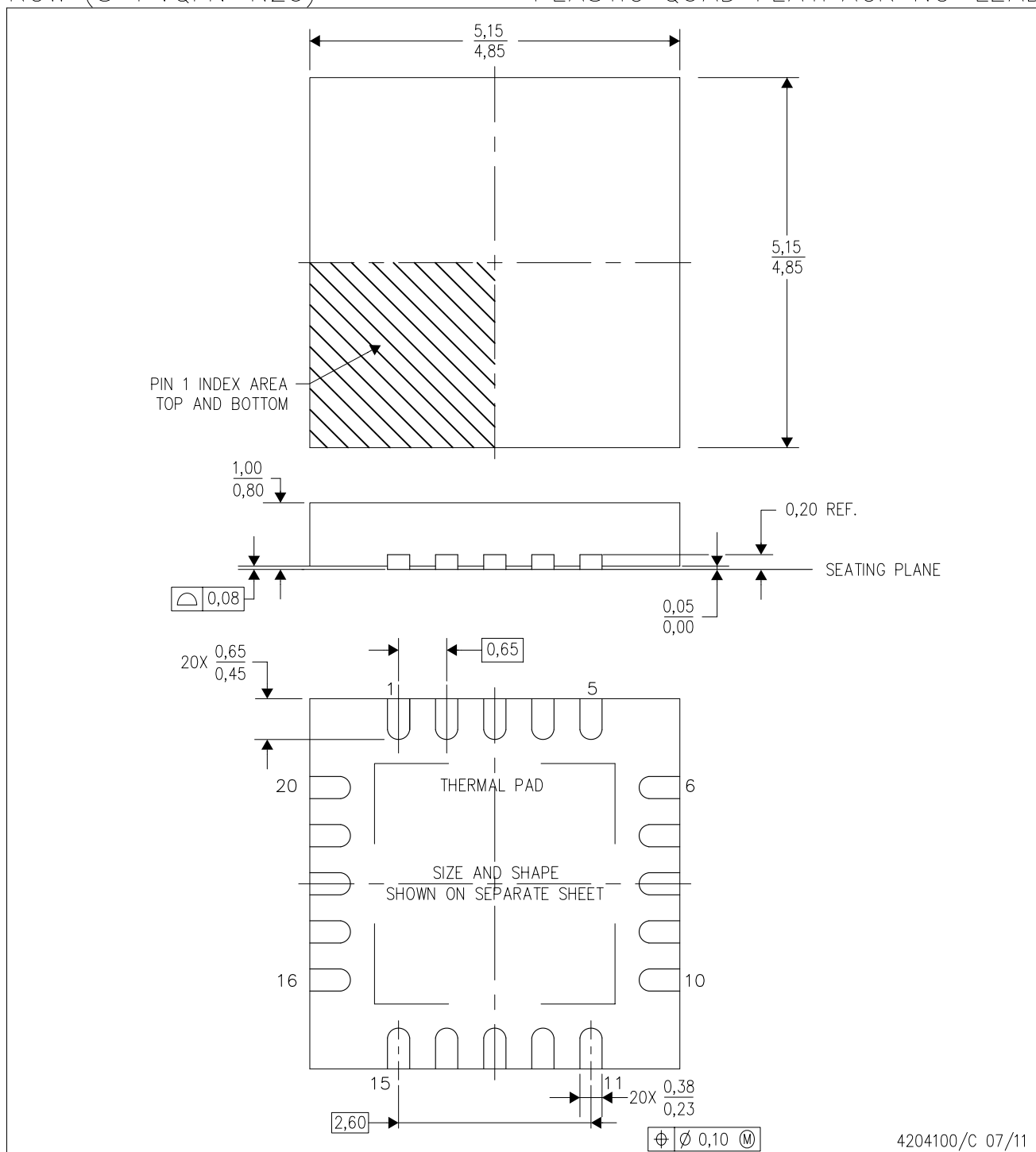


NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RGW (S-PVQFN-N20)

PLASTIC QUAD FLATPACK NO-LEAD



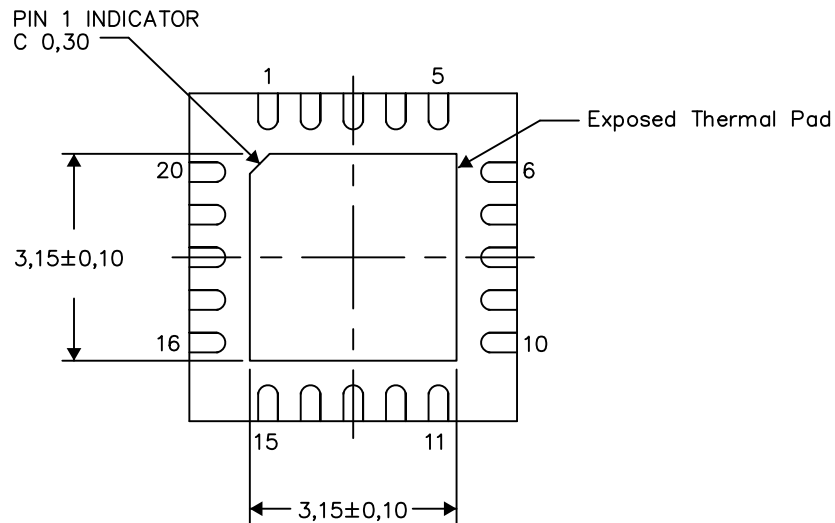
- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
 - This drawing is subject to change without notice.
 - Quad Flat pack, No-leads (QFN) package configuration
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Falls within JEDEC MO-220.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

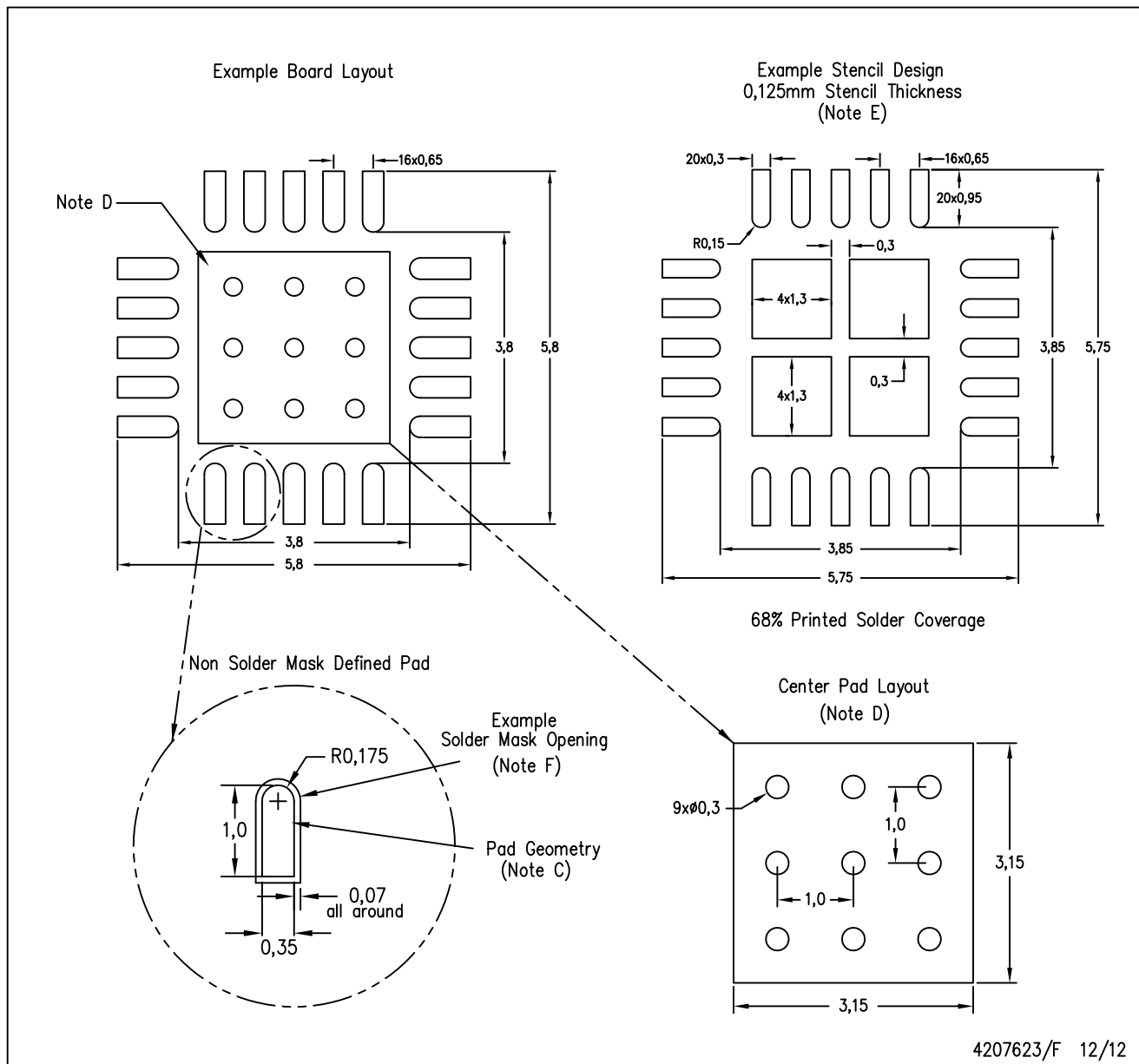
Exposed Thermal Pad Dimensions

4206352-2/K 12/12

NOTE: All linear dimensions are in millimeters

RGW (S-PVQFN-N20)

PLASTIC QUAD FLATPACK NO-LEAD

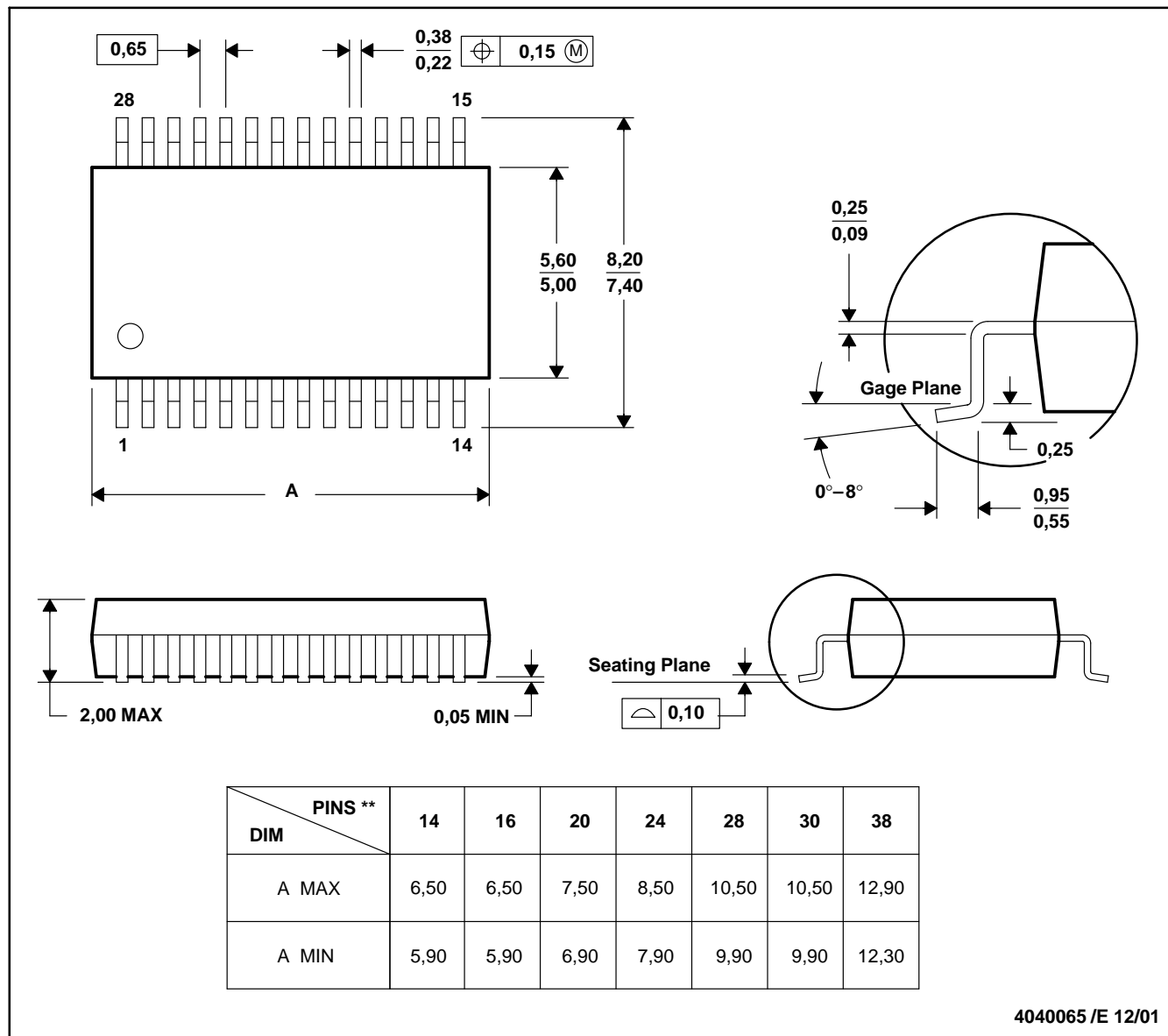


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for solder mask tolerances.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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