

## 3-V TO 5.5-V MULTICHANNEL RS-232 1-Mbit/s LINE DRIVER/RECEIVER

Check for Samples: [TRS3237E](#)

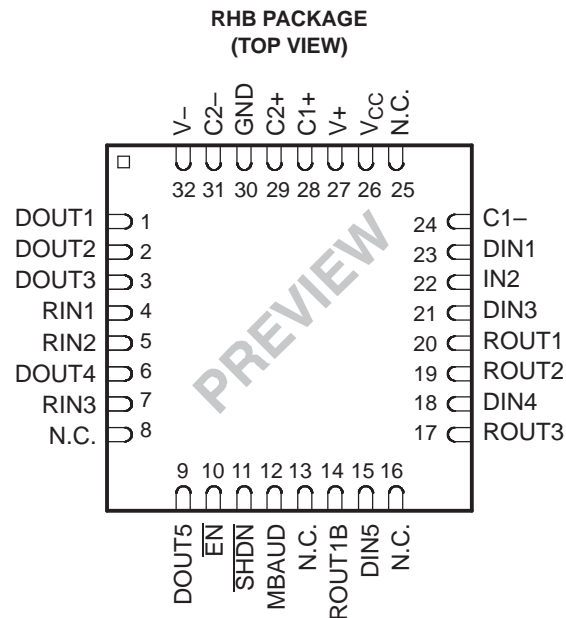
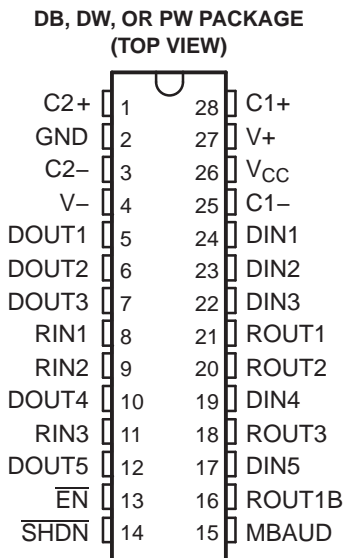
### FEATURES

- Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU v.28 Standards
- Operates With 3-V to 5.5-V  $V_{CC}$  Supply
- Operates From 250 kbits/s to 1 Mbit/s
- Low Standby Current . . . 1  $\mu$ A Typical
- External Capacitors . . . 4  $\times$  0.1  $\mu$ F
- Accepts 5-V Logic Input With 3.3-V Supply
- Designed to Be Interchangeable With Industry Standard '3237E Devices
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II

- ESD Protection for RS-232 I/O Pins
  - $\pm 15$  kV – Human-Body Model (HBM)
  - $\pm 8$  kV – IEC61000-4-2, Contact Discharge
  - $\pm 15$  kV – IEC61000-4-2, Air-Gap Discharge

### APPLICATIONS

- Battery-Powered, Hand-Held, and Portable Equipment
- PDAs and Palmtop PCs
- Notebooks, Sub-Notebooks, and Laptops
- Digital Cameras
- Mobile Phones and Wireless Devices



N.C.— Not internally connected

### DESCRIPTION/ORDERING INFORMATION

The TRS3237E consists of five line drivers, three line receivers, and a dual charge-pump circuit with  $\pm 15$ -kV ESD protection pin to pin (serial-port connection pins, including GND). The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. This device operates at data signaling rates of 250 kbit/s in normal operating mode (MBAUD = GND) and 1Mbit/s when MBAUD =  $V_{CC}$ . The driver output slew rate is a maximum of 30 V/ $\mu$ s.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

The TRS3237E transmitters are disabled and the outputs are forced into high-impedance state when the device is in shutdown mode ( $\overline{\text{SHDN}} = \text{GND}$ ) and the supply current falls to less than 1  $\mu\text{A}$ . Also, during shutdown, the onboard charge pump is disabled;  $V_+$  is lowered to  $V_{\text{CC}}$ , and  $V_-$  is raised toward GND. Receiver outputs also can be placed in the high-impedance state by setting enable ( $\overline{\text{EN}}$ ) high. ROUT1B remains active all the time, regardless of the EN and SHDN condition.

The TRS3237EC is characterized for operation from 0°C to 70°C. The TRS3237EI is characterized for operation from –40°C to 85°C.

**Table 1. ORDERING INFORMATION<sup>(1)</sup>**

$T_A$	PACKAGE <sup>(2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	SSOP – DB	Reel of 2000	TRS3237ECDBR	TRS3237EC
	SOIC – DW	Reel of 2000	TRS3237ECDWR	TRS3237EC
	TSSOP – PW	Reel of 2000	TRS3237ECPWR	RS37EC
	QFN – RHB	Reel of 2000	TRS3237ECRHBR	PREVIEW
–40°C to 85°C	SSOP – DB	Reel of 2000	TRS3237EIDBR	TRS3237EI
	SOIC – DW	Reel of 2000	TRS3237EIDWR	TRS3237EI
	TSSOP – PW	Reel of 2000	TRS3237EIPWR	RS37EI
	QFN – RHB	Reel of 2000	TRS3237EIRHBR	PREVIEW

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

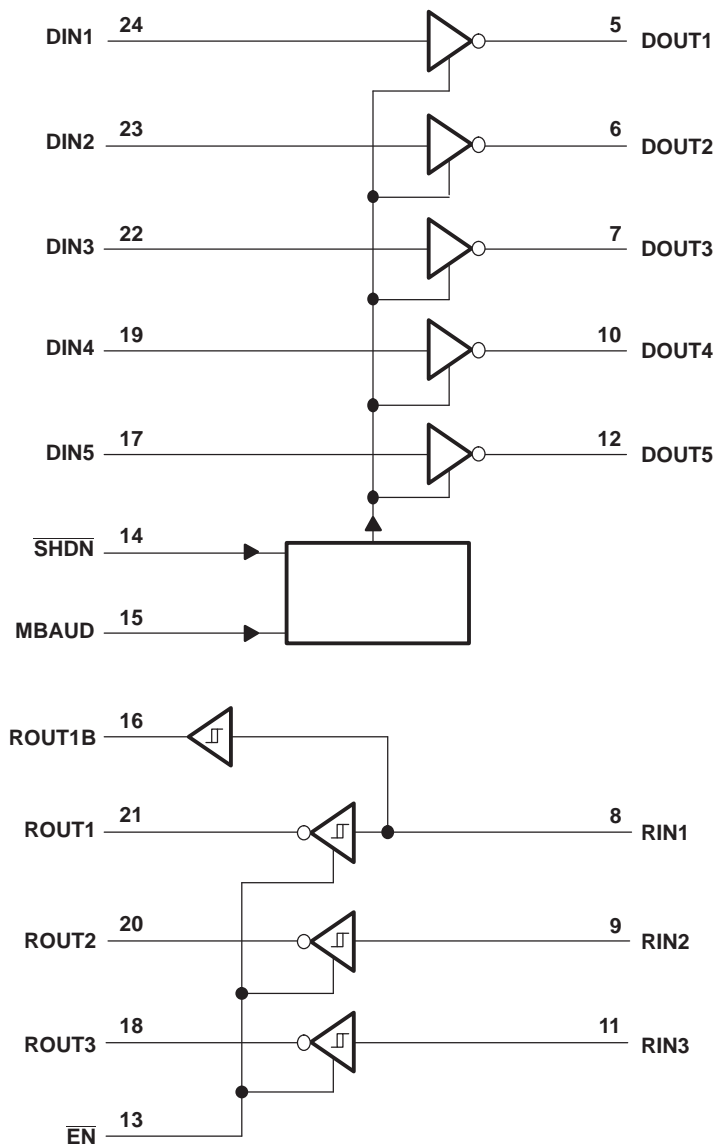
(2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

**Table 2. FUNCTION TABLE**

INPUTS		OUTPUTS		
$\overline{\text{SHDN}}$	$\overline{\text{EN}}$	DOUT	ROUT	ROUT1B
0	0	Z <sup>(1)</sup>	Active	Active
0	1	Z <sup>(1)</sup>	Z <sup>(1)</sup>	Active
1	0	Active	Active	Active
1	1	Active	Z <sup>(1)</sup>	Active

(1) Z = high impedance (off)

**LOGIC DIAGRAM (POSITIVE LOGIC)**



## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range <sup>(2)</sup>		–0.3	6	V
V <sub>+</sub>	Positive-output supply voltage range <sup>(2)</sup>		–0.3	7	V
V <sub>–</sub>	Negative-output supply voltage range <sup>(2)</sup>		0.3	–7	V
V <sub>+</sub> – V <sub>–</sub>	Supply voltage difference <sup>(2)</sup>			13	V
V <sub>I</sub>	Input voltage range	Driver ( $\overline{\text{SHDN}}$ , MBAUD, $\overline{\text{EN}}$ )	–0.3	6	V
		Receiver	–25	25	
V <sub>O</sub>	Output voltage range	Driver	–13.2	13.2	V
		Receiver	–0.3	V <sub>CC</sub> + 0.3	
	Short-circuit duration	DOUT to GND		Unlimited	
θ <sub>JA</sub>	Package thermal impedance <sup>(3)</sup>			62	°C/W
T <sub>stg</sub>	Storage temperature range		–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network GND.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

## RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>

See [Figure 5](#)

			MIN	NOM	MAX	UNIT
Supply voltage		V <sub>CC</sub> = 3.3 V	3	3.3	3.6	V
		V <sub>CC</sub> = 5 V	4.5	5	5.5	
V <sub>IH</sub>	Driver and control high-level input voltage	DIN, $\overline{\text{SHDN}}$ , MBAUD, $\overline{\text{EN}}$	V <sub>CC</sub> = 3.3 V	2	5.5	V
			V <sub>CC</sub> = 5 V	2.4	5.5	
V <sub>IL</sub>	Driver and control low-level input voltage	DIN, $\overline{\text{SHDN}}$ , MBAUD, $\overline{\text{EN}}$	0		0.8	V
V <sub>I</sub>	Receiver input voltage		–25		25	V
T <sub>A</sub>	Operating free-air temperature	TRS3237EC	0		70	°C
		TRS3237EI	–40		85	

- (1) Test conditions are C1–C4 = 0.1 μF at V<sub>CC</sub> = 3 V to 5 V.

## ELECTRICAL CHARACTERISTICS<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5](#))

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(2)</sup>	MAX	UNIT
I <sub>I</sub>	Input leakage current	DIN, $\overline{\text{SHDN}}$ , MBAUD, $\overline{\text{EN}}$		9	18	μA
I <sub>CC</sub>	Supply current (T <sub>A</sub> = 25°C)	No load, $\overline{\text{SHDN}}$ = V <sub>CC</sub>		0.5	2	mA
		$\overline{\text{SHDN}}$ = GND		1	10	μA
		Shutdown supply current $\overline{\text{SHDN}}$ = RIN = GND, DIN = GND or V <sub>CC</sub>		10	300	nA

- (1) Test conditions are C1–C4 = 0.1 μF at V<sub>CC</sub> = 3 V to 5 V.
- (2) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

## DRIVER SECTION ELECTRICAL CHARACTERISTICS<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5](#))

PARAMETER	TEST CONDITIONS	MIN	TYP <sup>(2)</sup>	MAX	UNIT
V <sub>OH</sub> High-level output voltage	DOUT at R <sub>L</sub> = 3 kΩ to GND, DIN = GND	5	5.4		V
V <sub>OL</sub> Low-level output voltage	DOUT at R <sub>L</sub> = 3 kΩ to GND, DIN = V <sub>CC</sub>	–5	–5.4		V
I <sub>IH</sub> High-level input current	V <sub>I</sub> = V <sub>CC</sub>		±0.01	±1	μA
I <sub>IL</sub> Low-level input current	V <sub>I</sub> at GND		±0.01	±1	μA
I <sub>OS</sub> Short-circuit output current <sup>(3)</sup>	V <sub>CC</sub> = 3.6 V or 3.3 V, V <sub>O</sub> = 0 V			±60	mA
r <sub>o</sub> Output resistance	V <sub>CC</sub> , V <sub>+</sub> , and V <sub>–</sub> = 0 V, V <sub>O</sub> = ±2 V	300	50k		Ω

(1) Test conditions are C1–C4 = 0.1 μF at V<sub>CC</sub> = 3 V to 5 V.

(2) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

(3) Short-circuit durations should be controlled to prevent exceeding the device absolute power-dissipation ratings, and not more than one output should be shorted at a time.

## DRIVER SECTION SWITCHING CHARACTERISTICS<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5](#))

PARAMETER	TEST CONDITIONS			MIN	TYP <sup>(2)</sup>	MAX	UNIT
Maximum data rate	C <sub>L</sub> = 1000 pF, MBAUD = GND	R <sub>L</sub> = 3 kΩ, 1 DIN switching, See <a href="#">Figure 1</a>		250		kbit/s	
	1000						
	1000						
	C <sub>L</sub> = 250 pF, V <sub>CC</sub> = 3 V to 4.5 V, MBAUD = V <sub>CC</sub>						
t <sub>sk(p)</sub>	Pulse skew <sup>(3)</sup>	C <sub>L</sub> = 150 pF to 2500 pF, R <sub>L</sub> = 3 kΩ to 7 kΩ, MBAUD = V <sub>CC</sub> or GND, See <a href="#">Figure 2</a>			100		ns
SR(tr)	Slew rate, transition region (see <a href="#">Figure 1</a> )	V <sub>CC</sub> = 3.3 V, R <sub>L</sub> = 3 kΩ to 7 kΩ, T <sub>A</sub> = 25°C	C <sub>L</sub> = 150 pF to 1000 pF	MBAUD = GND	6	30	V/μs
				MBAUD = V <sub>CC</sub>	24	150	
		C <sub>L</sub> = 150 pF to 2500 pF,	MBAUD = GND	4	30		

(1) Test conditions are C1–C4 = 0.1 μF at V<sub>CC</sub> = 3 V to 5 V.

(2) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

(3) Pulse skew is defined as |t<sub>PLH</sub> – t<sub>PHL</sub>| of each channel of the same device.

## RECEIVER SECTION ELECTRICAL CHARACTERISTICS<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5](#))

PARAMETER	TEST CONDITIONS	MIN	TYP <sup>(2)</sup>	MAX	UNIT
V <sub>OH</sub> High-level output voltage	I <sub>OH</sub> = –1 mA	V <sub>CC</sub> – 0.6	V <sub>CC</sub> – 0.1		V
V <sub>OL</sub> Low-level output voltage	I <sub>OL</sub> = 1 mA			0.4	V
V <sub>IT+</sub> Positive-going input threshold voltage	V <sub>CC</sub> = 3.3 V		1.5	2.4	V
	V <sub>CC</sub> = 5 V		2	2.4	
V <sub>IT–</sub> Negative-going input threshold voltage	V <sub>CC</sub> = 3.3 V	0.6	1.1		V
	V <sub>CC</sub> = 5 V	0.8	1.5		
V <sub>hys</sub> Input hysteresis (V <sub>IT+</sub> – V <sub>IT–</sub> )			0.5		V
I <sub>oz</sub> Output leakage current	$\overline{\text{EN}} = V_{CC}$		±0.05	±10	μA
r <sub>i</sub> Input resistance	V <sub>I</sub> = ±3 V to ±25 V	3	5	7	kΩ

(1) Test conditions are C1–C4 = 0.1 mF at V<sub>CC</sub> = 3 V to 5 V.

(2) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

## RECEIVER SECTION SWITCHING CHARACTERISTICS<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TYP <sup>(2)</sup>	UNIT
t <sub>PLH</sub> Propagation delay time, low- to high-level output	C <sub>L</sub> = 150 pF, See <a href="#">Figure 3</a>	150	ns
t <sub>PHL</sub> Propagation delay time, high- to low-level output	C <sub>L</sub> = 150 pF, See <a href="#">Figure 3</a>	150	ns
t <sub>en</sub> Output enable time	C <sub>L</sub> = 150 pF, R <sub>L</sub> = 3 kΩ, See <a href="#">Figure 4</a>	2.6	μs
t <sub>dis</sub> Output disable time	C <sub>L</sub> = 150 pF, R <sub>L</sub> = 3 kΩ, See <a href="#">Figure 4</a>	2.4	μs
t <sub>sk(p)</sub> Pulse skew <sup>(3)</sup>	See <a href="#">Figure 3</a>	50	ns

(1) Test conditions are C1–C4 = 0.1 μF at V<sub>CC</sub> = 3 V to 5 V.

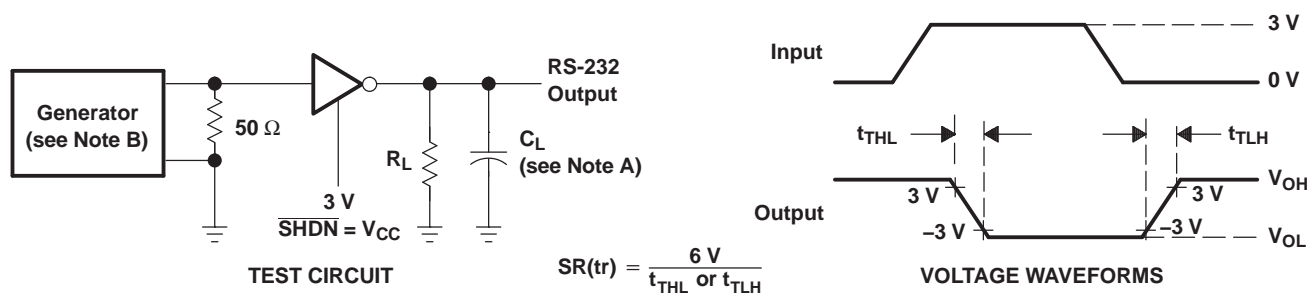
(2) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

(3) Pulse skew is defined as |t<sub>PLH</sub> – t<sub>PHL</sub>| of each channel of the same device.

## ESD PROTECTION

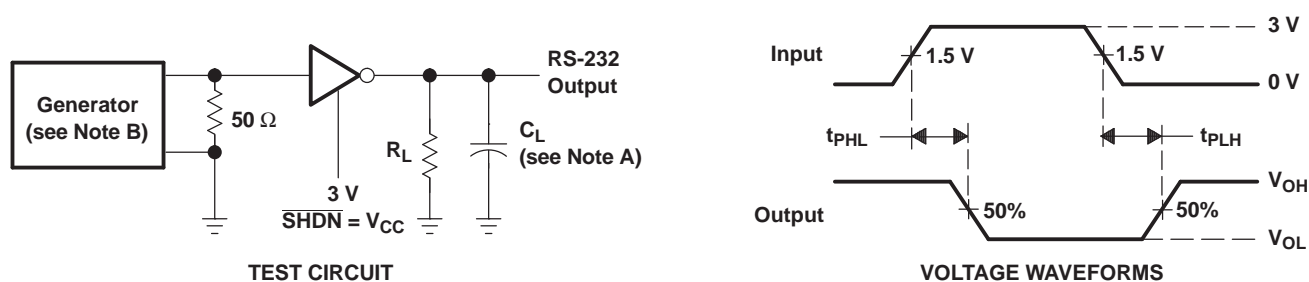
PIN	TEST CONDITIONS	TYP	UNIT
DOUT, RIN	IEC61000-4-2, Contact Discharge	±8	kV
	IEC61000-4-2, Air-Gap Discharge	±15	

## PARAMETER MEASUREMENT INFORMATION



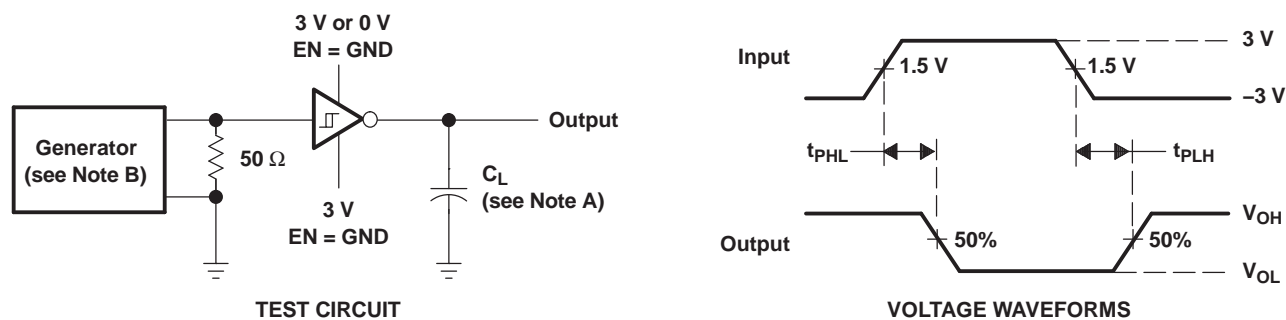
- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.  
B. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z<sub>O</sub> = 50 Ω, 50% duty cycle, t<sub>r</sub> ≤ 10 ns, t<sub>f</sub> ≤ 10 ns.

Figure 1. Driver Slew Rate



- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.  
B. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z<sub>O</sub> = 50 Ω, 50% duty cycle, t<sub>r</sub> ≤ 10 ns, t<sub>f</sub> ≤ 10 ns.

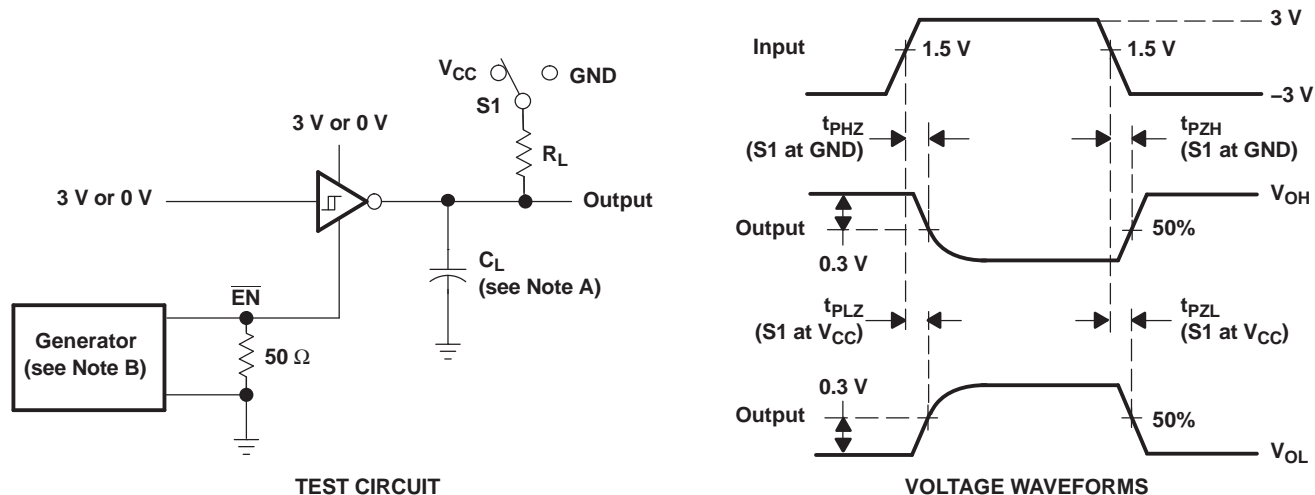
Figure 2. Driver Pulse Skew



- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.  
B. The pulse generator has the following characteristics: Z<sub>O</sub> = 50 Ω, 50% duty cycle, t<sub>r</sub> ≤ 10 ns, t<sub>f</sub> ≤ 10 ns.

Figure 3. Receiver Propagation Delay Times

## PARAMETER MEASUREMENT INFORMATION (continued)

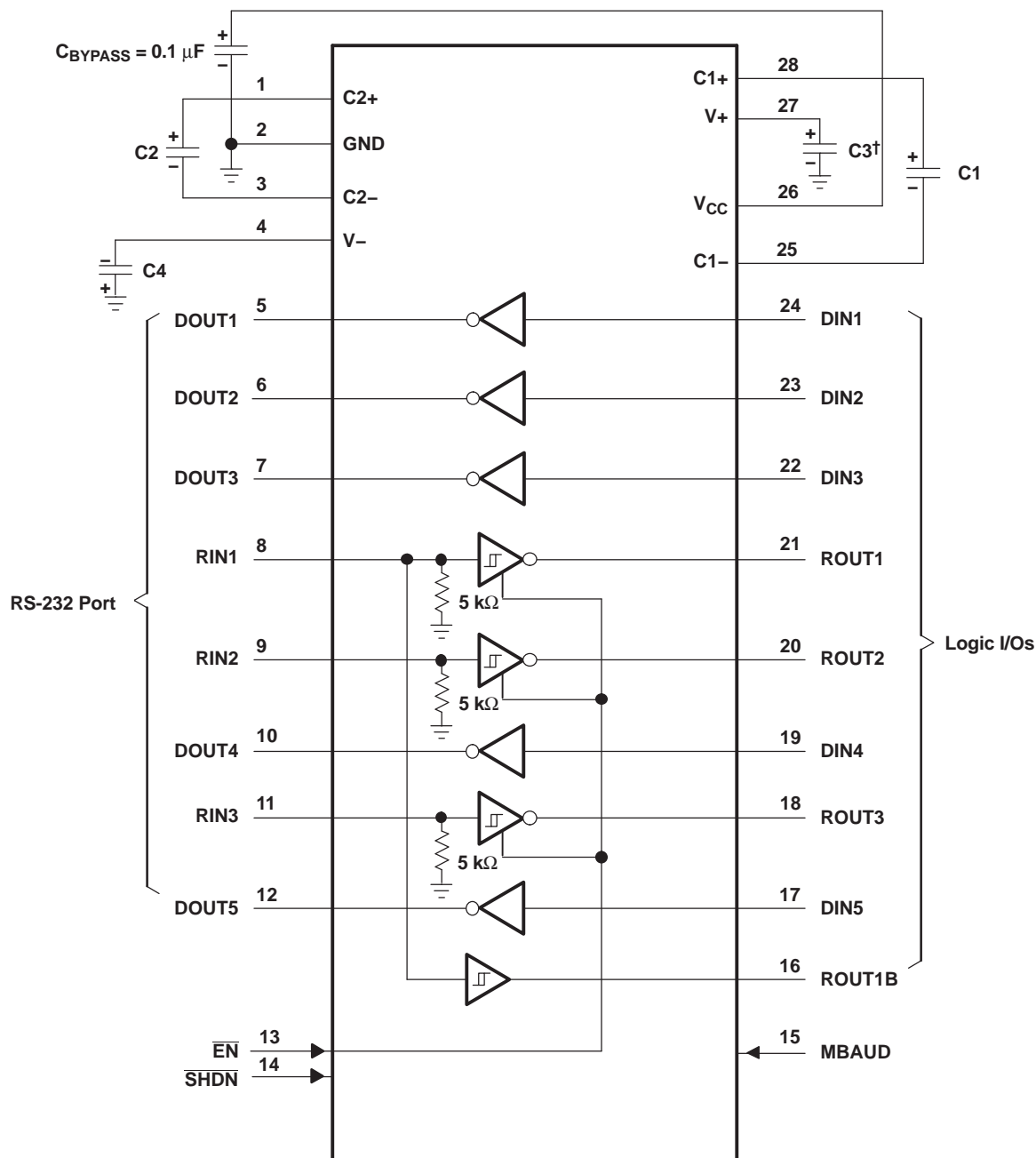


- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. The pulse generator has the following characteristics:  $Z_O = 50\ \Omega$ , 50% duty cycle,  $t_r \leq 10\ \text{ns}$ ,  $t_f \leq 10\ \text{ns}$ .
  - C.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - D.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .

**Figure 4. Receiver Enable and Disable Times**



## APPLICATION INFORMATION



† C3 can be connected to V<sub>CC</sub> or GND.

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

V<sub>CC</sub> vs CAPACITOR VALUES

V <sub>CC</sub>	C1	C2, C3, and C4
3.3 V ± 0.15 V	0.1 μF	0.1 μF
3.3 V ± 0.3 V	0.22 μF	0.22 μF
5 V ± 0.5 V	0.047 μF	0.33 μF
3 V to 5.5 V	0.22 μF	1 μF

Figure 5. Typical Operating Circuit and Capacitor Values

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TRS3237ECDB	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS3237EC	<a href="#">Samples</a>
TRS3237ECDBG4	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS3237EC	<a href="#">Samples</a>
TRS3237ECDBR	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS3237EC	<a href="#">Samples</a>
TRS3237ECDBRG4	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS3237EC	<a href="#">Samples</a>
TRS3237ECDW	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS3237EC	<a href="#">Samples</a>
TRS3237ECDWG4	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS3237EC	<a href="#">Samples</a>
TRS3237ECDWR	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS3237EC	<a href="#">Samples</a>
TRS3237ECDWRG4	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS3237EC	<a href="#">Samples</a>
TRS3237ECPWR	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	RS37EC	<a href="#">Samples</a>
TRS3237ECPWRG4	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	RS37EC	<a href="#">Samples</a>
TRS3237EIDB	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3237EI	<a href="#">Samples</a>
TRS3237EIDBG4	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3237EI	<a href="#">Samples</a>
TRS3237EIDBR	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3237EI	<a href="#">Samples</a>
TRS3237EIDBRG4	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3237EI	<a href="#">Samples</a>
TRS3237EIDWR	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3237EI	<a href="#">Samples</a>
TRS3237EIDWRG4	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3237EI	<a href="#">Samples</a>
TRS3237EIPW	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	RS37EI	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TRS3237EIPWG4	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	RS37EI	<a href="#">Samples</a>
TRS3237EIPWR	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	RS37EI	<a href="#">Samples</a>
TRS3237EIPWRG4	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	RS37EI	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRS3237ECDBR	SSOP	DB	28	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TRS3237ECDWR	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
TRS3237ECPWR	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
TRS3237EIDBR	SSOP	DB	28	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TRS3237EIDWR	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
TRS3237EIPWR	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS

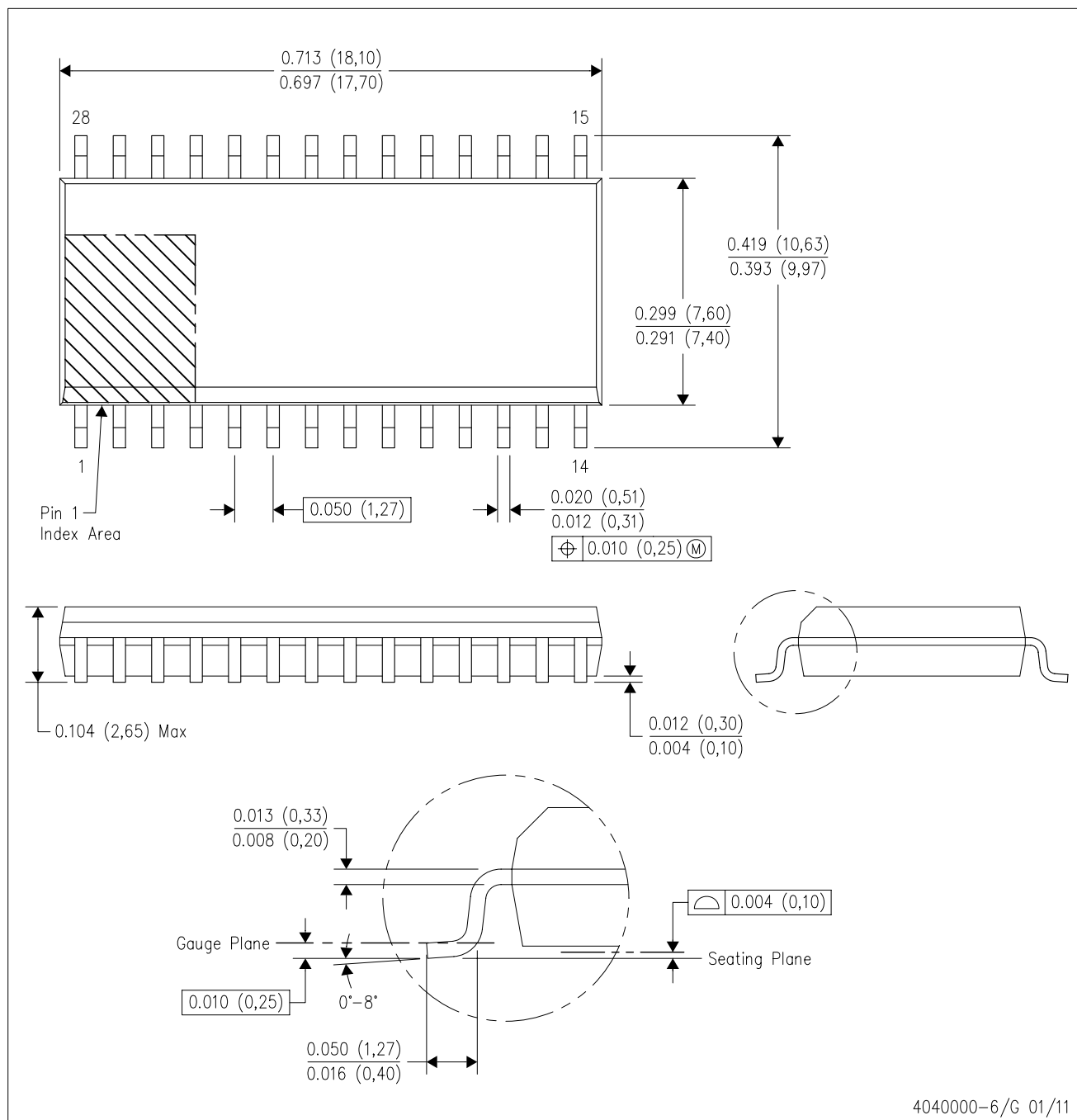


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRS3237ECDBR	SSOP	DB	28	2000	367.0	367.0	38.0
TRS3237ECDWR	SOIC	DW	28	1000	367.0	367.0	55.0
TRS3237ECPWR	TSSOP	PW	28	2000	367.0	367.0	38.0
TRS3237EIDBR	SSOP	DB	28	2000	367.0	367.0	38.0
TRS3237EIDWR	SOIC	DW	28	1000	367.0	367.0	55.0
TRS3237EIPWR	TSSOP	PW	28	2000	367.0	367.0	38.0

DW (R-PDSO-G28)

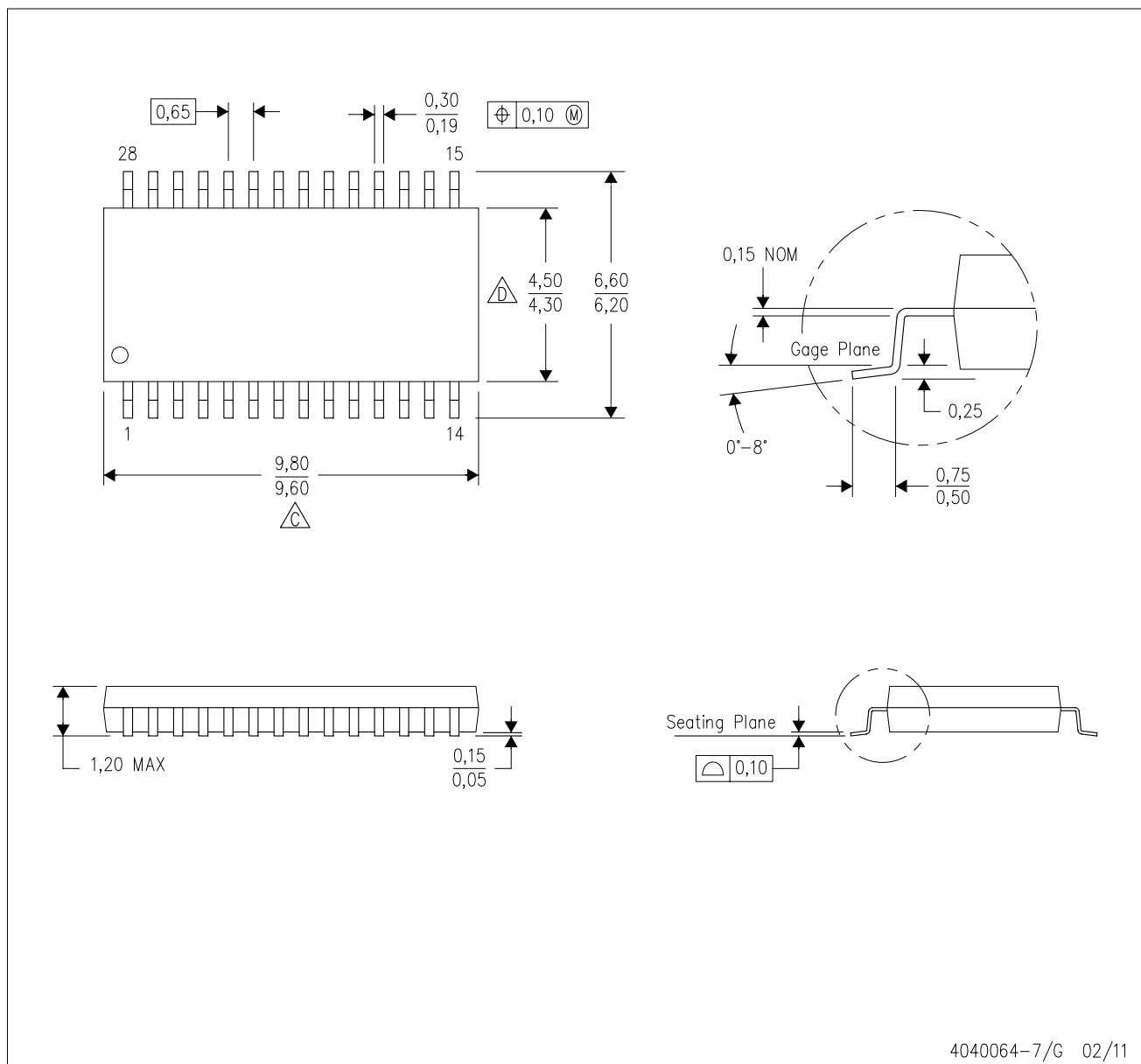
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MS-013 variation AE.

PW (R-PDSO-G28)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153



PW (R-PDSO-G28)

PLASTIC SMALL OUTLINE

Example Board Layout



Example  
Non Soldermask Defined Pad



Stencil Openings  
Based on a stencil thickness  
of .127mm (.005inch).



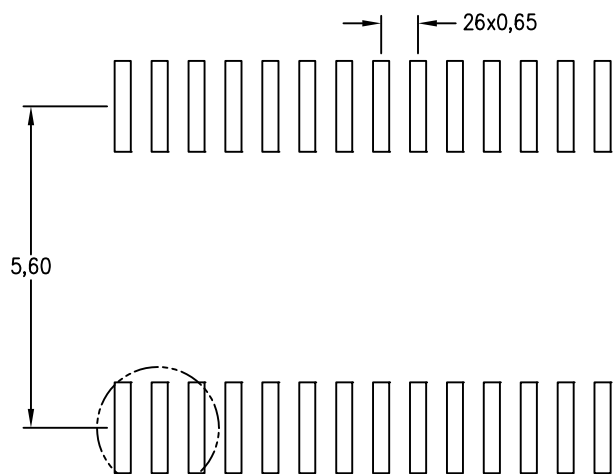
4211284-6/F 12/12

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

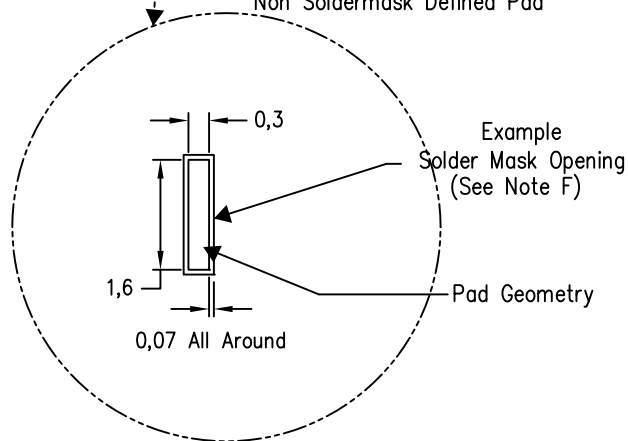
PW (R-PDSO-G28)

PLASTIC SMALL OUTLINE

Example Board Layout



Example  
Non Soldermask Defined Pad



Stencil Openings  
Based on a stencil thickness  
of .127mm (.005inch).



4211284-6/F 12/12

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

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