# TINY 1.5-A BOOST CONVERTER WITH ADJUSTABLE INPUT CURRENT LIMIT

**Check for Samples: TPS61252**

## FEATURES

- **Resistor Programmable Input Current Limit**
  - **±20% Current Accuracy at 500 mA over Full Temperature Range**
  - **Programmable from 100 mA up to 1500 mA**
- **Up to 92% Efficiency**
- **$V_{IN}$ Range from 2.3 V to 6.0 V**
- **Power Good Indicates Appropriate Output Voltage Level**
- **Adjustable Output Voltage up to 6.5 V**
- **100% Duty-Cycle Mode When $V_{IN} > V_{OUT}$**
- **Load Disconnect and Reverse Current Protection**
- **Short Circuit Protection**
- **Typical Operating Frequency 3.25 MHz**
- **Available in a 2×2-mm QFN-8 Package**

## APPLICATIONS

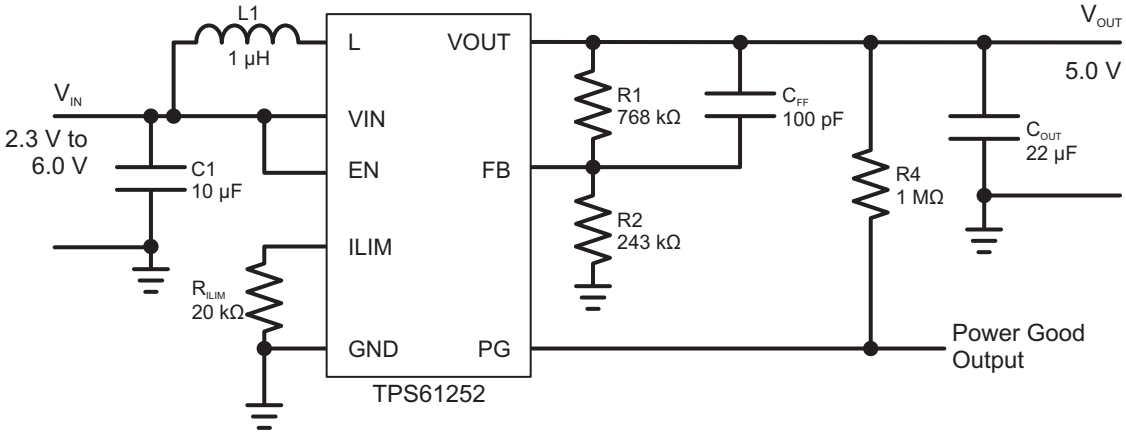
- **USB Host Supplies from a Single Li-Ion Battery**
- **Current Limited Applications**
- **Li-Ion Applications**
- **Audio Applications**
- **RF-PA Buffer**

## DESCRIPTION

The TPS61252 device provides a power supply solution for products powered by either a three-cell alkaline, NiCd or NiMH battery, or an one-cell Li-Ion or Li-polymer battery. The wide input voltage range is ideal to power portable applications like mobile phones or for computer peripherals. The device has a resistor programmable ($R_{ILIM}$) input current limit and is suitable for a wide variety of applications.

During light loads the device will automatically enter skip mode (PFM), which allows the converter to maintain the required output voltage, while only drawing 30 μA from the battery. This will allow maximum efficiency at lowest quiescent currents.

TPS61252 allows the use of small inductors and input capacitors to achieve a small solution size. The possibility to reduce the current limit by a external resistor offers the potential use of physically even smaller inductors with lower rated current to further reduce total solution sizes of the power supply. During shutdown, the load is completely disconnected from the battery. The TPS61252 is available in a 8-pin QFN package measuring 2×2 mm (DSG).

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## AVAILABLE DEVICE OPTION

| $T_A$ | OUTPUT VOLTAGE(1) | PACKAGE MARKING | PACKAGE | PART NUMBER(2) |
|---|---|---|---|---|
| –40°C to 85°C | Adjustable | QTI | 8-Pin QFN | TPS61252DSG |

(1) Contact TI for other fixed output voltage options
(2) For detailed ordering information please check the PACKAGE OPTION ADDENDUM section at the end of this datasheet.

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Voltage range(2) | VIN, VOUT, SW, EN, PG, FB, ILIM | –0.3 | 7 | V |
| Temperature range | Operating junction, $T_J$ | –40 | 150 | °C |
| | Storage, $T_{stg}$ | –65 | 150 | °C |
| ESD rating(3) | Human Body Model - (HBM) | | 2 | kV |
| | Charge Device Model - (CDM) | | 0.5 | kV |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
(2) All voltages are with respect to network ground terminal.
(3) ESD testing is performed according to the respective JESD22 JEDEC standard.

## THERMAL INFORMATION

| THERMAL METRIC(1) | | TPS61252 DSG 8 PINS | UNITS |
|---|---|---|---|
| $\theta_{JA}$ | Junction-to-ambient thermal resistance | 80.2 | °C/W |
| $\theta_{JCtop}$ | Junction-to-case (top) thermal resistance | 93.5 | |
| $\theta_{JB}$ | Junction-to-board thermal resistance | 54.2 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.9 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 59.3 | |
| $\theta_{JCbot}$ | Junction-to-case (bottom) thermal resistance | 20 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.


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## RECOMMENDED OPERATING CONDITIONS

| | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage at VIN | 2.3 | | 6.0 | V |
| Output voltage at VOUT | 3.0 | | 6.5 | V |
| Programmable valley switch current limit set by $R_{ILIM}$ | 100 | | 1500 | mA |
| Operating free air temperature range, $T_A$ | –40 | | 85 | °C |
| Operating junction temperature range, $T_J$ | –40 | | 125 | °C |

## ELECTRICAL CHARACTERISTICS

Over recommended free air temperature range, typical values are at $T_A$ = 25°C. Unless otherwise noted, specifications apply for condition $V_{IN}$ = EN = 3.6 V, $V_{OUT}$ = 5.0 V.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **DC/DC STAGE** | | | | | | |
| $V_{FB}$ | Feedback voltage | | 1.182 | 1.2 | 1.218 | V |
| | Maximum line regulation | | | 0.5 | | % |
| | Maximum load regulation | | | 0.5 | | % |
| f | Oscillator frequency | | | 3250 | | kHz |
| $r_{DS(on)}$ | High side switch on resistance | | | 200 | | mΩ |
| | Low side switch on resistance | | | 130 | | mΩ |
| | Reverse leakage current into $V_{OUT}$ | EN = GND | | | 3.5 | µA |
| $I_{V(CL)}$ | Programmable valley switch current limit | ILIM pin set to $V_{IN}$ | | 1500 | | mA |
| | | $R_{ILIM}$ = 20 kΩ (500mA) | -20 | | +20 | % |
| $I_Q$ | Quiescent current | PFM enabled, device is not switching | | 30 | | µA |
| $I_{SD}$ | Shutdown current | | | 0.85 | 3.5 | µA |
| OVP | Input over voltage protection threshold | Falling | | 6.4 | | V |
| | | Rising | | 6.5 | | V |
| **CONTROL STAGE** | | | | | | |
| $V_{UVLO}$ | Under voltage lockout threshold | Falling | | 2.0 | 2.1 | V |
| | | Hysteresis | | 0.1 | | V |
| $V_{IL}$ | EN input low voltage | 2.3 V ≤ $V_{IN}$ ≤ 6.0 V | | | 0.4 | V |
| $V_{IH}$ | EN input high voltage | 2.3 V ≤ $V_{IN}$ ≤ 6.0 V | 1.0 | | | V |
| | EN, PG input leakage current | Clamped to GND or $V_{IN}$ | | | 0.5 | µA |
| | Power Good threshold voltage | Rising referred to $V_{FB}$ | 92.5 | 95 | 97.5 | % |
| | | Falling referred to $V_{FB}$ | 87.5 | 90 | 92.5 | % |
| | Power good delay | | | 10 | | µs |
| | Overtemperature protection | | | 140 | | °C |
| | Overtemperature hysteresis | | | 20 | | °C |

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## PIN ASSIGNMENTS

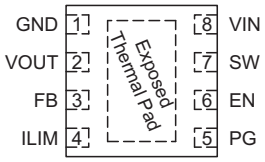


**Table 1. TERMINAL FUNCTIONS**

| TERMINAL | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| EN | 6 | I | Enable input. (1 enabled, 0 disabled) |
| FB | 3 | I | Voltage feedback pin |
| GND | 1 | | Ground |
| ILIM | 4 | I | Adjustable input valley current limit. Can be connected to $V_{IN}$ for maximum current. |
| PG | 5 | O | Output power good (1 good, 0 failure; open drain) |
| SW | 7 | I | Connection for Inductor |
| VIN | 8 | I | Supply voltage for power stage |
| VOUT | 2 | O | Boost converter output |
| Exposed Thermal Pad | | | Must be soldered to achieve appropriate power dissipation and for mechanical reasons. Must be connected to GND. |


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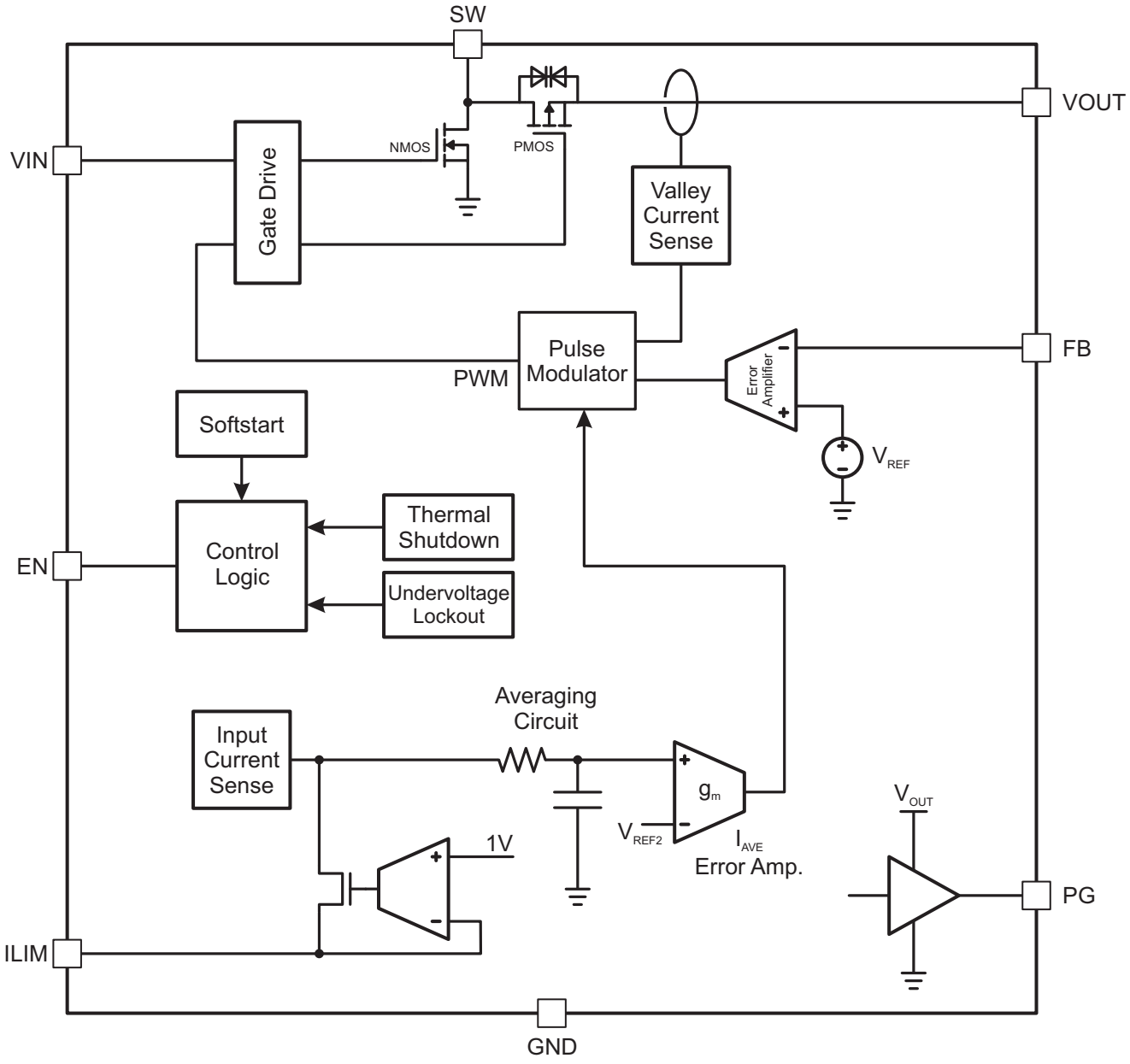
## FUNCTIONAL BLOCK DIAGRAM



## PARAMETER MEASUREMENT INFORMATION

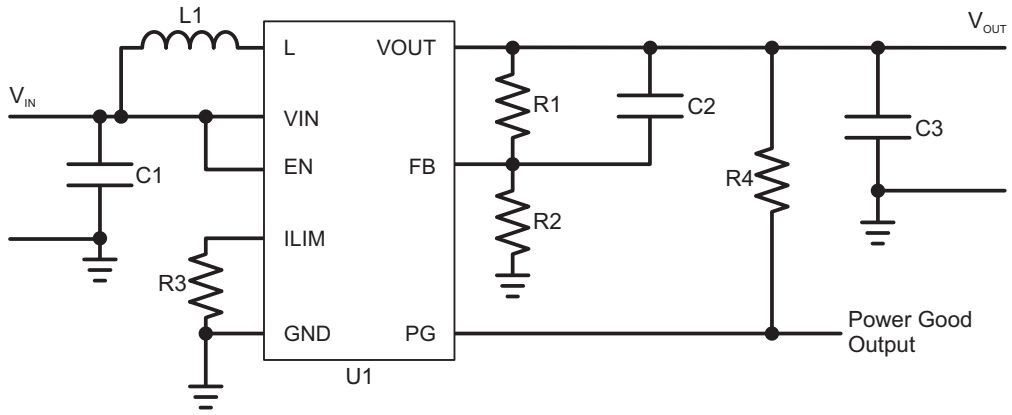



**Table 2. List of Components**

| REFERENCE | DESCRIPTION | MANUFACTURER |
|---|---|---|
| U1 | TPS61252 | Texas Instruments |
| L1 | 1.0 μH, 2.1 A, 27 mΩ, 2.8 mm x 2.8 mm x 1.5 mm | DEM2815C, TOKO |
| C1 | 1 x 4.7 μF, 10 V, 0805, X7R ceramic | GRM21BR71A475KA73, Murata |
| C2 | 1 x 100 pF, 50 V, 0603, COG ceramic | GRM1885C1H101JA01B, Murata |
| C3 | 2 × 22 μF, 10 V, 0805, X7R ceramic | GRM21BR61A226ME51, Murata |
| R1 | Depending on the output voltage of TPS61252, 1%, (all measurements with 5 V output voltage uses 768 kΩ) | |
| R2 | Depending on the output voltage of TPS61252, 1%, (all measurements with 5 V output voltage uses 240 kΩ) | |
| R3 | Depending on the input current limit of TPS61252, 1% | |
| R4 | 1 MΩ, 1% | any |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## TYPICAL CHARACTERISTICS

### TABLE OF GRAPHS

| DESCRIPTION | | FIGURE |
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| | vs Output current in 100% Duty-Cycle Mode ($V_{OUT}$ = 5.0 V, $I_{LIM}$ = 1.5 A) | Figure 2 |
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| Output voltage | vs Output current ($V_{OUT}$ = 5.0 V, $I_{LIM}$ = 1.5 A) | Figure 5 |
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| | Load transient response ($V_{IN}$ > $V_{OUT}$, $I_{LIM}$ = 1000mA, Load change from 50 mA to 550 mA) | Figure 7 |
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**EFFICIENCY vs OUTPUT CURRENT**

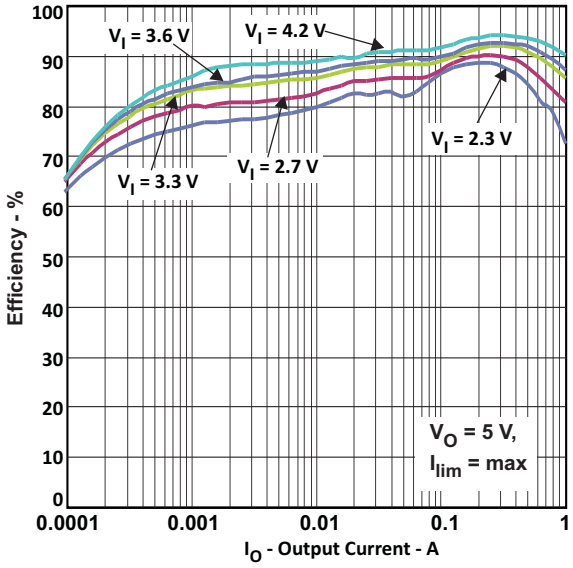


Figure 1.

**EFFICIENCY vs OUTPUT CURRENT – IN 100% DUTY CYCLE MODE**

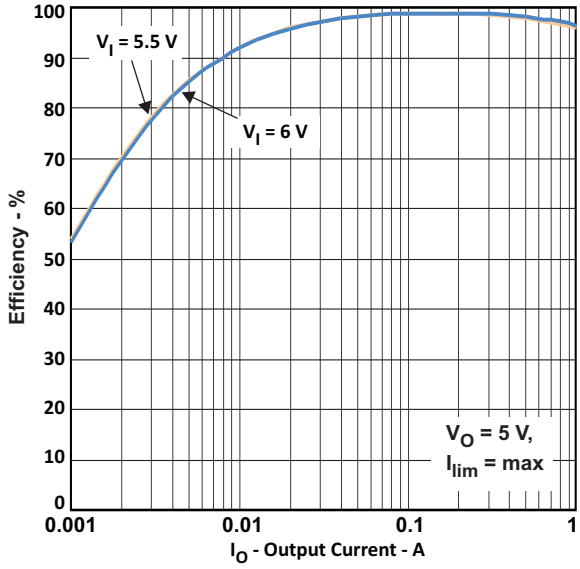


Figure 2.

EFFICIENCY
vs
INPUT VOLTAGE

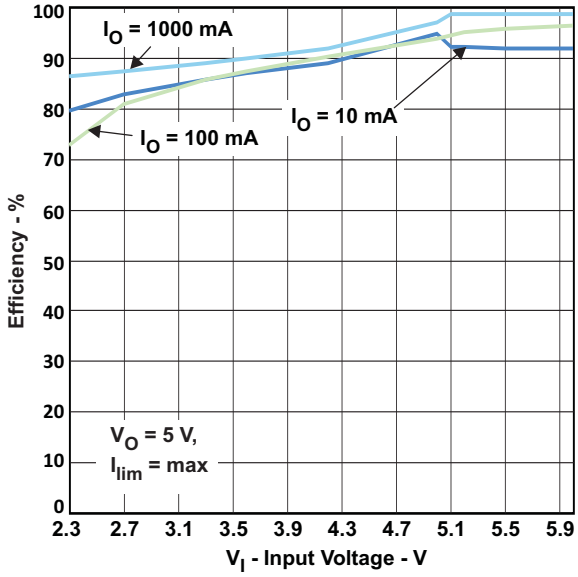


Figure 3.

MAXIMUM OUTPUT CURRENT
vs
INPUT VOLTAGE

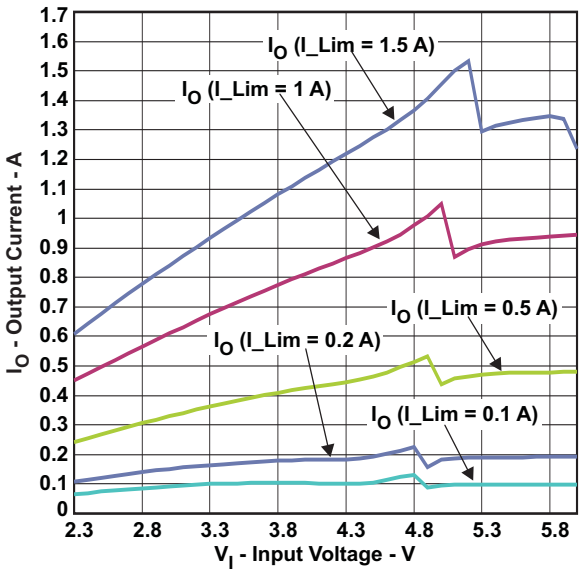


Figure 4.

OUTPUT VOLTAGE
vs
OUTPUT CURRENT

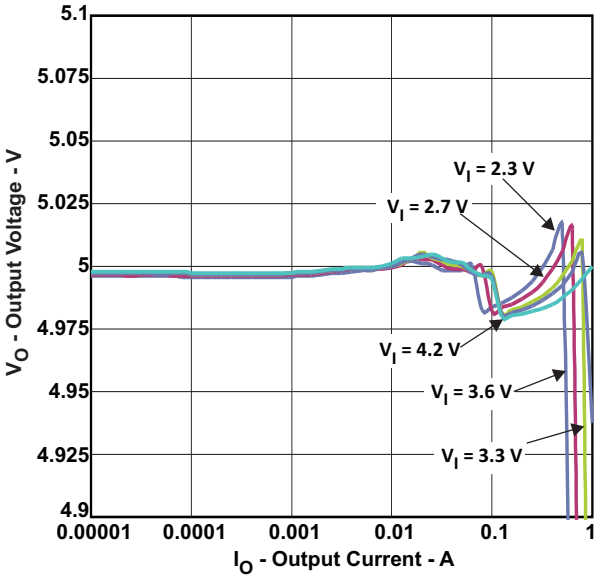


Figure 5.

LOAD TRANSIENT RESPONSE $I_{LIM}$ = 500 mA (20 to 300 mA)

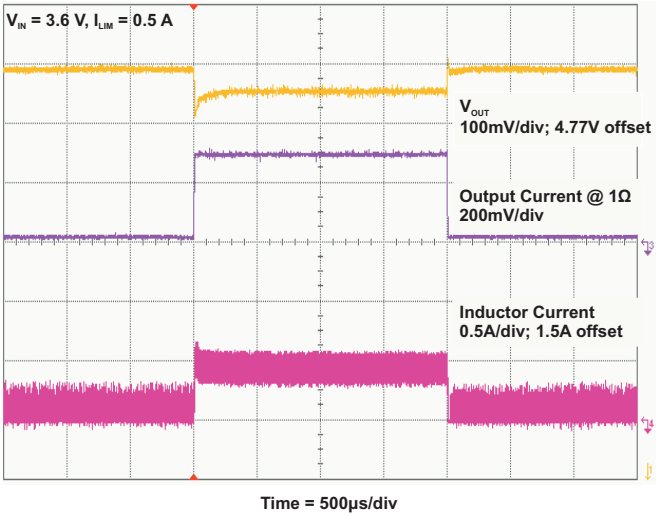


Figure 6.


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**LOAD TRANSIENT RESPONSE $I_{LIM}$ = 1000 mA (50 to 550 mA)**

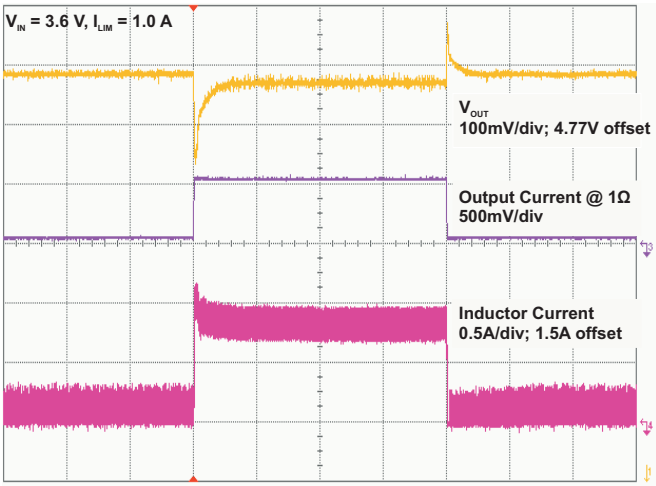


**Figure 7.**

**STARTUP AFTER ENABLE $I_{LIM}$ = 500mA, NO LOAD**

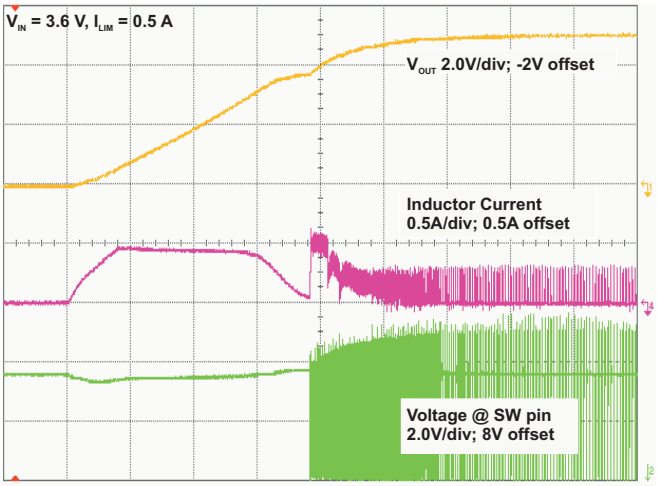


**Figure 8.**

**STARTUP AFTER ENABLE $I_{LIM}$ = 1000mA, NO LOAD**

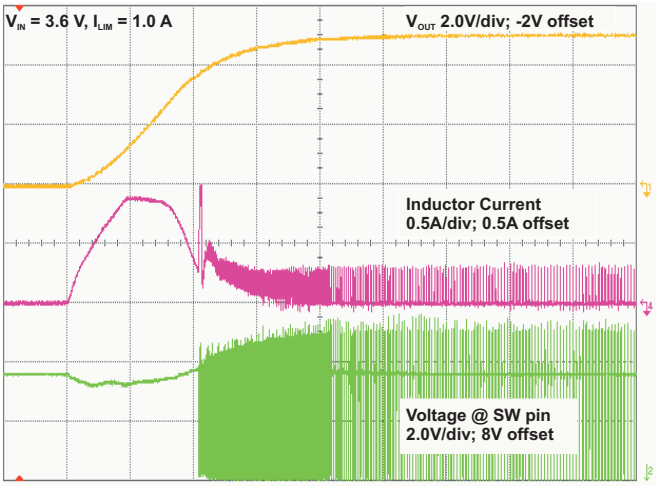


**Figure 9.**

**STARTUP AFTER ENABLE $I_{LIM}$ = 1000mA, 500 mA LOAD**

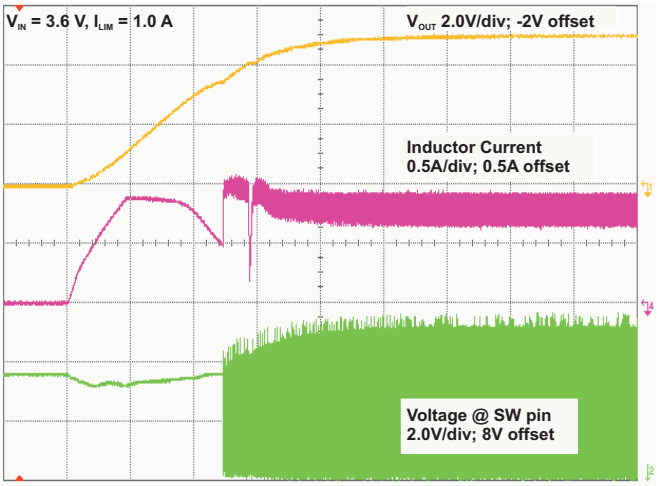


**Figure 10.**

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# DETAILED DESCRIPTION

## OPERATION

The TPS61252 Boost Converter operates as a quasi-constant frequency adaptive on-time controller. In a typical application the frequency will be 3.25 MHz and is defined by the input to output voltage ratio and does not vary from moderate to heavy load currents. At light load currents the converter will automatically enter Power Save Mode and operates then in PFM (Pulse Frequency Modulation) mode. During pulse-width-modulation (PWM) operation the converter uses a unique fast response quasi-constant on-time valley current mode controller scheme which offers very good line and load regulation allowing the use of small ceramic input and output capacitors.

Based on the $V_{IN}/V_{OUT}$ ratio, a simple circuit predicts the required on-time. At the beginning of the switching cycle, the low-side NMOS switch is turned-on and the inductor current ramps up to a peak current that is defined by the on-time and the inductance. In the second phase, once the peak current is reached, the current comparator trips, the on-timer is reset turning off the switch, and the current through the inductor then decays to an internally set valley current limit. Once this occurs, the on-timer is set to turn the boost switch back on again and the cycle is repeated.

The TPS61252 controls the input current through intelligent adjustment of a valley current limit that corrects the value in a way that it almost turns out as an average input current limit. The current can be adjusted with an accuracy of ±20%.

This architecture with adaptive slope compensation provides excellent transient load response and requires minimal output filtering. Internal softstart and loop compensation simplifies the design process while minimizing the number of external components.

## CURRENT LIMIT OPERATION

The current limit circuit employs a valley current sensing scheme. Current limit detection occurs during the off time through sensing of the voltage drop across the synchronous rectifier.

The output voltage is reduced as the power stage of the device operates in a constant current mode. The maximum continuous output current ($I_{OUT(CL)}$), before entering current limit (CL) operation, can be defined by Equation 1.

$$I_{OUT(CL)} = (1 - D) \cdot \left(I_{V(CL)} + \frac{1}{2} \Delta I_L\right) \quad (1)$$

The duty cycle (D) can be estimated by Equation 2

$$D = 1 - \frac{V_{IN} \cdot \eta}{V_{OUT}} \quad (2)$$

and the peak-to-peak current ripple ($\Delta I_L$) is calculated by Equation 3

$$\Delta I_L = \frac{V_{IN} \cdot D}{L \cdot f} \quad (3)$$

The output current, $I_{OUT(DC)}$, is the average of the rectifier current waveform. When the load current is increased such that the lower peak is above the current limit threshold, the off-time is increased to allow the current to decrease to this threshold before the next on-time begins. When the current limit is reached the output voltage decreases if the load is further increased.

## SOFTSTART

The TPS61252 has an internal softstart circuit that controls the ramp-up of the current during start-up and prevents the converter from inrush current that exceeds the set current limit. For typical 100 µs the current is ramped to the set current limit. After reaching the current limit threshold it stays there until $V_{IN} = V_{OUT}$ then the converter starts switching and boosting up the voltage to its nominal output voltage. During the complete start-up the input current does not exceed the current limit that is set by resistor $R_{ILIM}$.


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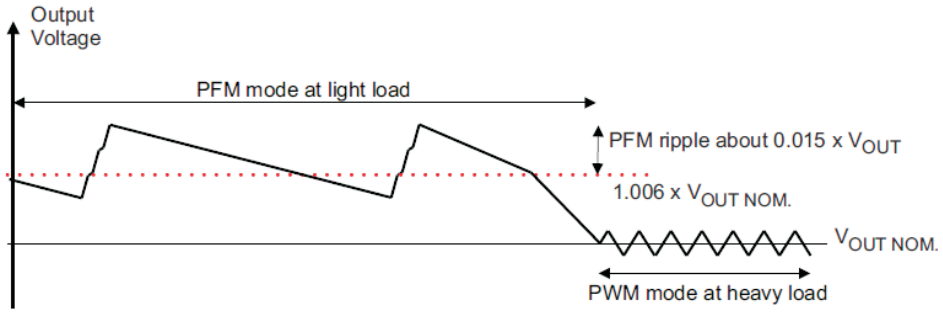
## POWER-SAVE MODE

The TPS61252 integrates a power save mode to improve efficiency at light load. In power save mode the converter only operates when the output voltage trips below a set threshold voltage. It ramps up the output voltage with several pulses and goes into power save mode once the output voltage exceeds the set threshold voltage. During the power save operation when the output voltage is above the set threshold the converter turns off some of the inner circuits to save energy.




The PFM mode is left and PWM mode entered in case the output current can no longer be supported in PFM mode.

## 100% DUTY-CYCLE MODE

If $V_{IN}$ > $V_{OUT}$ the TPS61251 offers the lowest possible input-to-output voltage difference while still maintaining current limit operation with the use of the 100% duty-cycle mode. In this mode, the PMOS switch is constantly turned on. During this operation the output voltage follows the input voltage and will not fall below the programmed value if the input voltage decreases below $V_{OUT}$. The output voltage drop during 100% mode depends on the load current and input voltage, and the resulting output voltage is calculated as:

$$V_{OUT} = V_{IN} - \left(DCR + r_{DS(on)}\right) \cdot I_{OUT} \quad (4)$$

with:

DCR is the DC resistance of the inductor

$r_{DS(on)}$ is the typical on-resistance of the PMOS switch

## ENABLE

The device is enabled by setting EN pin to a voltage above 1 V. At first, the internal reference is activated and the internal analog circuits are settled. Afterwards, the output voltage ramps up controlled by the softstart circuitry. The output voltage reaches its nominal value as fast as the current limit settings and the load condition allows it.

The EN input can be used to control power sequencing in a system with several DC/DC converters. The EN pin can be connected to the output of another converter, to drive the EN pin high and getting a sequencing of supply rails. With EN = GND, the device enters shutdown mode.

## UNDER-VOLTAGE LOCKOUT (UVLO)

The under voltage lockout circuit prevents the device from malfunctioning at low input voltages and the battery from excessive discharge. It disables the output stage of the converter once the falling $V_{IN}$ trips the under-voltage lockout threshold $V_{UVLO}$ which is typically 2.0V. The device starts operation once the rising $V_{IN}$ trips $V_{UVLO}$ threshold plus its hysteresis of 100 mV at typ. 2.1V.

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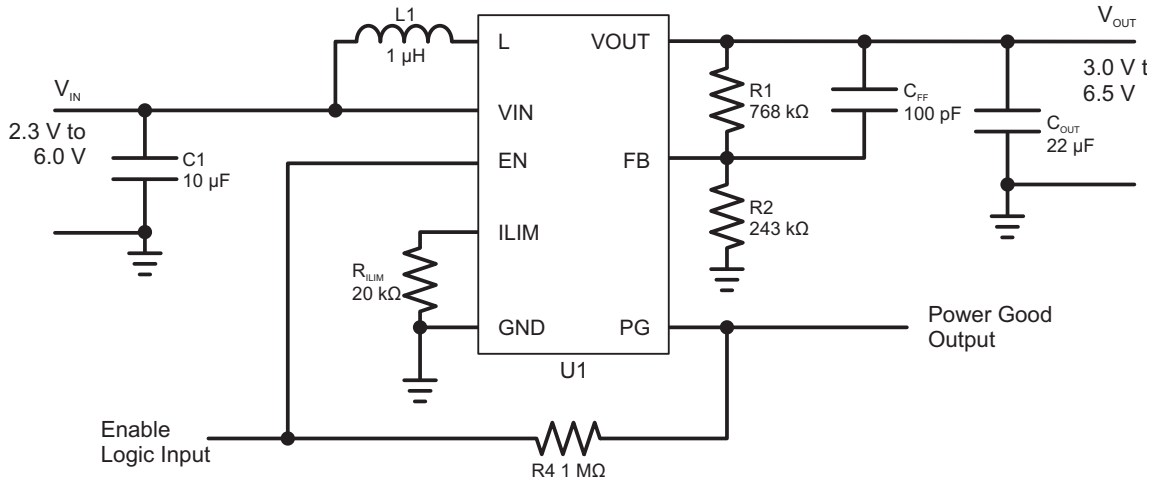
## POWER GOOD

The device has a built in power good function to indicate whether the output voltage operates within appropriate levels. The power good output (PG) is set high after the feedback voltage reaches 95% of its nominal value and stays there until the feedback voltage falls below 90 % of the nominal value. The power good is operable as long as the converter is enabled and $V_{IN}$ is present. If the converter is disabled by pulling the EN pin low the PG open drain output is high resistive. That means it follows the voltage it is connected to via the pull-up resistor. If the converter is controlled by an external enable signal and the power good should indicate that the output is turned off the application circuit below should be used.




## INPUT OVER VOLTAGE PROTECTION

This converter has a input over voltage protection that protects the device from damage due to a voltage higher than the absolute maximum rating of the input allows. If 6.5 V (typ.) at the input is exceeded the converter completely shuts down to protect its inner circuitry. If the input voltage drops below 6.4 V (typ.) it turns on the device again and enters normal start up.

## LOAD DISCONNECT AND REVERSE CURRENT PROTECTION

Regular boost converters do not disconnect the load from the input supply and therefore a connected battery will be discharge during shutdown. The advantage of TPS61252 is that this converter is disconnecting the output from the input of the power supply when it is disabled. In case of a connected battery it prevents it from being discharge during shutdown of the converter.

## THERMAL REGULATION

The TPS61252 contains a thermal regulation loop that monitors the die temperature. If the die temperature rises to values above 110 °C, the device automatically reduces the current to prevent the die temperature from further increasing. Once the die temperature drops about 10 °C below the threshold, the device will automatically increase the current to the target value. This function also reduces the current during a short-circuit-condition.

## THERMAL SHUTDOWN

As soon as the junction temperature, $T_J$, exceeds 140°C (typical) the device enters thermal shutdown. In this mode, the High Side and Low Side MOSFETs are turned-off. When the junction temperature falls about 20 °C below the thermal shutdown, the device continuous the operation.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# APPLICATION INFORMATION

## EXAMPLE

During the following Application Information section one specific example will be used to define and work with the different equations.

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Input Voltage | $V_{IN}$ | 3.6 | V |
| Minimum Input Voltage | $V_{IN(min)}$ | 2.6 | V |
| Output Voltage | $V_{OUT}$ | 5.0 | V |
| Input Current Limit set by $R_{ILIM}$ | $I_{LIM}$ | 1000 | mA |
| Feedback Voltage | $V_{FB}$ | 1.2 | V |
| Switching Frequency | f | 3.25 | MHz |
| Estimated Efficiency | η | 90 | % |
| Inductor Value of Choice | L1 | 1.0 | µH |

## OUTPUT VOLTAGE SETTING

The output voltage can be calculated by Equation 5:

$$V_{OUT} = V_{FB} \cdot \left(1 + \frac{R_1}{R_2}\right) \quad (5)$$

To minimize the current through the feedback divider network, R2 should be between 180k and 360k. The sum of R1 and R2 should not exceed ~1MΩ, to keep the network robust against noise. Regarding the example, R1 is 768 kΩ and R2 is 240 kΩ.

An external feed forward capacitor C1 is required for optimum load transient response. The value of C1 should be 100pF. The connection from FB pin to the resistor divider should be kept short and away from noise sources, such as the inductor or the SW line.

## INPUT CURRENT LIMIT

The input current limit is set by selecting the correct external resistor value. Equation 6 is a guideline for selecting the correct resistor value:

$$R_{ILIM} = \frac{1.0V}{I_{LIM}} \cdot 10{,}000 \quad (6)$$

For a current limit of 1A the resistor value will be 10 kΩ

## MAXIMUM OUTPUT CURRENT

The maximum output current is set by $R_{ILIM}$ and the input to output voltage ratio and can be calculated by Equation 7:

$$I_{OUT(max)} \approx I_{LIM} \cdot \frac{V_{IN} \cdot \eta}{V_{OUT}} \quad (7)$$

Following the example $I_{OUT(max)}$ will be 648 mA at 3.6 V input voltage and will decrease with lower input voltage values due to the energy conservation.

## INDUCTOR SELECTION

As for all switching power supplies two main passive components are required for storing the energy during operation. This is done by an inductor and an output capacitor. The inductor must be connected between VIN pin and SW pin to make sure that the TPS61252 device operates. To select the right inductor current rating the programmed input current limit as well as the current ripple through the inductor is necessary. An estimation of the maximum peak inductor current can be done using Equation 8.

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$$I_{L(max)} = I_{LIM} + \Delta I_L = I_{LIM} + \frac{V_{IN(min)} \cdot D}{L \cdot f} \quad \text{with} \quad D = 1 - \frac{V_{IN(min)} \cdot \eta}{V_{OUT}} \tag{8}$$

Regarding the above example the current ripple ($\Delta I_L$) will be 426 mA and therefore an inductor with a rated current of about 1.5 A should be used.

The TPS61252 is designed to work with inductor values between 1.0 µH and 2.2 µH. For typical applications a 1.5 µH inductor is recommended. Regarding the conversion factor and the need of a sufficient output current the rated current for the inductor drives into lower inductance values. Therefore the inductor value can be reduced down to 1.0 µH without degrading the stability. Reduced inductance values increase the current ripple that needs to be included in the peak current calculation for the inductor (Equation 8). Using standard boost converters the current through the inductor is defined by the switch current limit of the converters switches and therefore bigger inductors have to be chosen. TPS61252 allows you to reduce the current limit to the needs of the application regardless the maximum switch current limit of the converter. Programming a lower current value allows the use of smaller inductors without the danger to get into saturation.

## OUTPUT CAPACITOR

For the output capacitor, it is recommended to use small ceramic capacitors placed as close as possible to the VOUT and GND pins of the IC. If, for any reason, the application requires the use of large capacitors which cannot be placed close to the IC, a smaller ceramic capacitor in parallel to the large one is highly recommended. This small capacitor should be placed as close as possible to the converters VOUT and GND pins. To get an estimate of the recommended minimum output capacitance, Equation 9 can be used.

$$C_{MIN} = \frac{I_{OUT} \cdot \left(V_{OUT} - V_{IN}\right)}{f \cdot \Delta V \cdot V_{OUT}} \tag{9}$$

Where ΔV is the maximum allowed output ripple.

With a chosen ripple voltage of 10 mV, a minimum effective capacitance of 9.6 µF is needed regarding the example. The total ripple will be larger due to the ESR of the output capacitor. This additional component of the ripple can be calculated using Equation 10

$$V_{ESR} = I_{OUT} \cdot R_{ESR} \tag{10}$$

To maintain control loop stability a capacitor with twice the value (I. e. 22 µF) of the calculated minimum capacitance is required be used due to DC Bias effects. There are no additional requirements regarding minimum ESR. Larger capacitors cause lower output voltage ripple as well as lower output voltage drop during load transients but the total output capacitance value should not exceed values above 50 µF.

## INPUT CAPACITOR

Multilayer ceramic capacitors are an excellent choice for input decoupling of the step-up converter as they have extremely low ESR and are available in small form factors. The input capacitors should be located as close as possible to the device. While a 10µF input capacitor is sufficient for most applications, larger values may be used to reduce input current ripple without limitations. Also low ESR tantalum capacitors may be used.

**NOTE**

**DC Bias effect:** High capacitance ceramic capacitors have a DC Bias effect, which will have a strong influence on the final effective capacitance. Therefore the right capacitor value has to be chosen very carefully. Package size and voltage rating in combination with dielectric material are responsible for differences between the rated capacitor value and the effective capacitance. A 10 V rated 0805 capacitor with 10 µF can have a effective capacitance of less than 5 µF at an output voltage of 5 V.


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## CHECKING LOOP STABILITY

The first step of circuit and stability evaluation is to look from a steady-state perspective at the following signals:

- Switch node, SW
- Inductor current, $I_L$
- Output ripple voltage, $V_{OUT(AC)}$

These are the basic signals that need to be measured when evaluating a switching converter. When the switching waveform shows large duty cycle jitter or the output voltage or inductor current shows oscillations, the regulation loop may be unstable. This is often a result of board layout and/or L-C combination.

As the next step in the evaluation of the regulation loop, the load transient response is tested. The time between the load transient takes place and the turn on of the PMOS switch, the output capacitor must supply all of the current required by the load. $V_{OUT}$ immediately shifts by an amount equal to $\Delta I_{(LOAD)}$ x ESR, where ESR is the effective series resistance of $C_{OUT}$. $\Delta I_{(LOAD)}$ begins to charge or discharge $C_{OUT}$ generating a feedback error signal used by the regulator to return $V_{OUT}$ to its steady-state value. The results are most easily interpreted when the device operates in PWM mode.

During this recovery time, $V_{OUT}$ can be monitored for settling time, overshoot or ringing that helps judge the converter's stability. Without any ringing, the loop has usually more than 60° of phase margin. Because the damping factor of the circuitry is directly related to several resistive parameters (e.g., MOSFET $r_{DS(on)}$) that are temperature dependant, the loop stability analysis has to be done over the input voltage range, load current range, and temperature range.

## LAYOUT CONSIDERATIONS

For all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks. The input capacitor, output capacitor, and the inductor should be placed as close as possible to the IC. Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at any place close to one of the ground pins of the IC.

The feedback divider should be placed close to the IC to keep the feedback connection short. To lay out the ground, short traces and wide are recommended. This avoids ground shift problems, which can occur due to superimposition of power ground current and the feedback divider.

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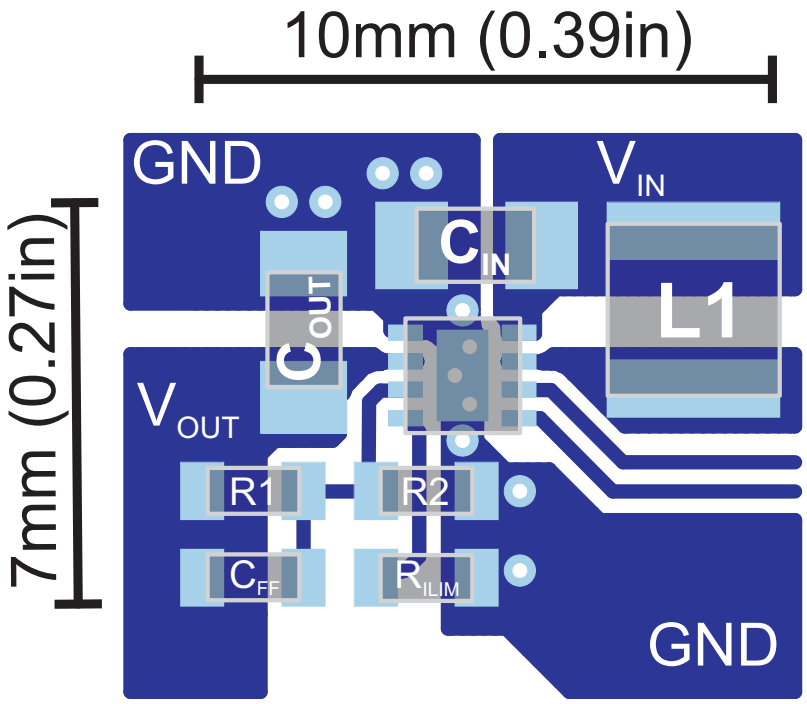


**Figure 11. Suggested Layout (Top)**

## THERMAL INFORMATION

The implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
  - E.g. increase of the GND plane on the top layer which is connected to the exposed thermal pad
  - Use thicker cupper layer
- Improving the thermal coupling of the component to the PCB
- Introducing airflow in the system

Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design. The maximum junction temperature ($T_J$) of the TPS61252 is 150°C.


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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS61252DGST | PREVIEW | WSON | DSG | 8 | 250 | TBD | Call TI | Call TI | -40 to 85 | | |
| TPS61252DSGR | ACTIVE | WSON | DSG | 8 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | QTI | Samples |
| TPS61252DSGT | ACTIVE | WSON | DSG | 8 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | | QTI | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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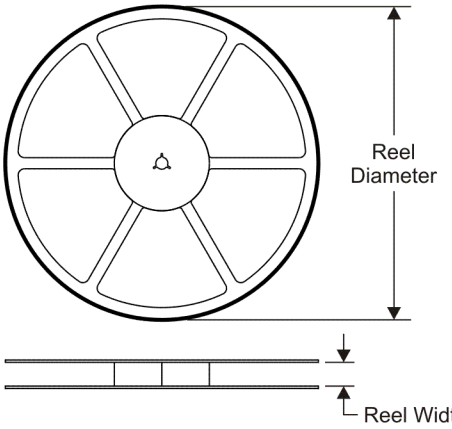
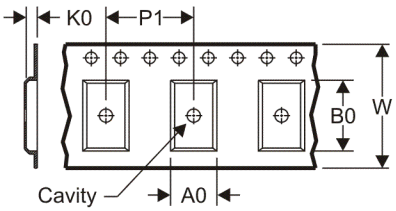
## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

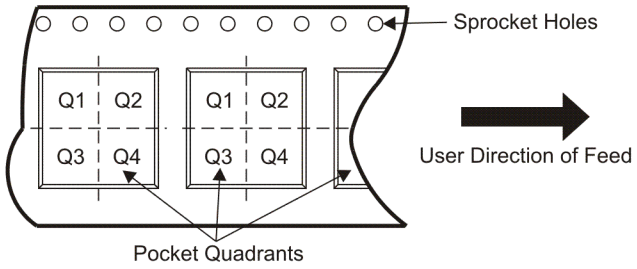



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

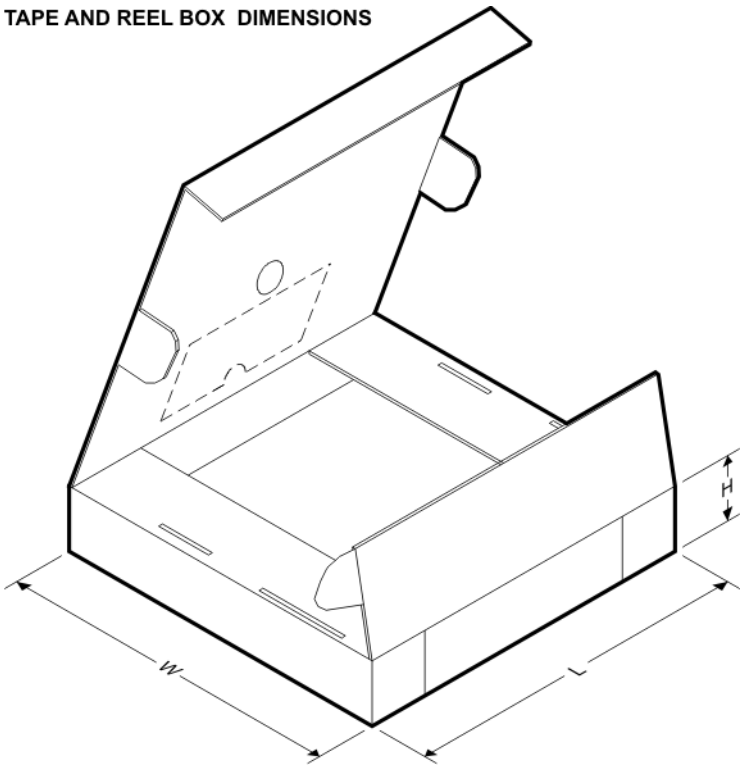
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS61252DSGR | WSON | DSG | 8 | 3000 | 179.0 | 8.4 | 2.2 | 2.2 | 1.2 | 4.0 | 8.0 | Q2 |
| TPS61252DSGT | WSON | DSG | 8 | 250 | 179.0 | 8.4 | 2.2 | 2.2 | 1.2 | 4.0 | 8.0 | Q2 |

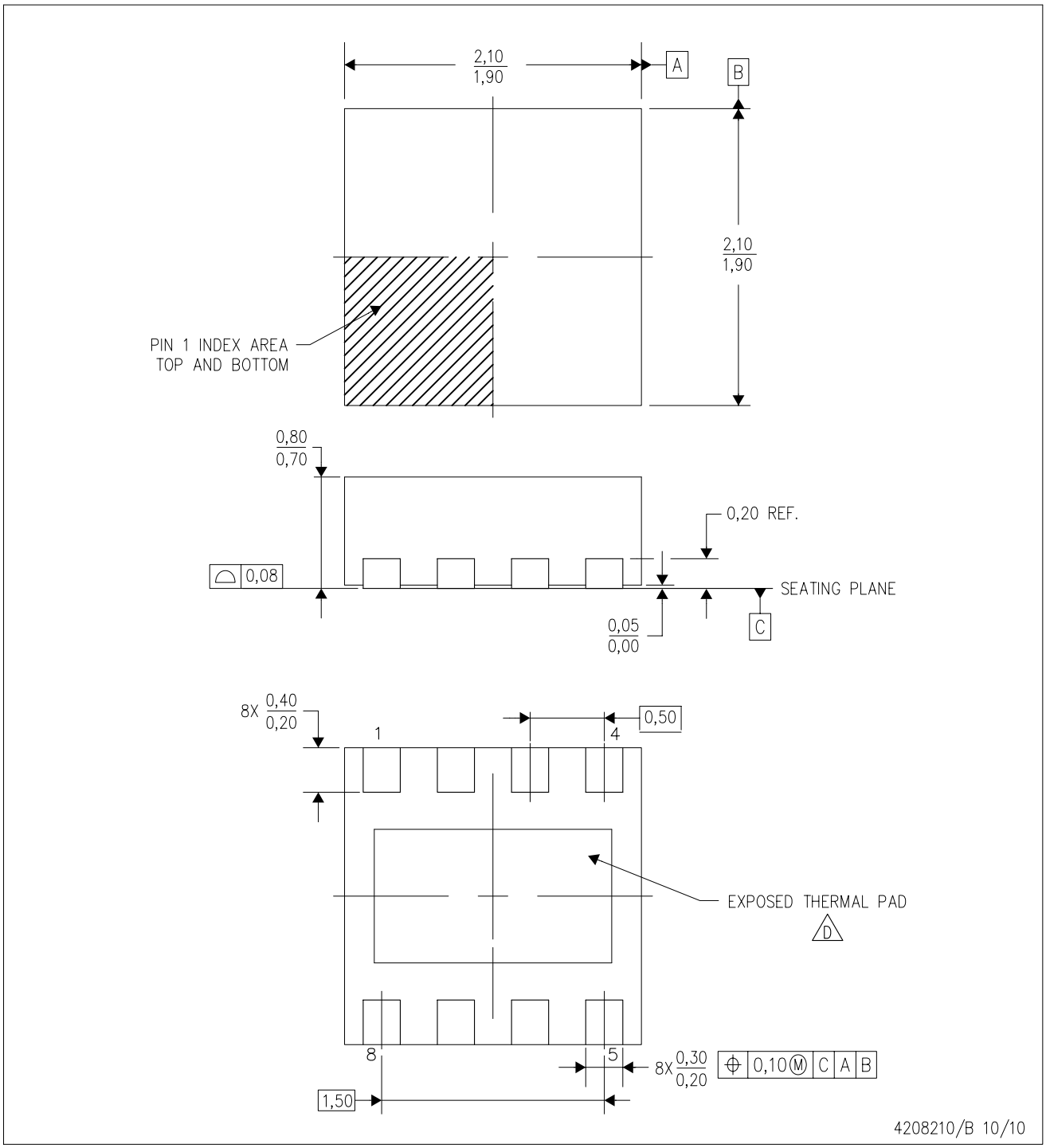
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS61252DSGR | WSON | DSG | 8 | 3000 | 195.0 | 200.0 | 45.0 |
| TPS61252DSGT | WSON | DSG | 8 | 250 | 195.0 | 200.0 | 45.0 |

DSG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–229.

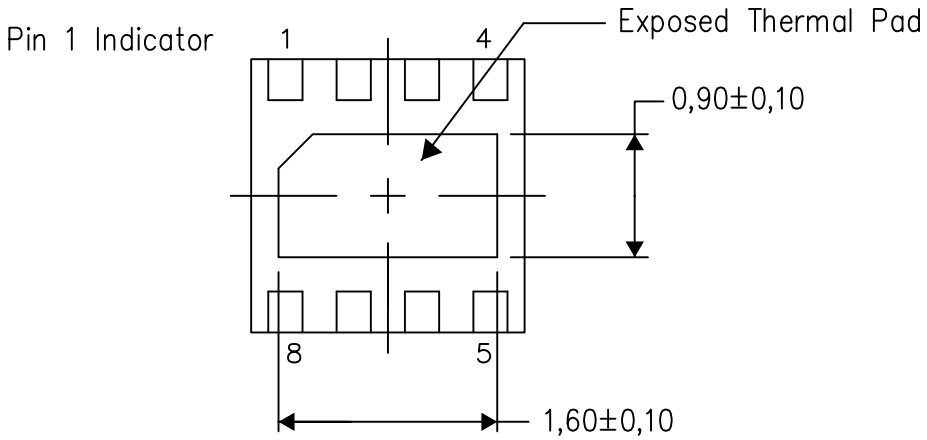
DSG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



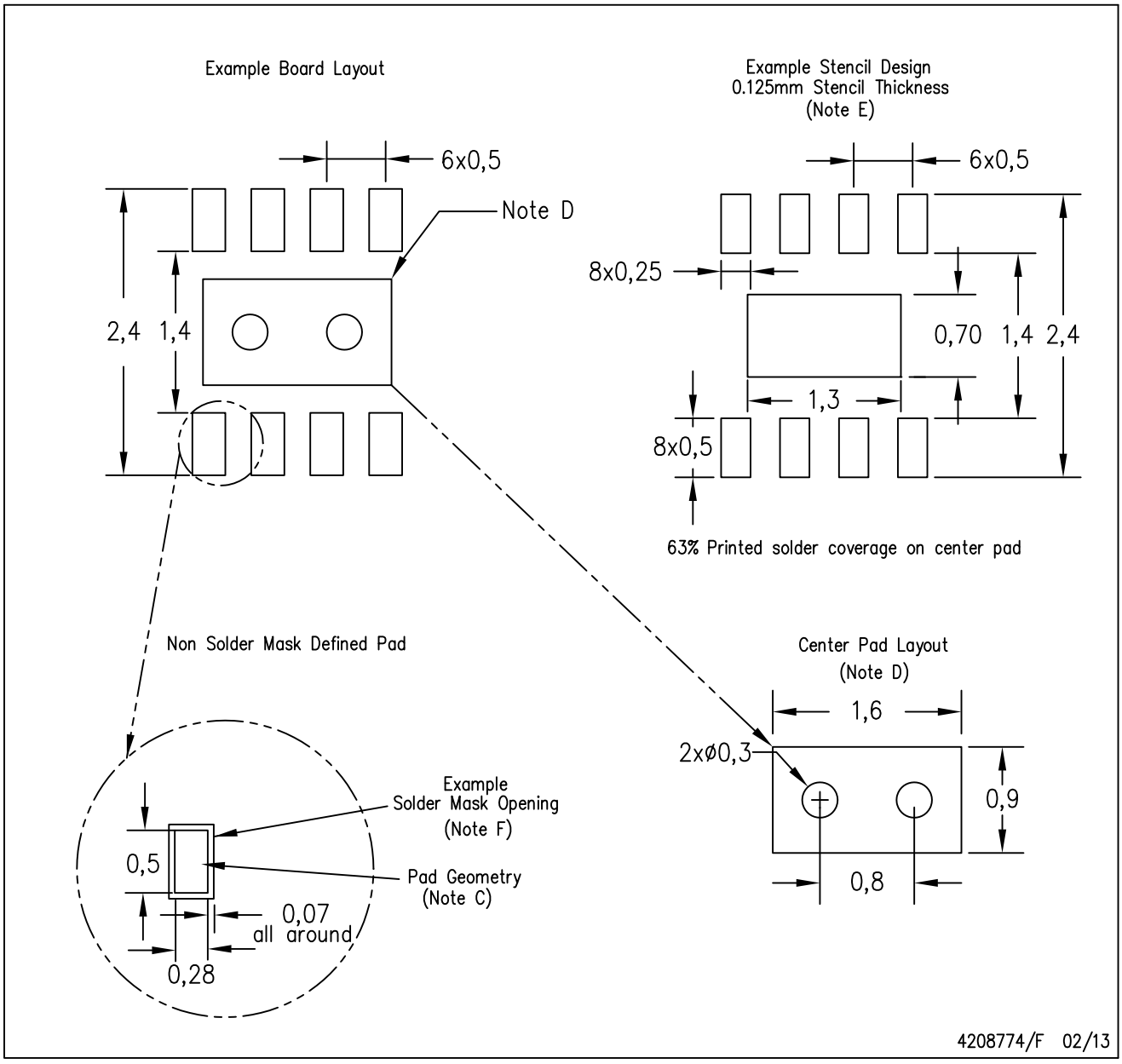

Bottom View

Exposed Thermal Pad Dimensions

4208347/G 08/13

NOTE: All linear dimensions are in millimeters

DSG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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