

ULTRA-SMALL, LOW-INPUT VOLTAGE, LOW R_{ON} LOAD SWITCH

Check for Samples: [TPS22907](#)

FEATURES

- Low Input Voltage: 1.1 V to 3.6 V
- Ultra-Low On-State Resistance (R_{ON})
- Typical R_{ON} values
 - $R_{ON} = 44\text{ m}\Omega$ at $V_{IN} = 3.6\text{ V}$
 - $R_{ON} = 50\text{ m}\Omega$ at $V_{IN} = 2.5\text{ V}$
 - $R_{ON} = 58\text{ m}\Omega$ at $V_{IN} = 1.8\text{ V}$
 - $R_{ON} = 83\text{ m}\Omega$ at $V_{IN} = 1.2\text{ V}$
- 1-A Maximum Continuous Switch Current
- Maximum Quiescent Current $< 1\text{ }\mu\text{A}$
- Maximum Shutdown Current $< 1\text{ }\mu\text{A}$
- Low Control Input Thresholds Enable Use of Low-Voltage Logic
- Controlled Slew Rate to Avoid Inrush Currents
- ESD Performance Tested Per JESD 22
 - 3000 V Human-Body Model (A114-B, Class II)
 - 1000 V Charged-Device Model (C101)
- Ultra-Small Four-Terminal Wafer-Chip-Scale Package (WCSP)
 - Nominal Dimensions Shown – See Addendum for Details
 - 0.9 mm \times 0.9 mm
 - 0.5-mm Pitch, 0.5-mm Height

APPLICATIONS

- Battery Powered Equipment
- Portable Industrial Equipment
- Portable Medical Equipment
- Portable Media Players
- Point of Sale Terminal
- GPS Devices
- Digital Cameras
- Portable Instrumentation
- Smartphones / Tablets

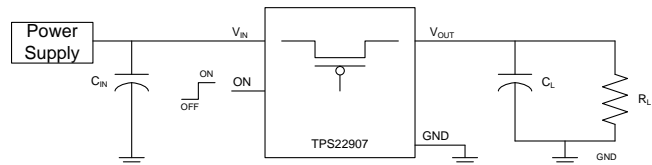


Figure 1. Typical Application

DESCRIPTION

The TPS22907 is an ultra-small, low R_{ON} load switch with controlled turn on. The device contains a P-channel MOSFET that operates over an input voltage range of 1.1 V to 3.6 V. The switch is controlled by an on/off input (ON), which is capable of interfacing directly with low-voltage control signals.

The TPS22907 is available in a space-saving 4-terminal WCSP with 0.5-mm pitch (YZT). The device is characterized for operation over the free-air temperature range of -40°C to 85°C .

Table 1. Device Feature List

DEVICE	R_{ON} (Typical) $V_{IN} = 1.8\text{ V}$	SLEW RATE (Typical) $V_{IN} = 1.8\text{ V}$	MAXIMUM OUTPUT CURRENT	ENABLE
TPS22907	58 m Ω	36 μs	1 A	Active high



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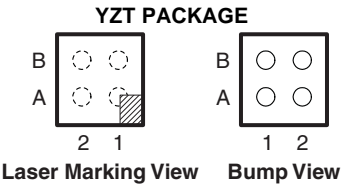
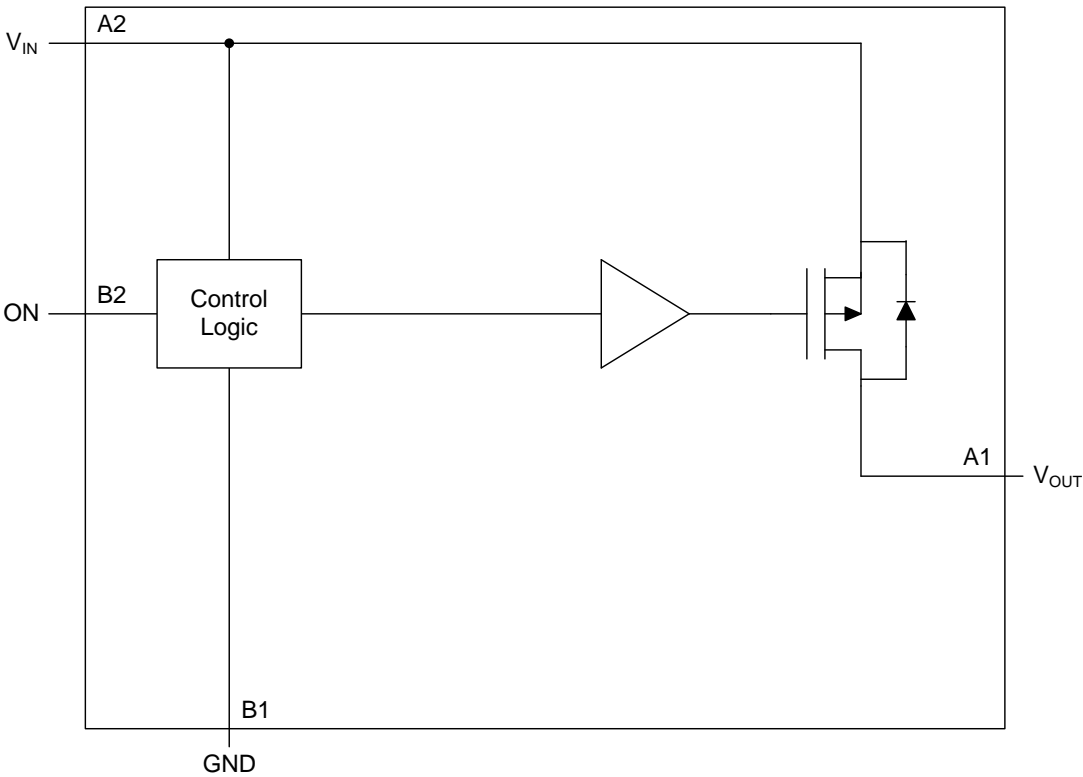


This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

For detailed ordering information, see the *PACKAGE OPTION ADDENDUM* section at the end of this data sheet.

FUNCTIONAL BLOCK DIAGRAM



FUNCTION TABLE

ON (Control Input)	V _{IN} to V _{OUT}
L	OFF
H	ON

TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
BALL NO.	NAME	
A1	V _{OUT}	Switch output
A2	V _{IN}	Switch input, bypass capacitor recommended for minimizing V _{IN} dip. See Application Information.
B1	GND	Ground
B2	ON	Switch control input, active high. Do not leave floating.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

		VALUE	UNIT
V _{IN}	Input voltage range	–0.3 to 4	V
V _{OUT}	Output voltage range	–0.3 to (V _{IN} + 0.3)	V
V _{ON}	Input voltage range	–0.3 to 4	V
I _{MAX}	Maximum continuous switch current, T _A = –40°C to 85°C	1	A
I _{PLS}	Maximum pulsed current (100-μs pulse, 2% duty cycle), T _A = –40°C to 85°C	2.7	A
T _A	Operating free-air temperature range	–40 to 85	°C
T _J	Maximum junction temperature	125	°C
T _{STG}	Storage temperature range	–65 to 150	°C
T _{LEAD}	Maximum lead temperature (10-s soldering time)	300	°C
ESD	Electrostatic discharge protection	Human-Body Model (HBM)	V
		Charged-Device Model (CDM)	
		3000	
		1000	

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC ⁽¹⁾⁽²⁾		TPS22907	UNITS
		YZT (4 PINS)	
Θ _{JA}	Junction-to-ambient thermal resistance	189.4	°C/W
Θ _{JC(top)}	Junction-to-case(top) thermal resistance	1.9	
Θ _{JB}	Junction-to-board thermal resistance	37.2	
Ψ _{JT}	Junction-to-top characterization parameter	10.2	
Ψ _{JB}	Junction-to-board characterization parameter	37	
Θ _{JC(bottom)}	Junction-to-case(bottom) thermal resistance	N/A	

- (1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, [SPRA953](#)

- (2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V _{IN}	Input voltage range	1.1	3.6	V
V _{OUT}	Output voltage range		V _{IN}	V
V _{IH}	High-level input voltage, ON	0.85	3.6	V
V _{IL}	Low-level input voltage, ON		0.4	V
C _{IN}	Input capacitor	1 ⁽¹⁾		μF

- (1) See [Application Information](#).

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, the specification applies over the operating ambient temperature $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ and $V_{\text{IN}} = 1.1\text{ V}$ to 3.6 V . Typical values are for $V_{\text{IN}} = 3.6\text{ V}$ and $T_A = 25^{\circ}\text{C}$.

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
I_{IN}	Quiescent current	$I_{\text{OUT}} = 0\text{ mA}$, $V_{\text{IN}} = V_{\text{ON}}$			0.07	1	μA
$I_{\text{IN(OFF)}}$	Off supply current	$V_{\text{ON}} = 0\text{ V}$, $\text{OUT} = \text{Open}$			0.05	1	μA
$I_{\text{IN(LEAKAGE)}}$	Leakage current	$V_{\text{ON}} = 0\text{ V}$, $V_{\text{OUT}} = 0\text{ V}$			0.05	1	μA
R_{ON}	ON-state resistance	$V_{\text{IN}} = 3.6\text{ V}$, $I_{\text{OUT}} = -200\text{ mA}$	25°C		44	60	$\text{m}\Omega$
			Full range			67	
		$V_{\text{IN}} = 2.5\text{ V}$, $I_{\text{OUT}} = -200\text{ mA}$	25°C		50	63	
			Full range			70	
		$V_{\text{IN}} = 1.8\text{ V}$, $I_{\text{OUT}} = -200\text{ mA}$	25°C		58	72	
			Full range			80	
		$V_{\text{IN}} = 1.2\text{ V}$, $I_{\text{OUT}} = -200\text{ mA}$	25°C		83	106	
			Full range			117	
		$V_{\text{IN}} = 1.1\text{ V}$, $I_{\text{OUT}} = -200\text{ mA}$	25°C		97	125	
			Full range			140	
I_{ON}	ON input leakage current	$V_{\text{ON}} = 1.1\text{ V}$ to 3.6 V or 0 V	Full range		0.005	1	μA

SWITCHING CHARACTERISTICS

$V_{\text{IN}} = 3.6\text{ V}$, $T_A = 25^{\circ}\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{ON}	Turn-ON time	$R_L = 500\ \Omega$	$C_L = 0.1\ \mu\text{F}$		28		μs
t_{OFF}	Turn-OFF time	$R_L = 500\ \Omega$	$C_L = 0.1\ \mu\text{F}$		40		μs
t_r	V_{OUT} rise time	$R_L = 500\ \Omega$	$C_L = 0.1\ \mu\text{F}$		25		μs
t_f	V_{OUT} fall time	$R_L = 500\ \Omega$	$C_L = 0.1\ \mu\text{F}$		116		μs

SWITCHING CHARACTERISTICS

$V_{\text{IN}} = 1.8\text{ V}$, $T_A = 25^{\circ}\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{ON}	Turn-ON time	$R_L = 500\ \Omega$	$C_L = 0.1\ \mu\text{F}$		48		μs
t_{OFF}	Turn-OFF time	$R_L = 500\ \Omega$	$C_L = 0.1\ \mu\text{F}$		40		μs
t_r	V_{OUT} rise time	$R_L = 500\ \Omega$	$C_L = 0.1\ \mu\text{F}$		36		μs
t_f	V_{OUT} fall time	$R_L = 500\ \Omega$	$C_L = 0.1\ \mu\text{F}$		113		μs

SWITCHING CHARACTERISTICS

$V_{\text{IN}} = 1.1\text{ V}$, $T_A = 25^{\circ}\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{ON}	Turn-ON time	$R_L = 500\ \Omega$	$C_L = 0.1\ \mu\text{F}$		81		μs
t_{OFF}	Turn-OFF time	$R_L = 500\ \Omega$	$C_L = 0.1\ \mu\text{F}$		42		μs
t_r	V_{OUT} rise time	$R_L = 500\ \Omega$	$C_L = 0.1\ \mu\text{F}$		57		μs
t_f	V_{OUT} fall time	$R_L = 500\ \Omega$	$C_L = 0.1\ \mu\text{F}$		113		μs

TYPICAL CHARACTERISTICS

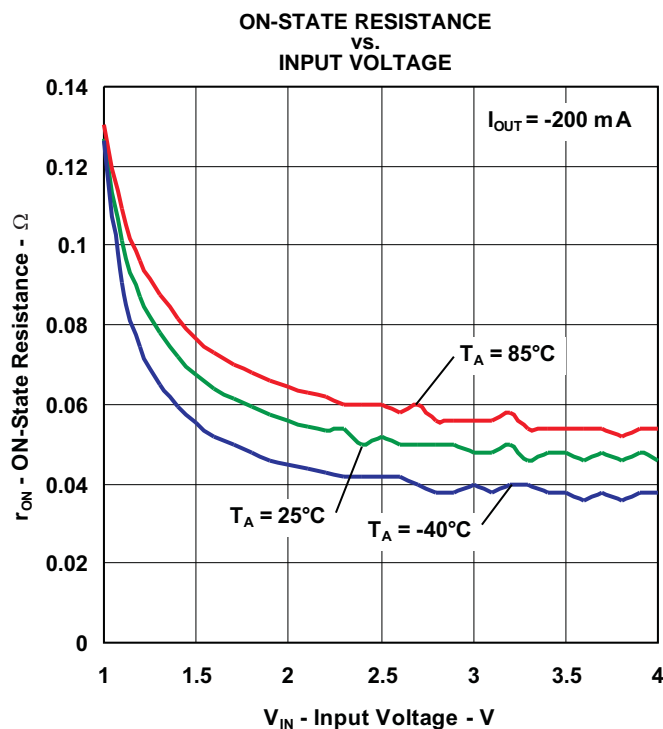


Figure 2.

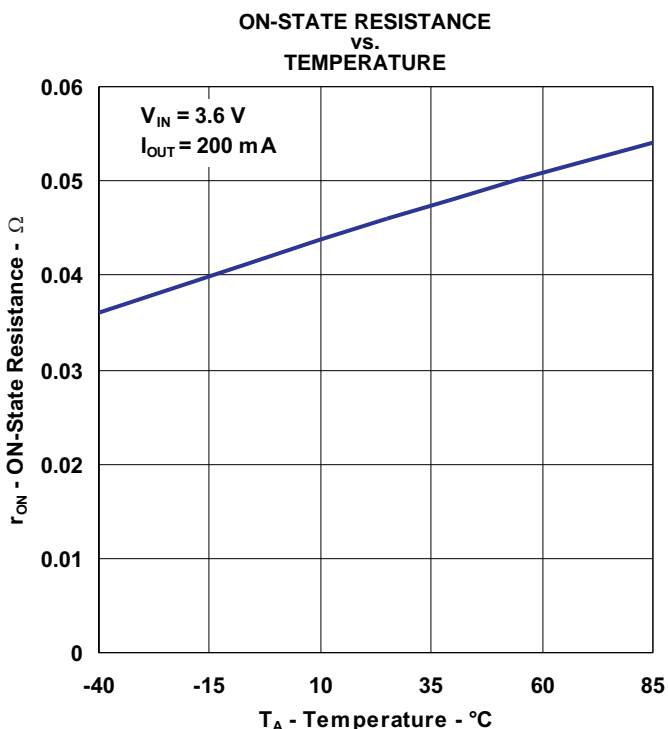


Figure 3.

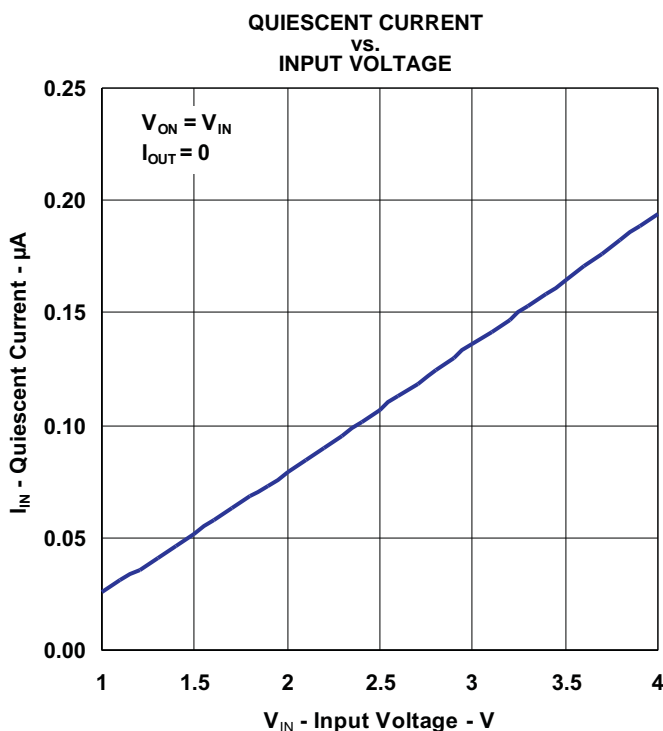


Figure 4.

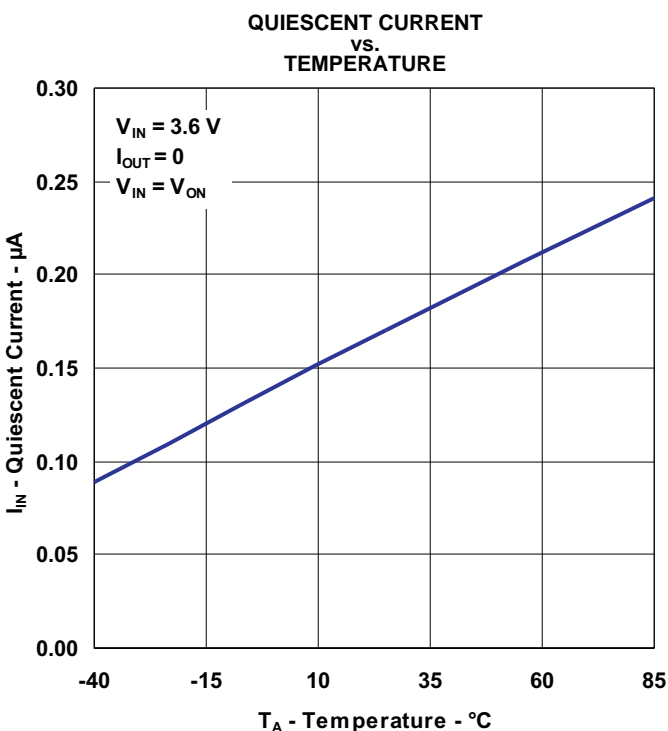


Figure 5.

TYPICAL CHARACTERISTICS (continued)

OFF SUPPLY CURRENT
vs.
INPUT VOLTAGE

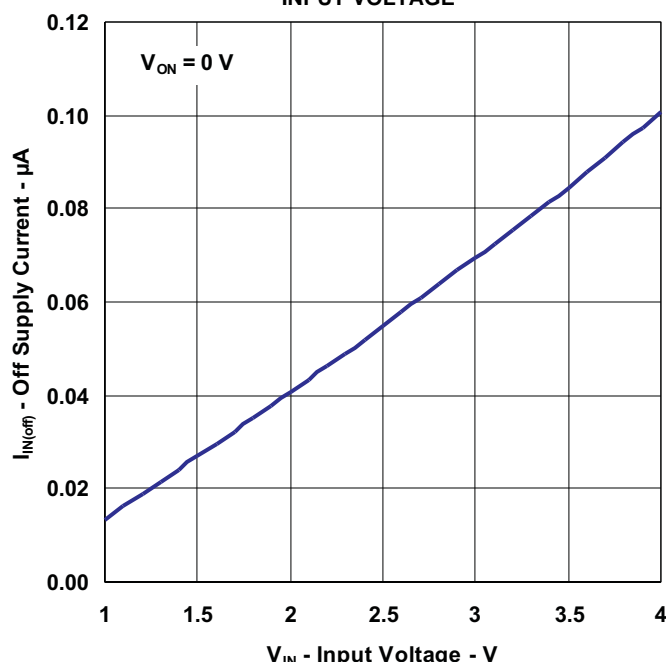


Figure 6.

OFF SUPPLY CURRENT
vs.
TEMPERATURE

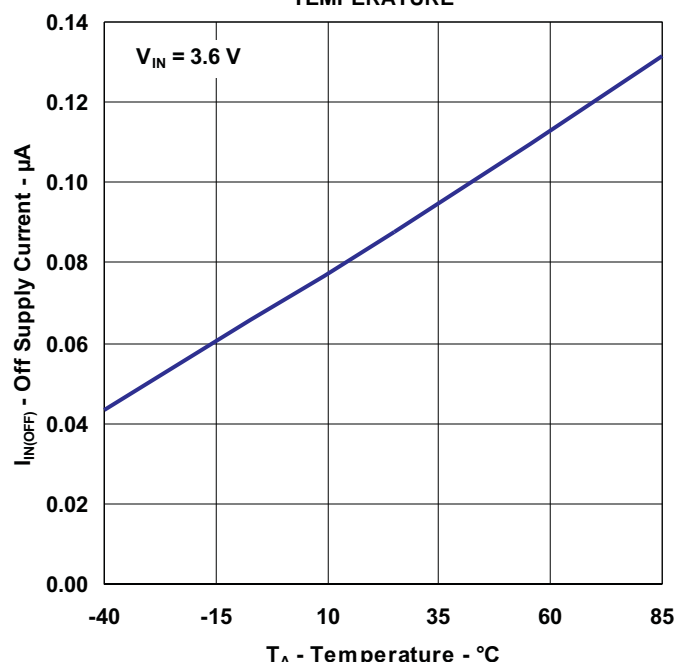


Figure 7.

LEAKAGE CURRENT
vs.
INPUT VOLTAGE

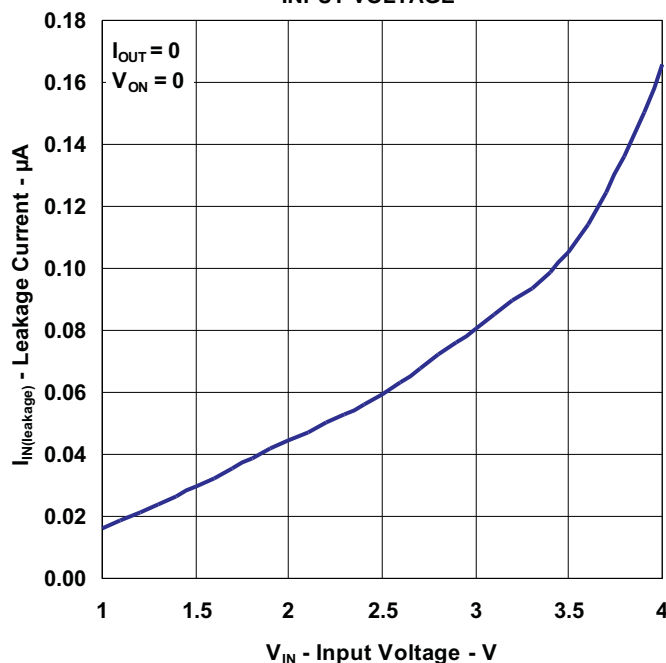


Figure 8.

LEAKAGE CURRENT
vs.
TEMPERATURE

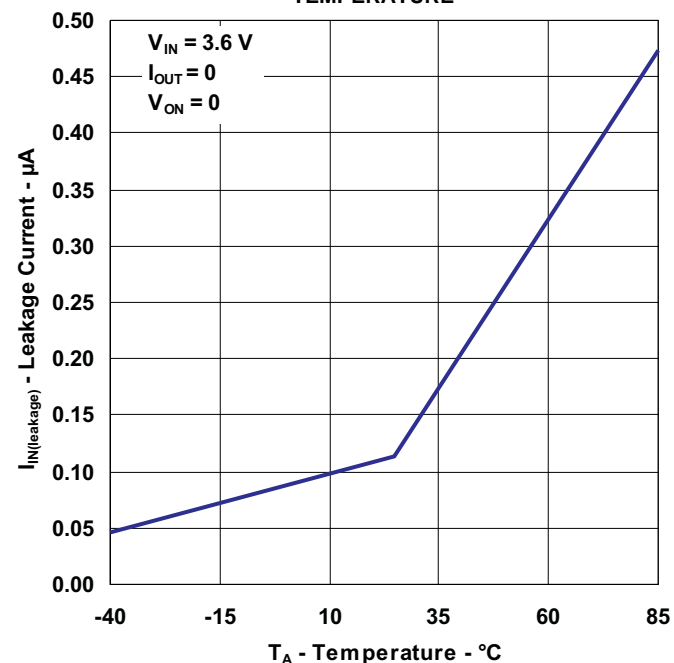


Figure 9.

TYPICAL CHARACTERISTICS (continued) ON INPUT THRESHOLD

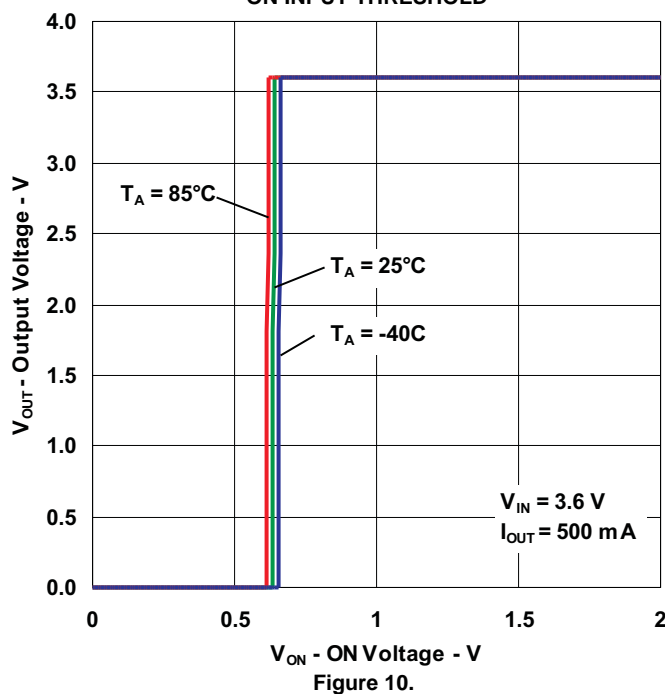


Figure 10.

ON TIME vs. TEMPERATURE

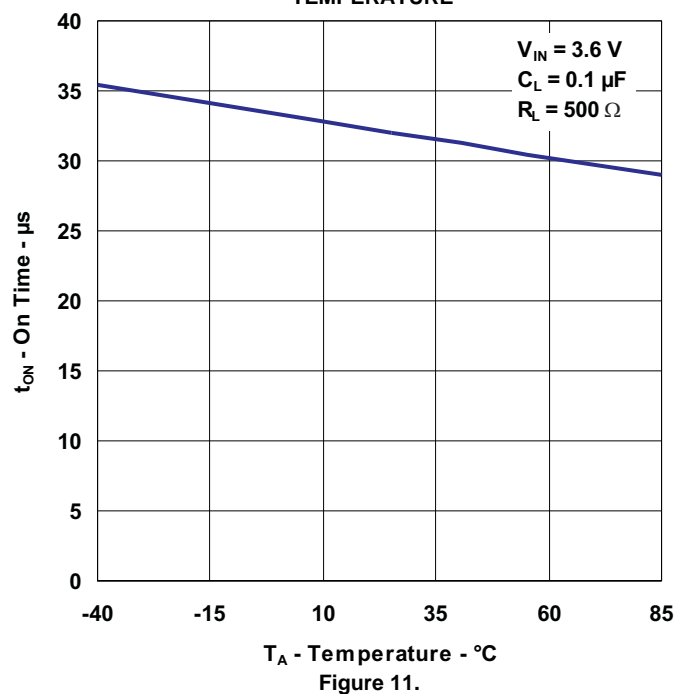


Figure 11.

OFF TIME vs. TEMPERATURE

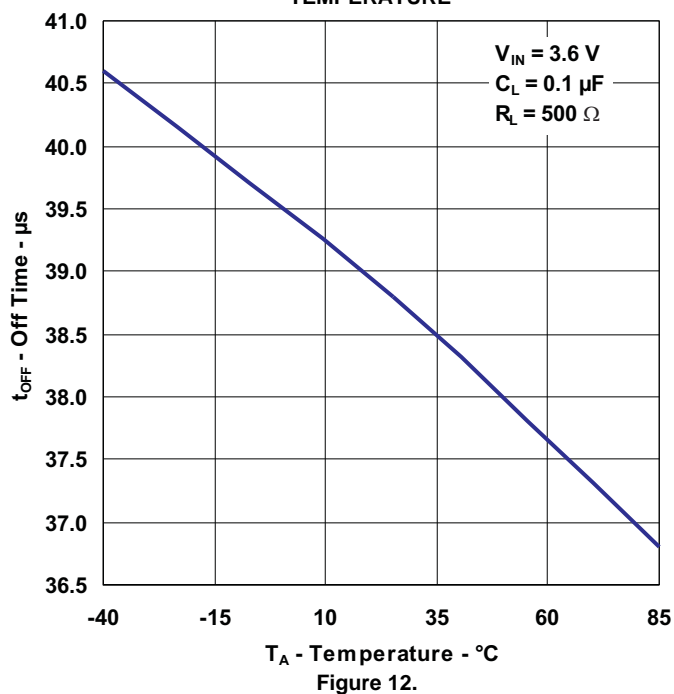


Figure 12.

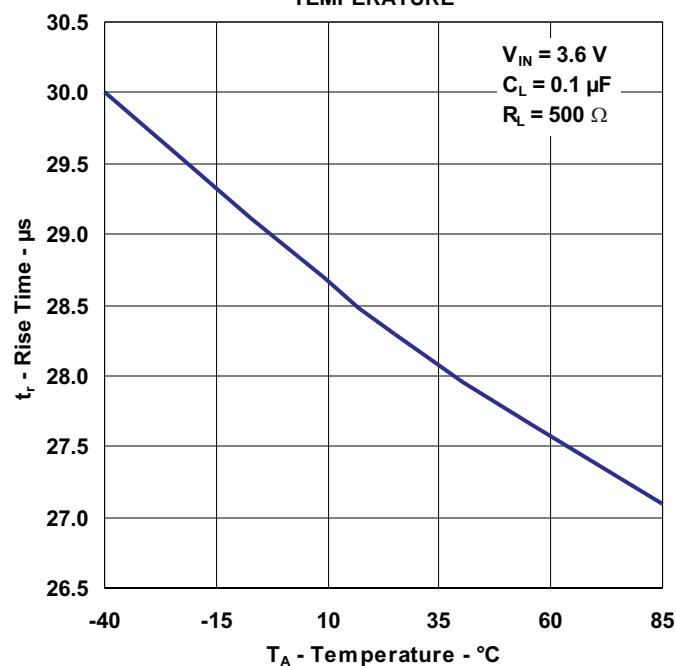
TYPICAL CHARACTERISTICS (continued)**RISE TIME
vs.
TEMPERATURE**

Figure 13.

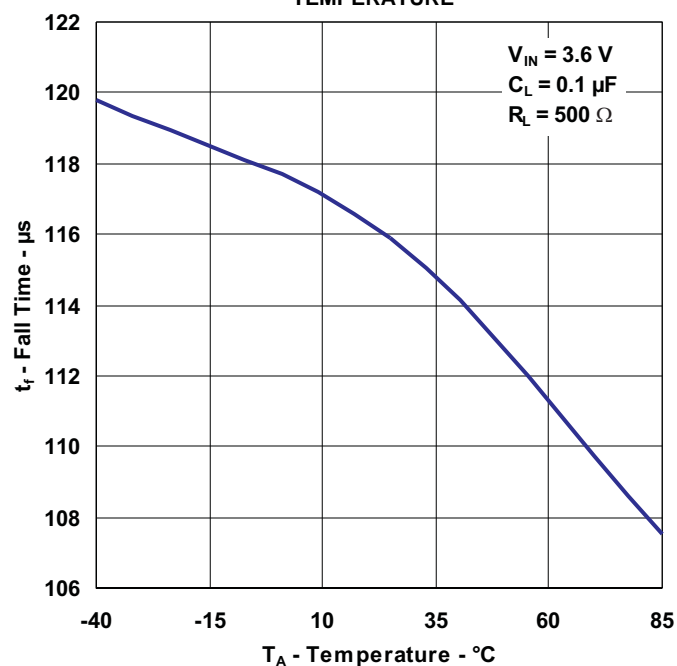
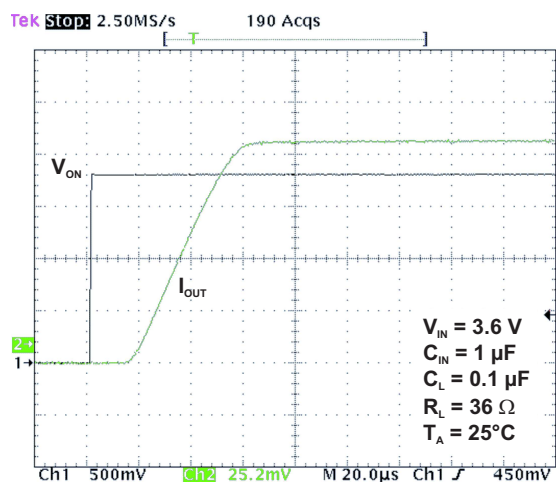
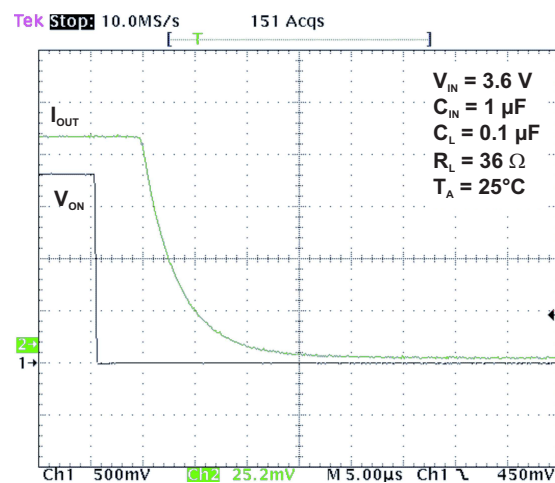
**FALL TIME
vs.
TEMPERATURE**

Figure 14.

Figure 15. t_{ON} RESPONSEFigure 16. t_{OFF} RESPONSE

TYPICAL CHARACTERISTICS (continued)

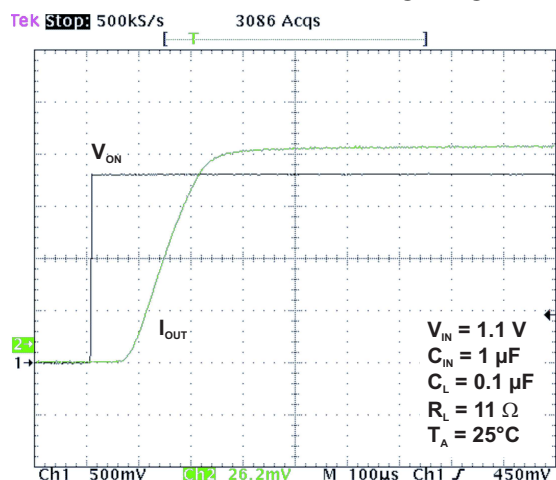


Figure 17. t_{ON} RESPONSE

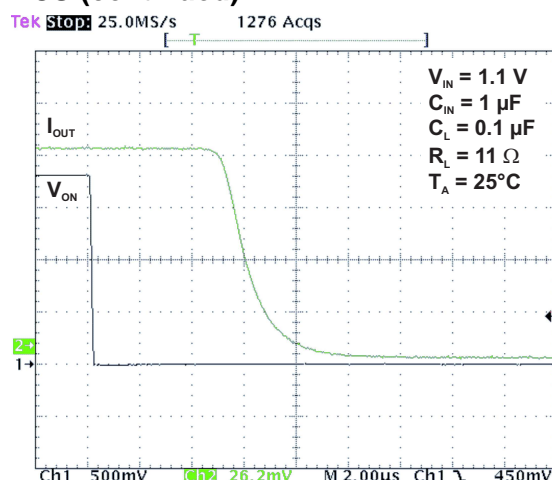


Figure 18. t_{OFF} RESPONSE

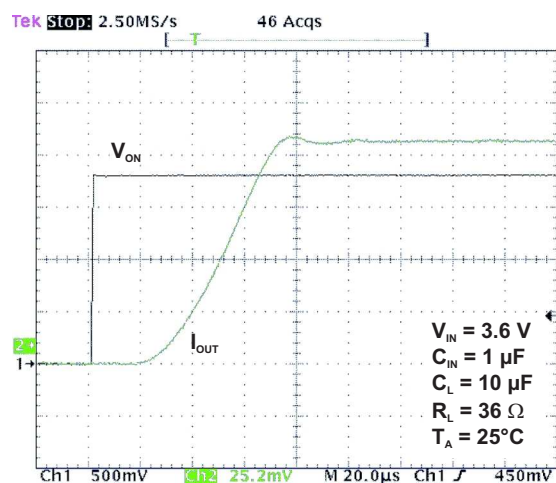


Figure 19. t_{ON} RESPONSE

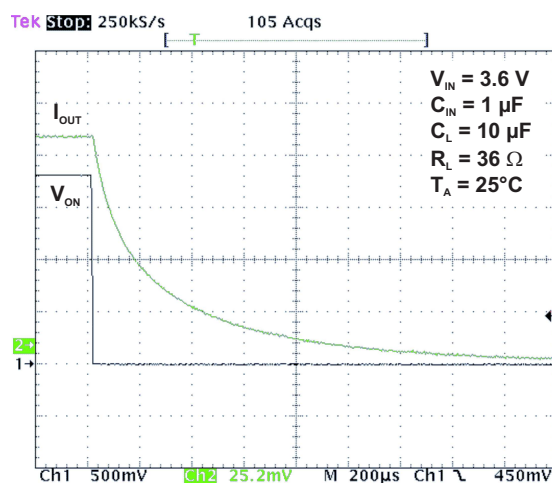


Figure 20. t_{OFF} RESPONSE

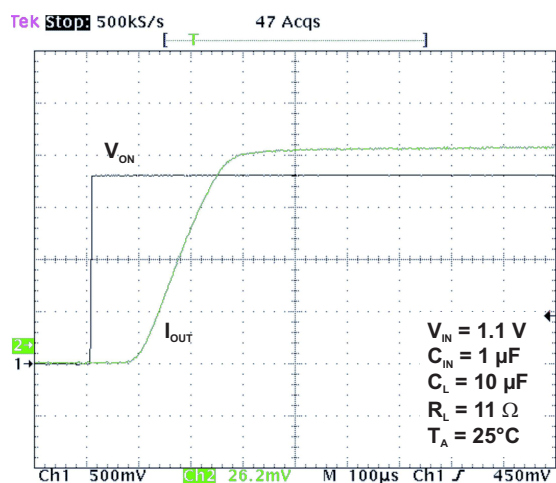


Figure 21. t_{ON} RESPONSE

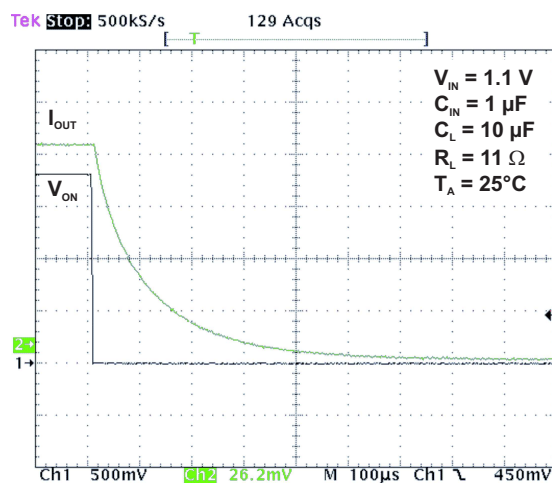
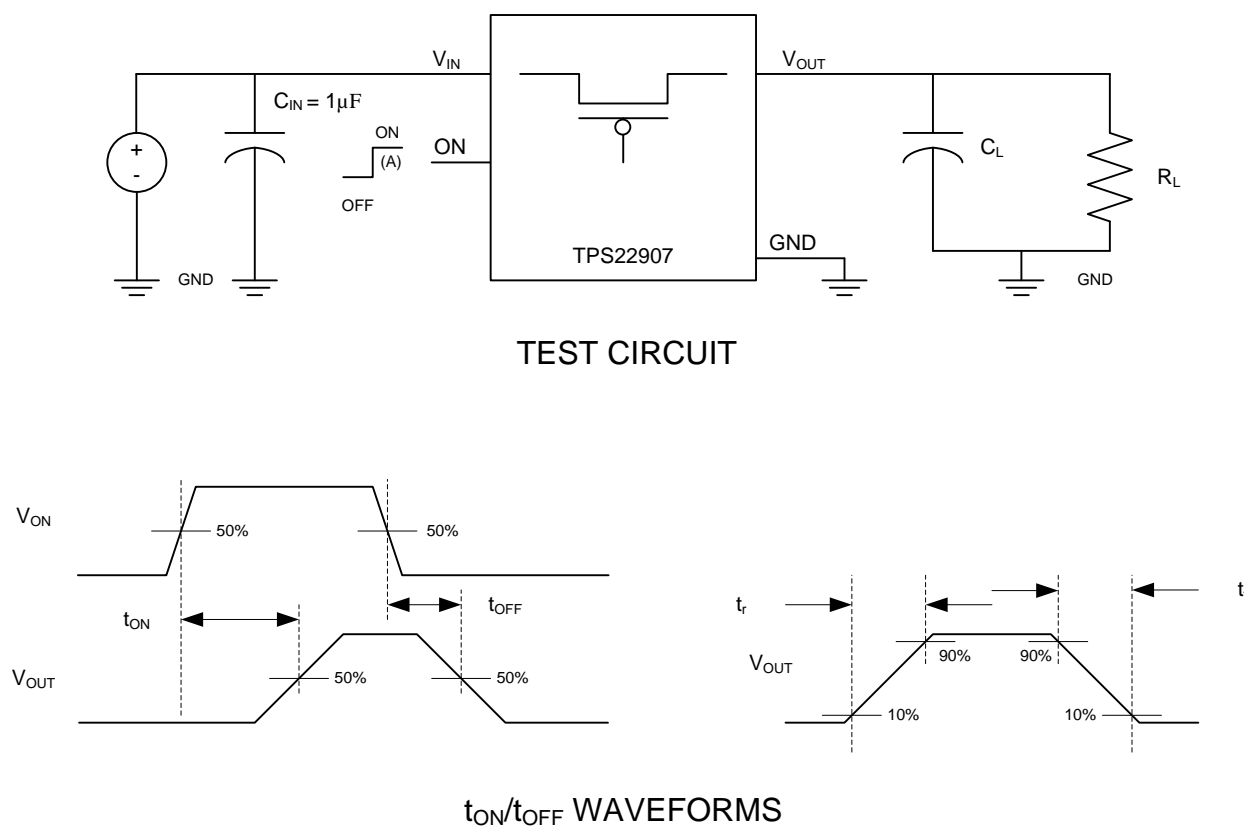


Figure 22. t_{OFF} RESPONSE

SWITCHING CHARACTERISTIC MEASUREMENT INFORMATION



(A) Control signal rise and fall times are 100ns.

Figure 23. Test Circuit and t_{ON}/t_{OFF} Waveforms

APPLICATION INFORMATION

On/Off Control

The ON pin controls the state of the switch. Asserting ON high enables the switch. ON is active high and has a low threshold, making it capable of interfacing with low-voltage signals. The ON pin is compatible with standard GPIO logic threshold. It can be used with any microcontroller with 1.2-V, 1.8-V, 2.5-V, or 3.3-V GPIOs.

Input Capacitor

To limit the voltage drop on the input supply caused by transient inrush currents when the switch turns on into a discharged load capacitor or short-circuit, a capacitor needs to be placed between V_{IN} and GND. A 1- μ F ceramic capacitor, C_{IN} , placed close to the pins is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop during high-current application. When switching heavy loads, it is recommended to have an input capacitor approximately ten times higher than the output capacitor to avoid excessive voltage drop.

Output Capacitor

Due to the integrated body diode in the PMOS switch, a C_{IN} greater than C_L is highly recommended. A C_L greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from V_{OUT} to V_{IN} . A C_{IN} to C_L ratio of at least 10 to 1 is recommended for minimizing V_{IN} dip caused by inrush currents during startup; however, a 10 to 1 ratio for capacitance is not required for proper functionality of the device. A ratio smaller than 10 to 1 (such as 1 to 1) could cause slightly more V_{IN} dip at turn on due to inrush currents.

Board Layout

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for V_{IN} , V_{OUT} , and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

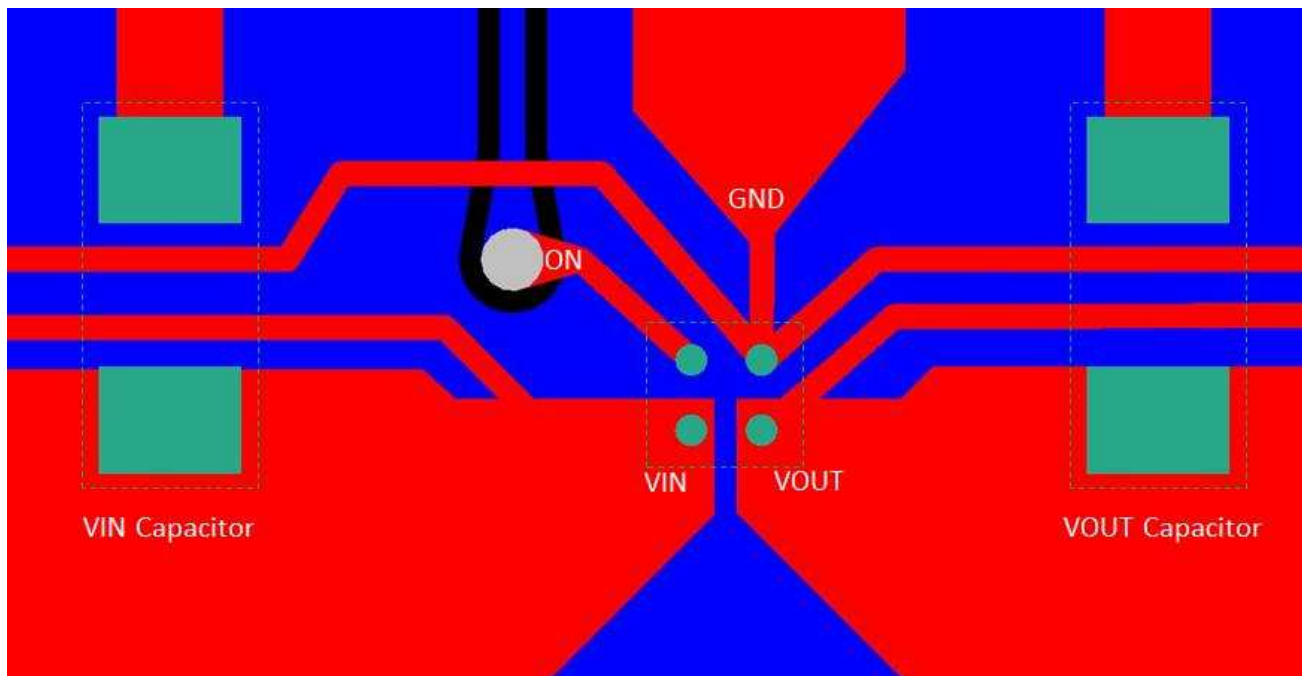


Figure 24. Example Layout for the TPS22907

REVISION HISTORY

Changes from Original (November 2009) to Revision A	Page
• Changed Feature From: Ultra-Low ON-State Resistance To: Ultra-Low ON-State Resistance (R_{ON})	1
• Changed the Feature for the Wafer-Chip-Scale Package	1
• Changed Application From: Point Of Sales Terminal To: Point of Sale Terminal	1
• Changed Application From: Smartphones To: Smartphones / Tablets	1
• Changed Table 1 , Device Feature List	1
• Deleted the ORDERING INFORMATION table	1
• Changed the I_{IN} Test Condition From: $I_{OUT} = 0$ To $I_{OUT} = 0mA$	4
• Changed the $I_{IN(OFF)}$ Test Condition From: $V_{ON} = GND$ To $V_{ON} = 0V$	4
• Changed the $I_{IN(LEAKAGE)}$ Test Condition From: $V_{ON} = GND$, $V_{OUT} = 0$ To $V_{ON} = 0V$, $V_{OUT} = 0V$	4

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22907YZTR	ACTIVE	DSBGA	YZT	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	5K (F ~ G)	Samples
TPS22907YZTT	ACTIVE	DSBGA	YZT	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	5K (F ~ G)	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

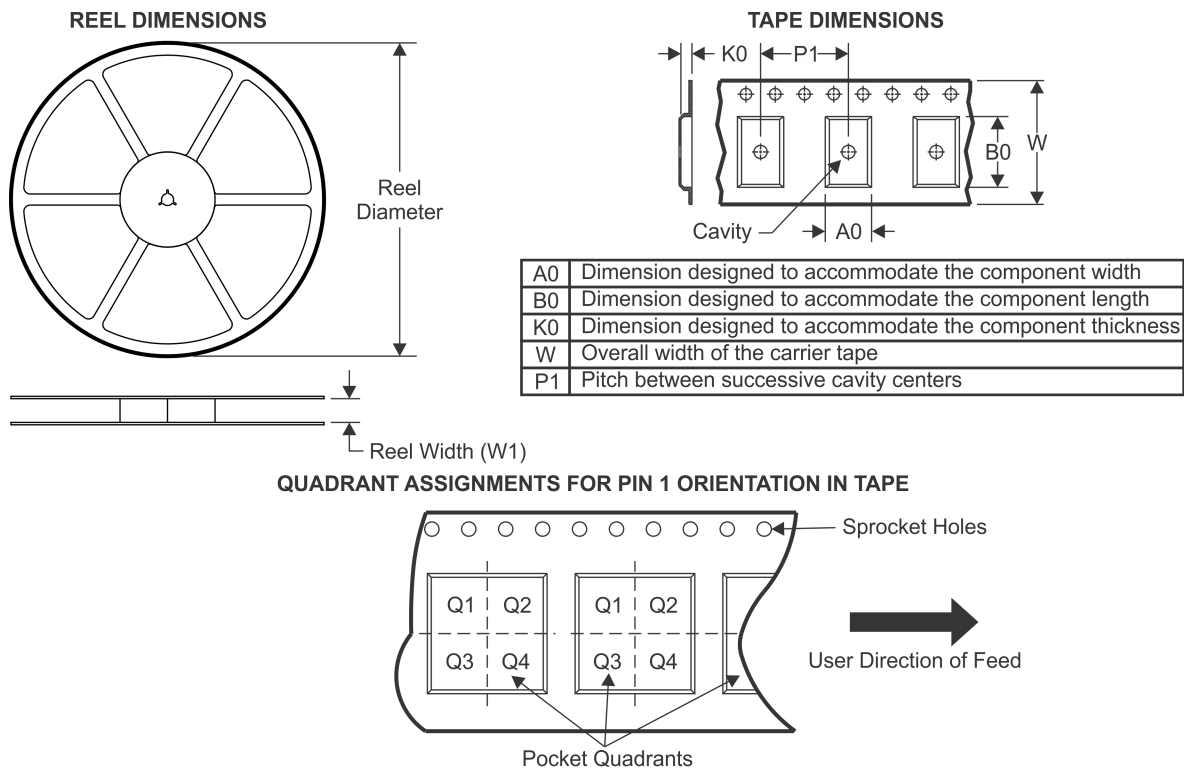
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22907YZTR	DSBGA	YZT	4	3000	178.0	9.2	1.0	1.0	0.73	4.0	8.0	Q1
TPS22907YZTT	DSBGA	YZT	4	250	178.0	9.2	1.0	1.0	0.73	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

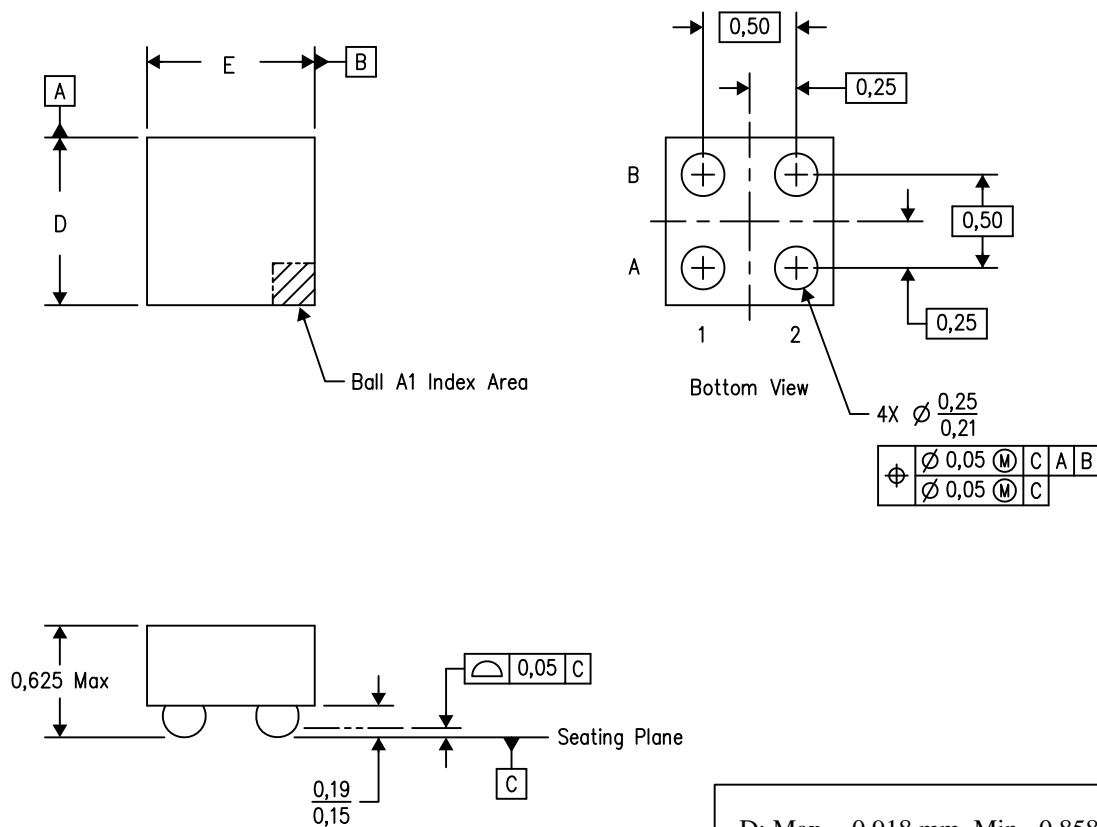


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22907YZTR	DSBGA	YZT	4	3000	220.0	220.0	35.0
TPS22907YZTT	DSBGA	YZT	4	250	220.0	220.0	35.0

YZT (S-XBGA-N4)

DIE-SIZE BALL GRID ARRAY



D: Max = 0.918 mm, Min = 0.858 mm

E: Max = 0.918 mm, Min = 0.858 mm

4205418-2/H 05/13

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.

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