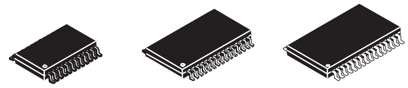

PC CARD™ POWER-INTERFACE SWITCH WITH RESET FOR SERIAL PCMCIA CONTROLLER

FEATURES

- **Fully Integrated V_{CC} and V_{PP} Switching for Single-Slot or Dual-Slot PC Card™ Interface**
- **P^2C™ 3-Lead Serial Interface Compatible With CardBus™ Controller**
- **Meets PC Card Standard**
- **RESET for System Initialization of PC Cards**
- **12-V Supplies Can Be Disabled Except During 12-V Flash Programming**
- **Short-Circuit and Thermal Protection**
- **24-Pin HTSSOP (PWP), 30-Pin SSOP (DB), and 32-Pin TSSOP (DAP) Packages**
- **Compatible With 3.3-V, 5-V, and 12-V PC Cards**
- **Low $r_{DS(on)}$ (95-mΩ, 5-V V_{CC} Switch; 85-mΩ 3.3-V V_{CC} Switch)**
- **Single-Slot Switch: TPS2210A**
  Dual-Slot Switch: TPS2204A and TPS2206A
- **Break-Before-Make Switching**

APPLICATIONS

- **Notebook and Desktop Computers**
- **Set-Top Boxes**
- **Personal Digital Assistants(PDAs)**
- **Digital Cameras**
- **Bar Code Scanners**

DESCRIPTION

The TPS2204A and TPS2206A PC CardBus™ power-interface switches provide an integrated power-management solution for two PC Card™ sockets. The TPS2210A is a single-slot option for this family of devices. These devices allow the controlled distribution of 3.3 V, 5 V, and 12 V to each card slot. The current-limiting and thermal-protection features eliminate the need for fuses. Current-limit reporting helps the user isolate a system fault. The switch $r_{DS(on)}$ and current-limit values are set for the peak and average current requirements stated in the PC Card™ specification, and are optimized for cost.

The TPS2206A is pin and/or functionally compatible with the TPS2206, TPS2216, TPS2216A, TPS2226, TPS2226A, and TPS2228 with a few exceptions, as shown in the Available Options table.

AVAILABLE OPTIONS OF THE TPS2206A PIN COMPATABLE SWITCHES

PART NUMBER	INDEPENDENT V_{PP} SWITCHING	PIN VARIATION					INPUT VOLTAGES
		$\overline{\text{RESET}}$	RESET	$\overline{\text{SHDN}}$	MODE	STBY	
TPS2206	No	Yes	Yes	No	No	No	3.3 V, 5 V, 12 V
TPS2206A	No	Yes	No	Yes	No	No	3.3 V, 5 V, 12 V
TPS2216	Yes/No(1)	Yes	Yes	No	Yes	Yes	3.3 V, 5 V, 12 V
TPS2216A	Yes/No(1)	Yes	Yes	No	Yes	Yes	3.3 V, 5 V, 12 V
TPS2226	Yes	Yes	No	Yes	No	No	3.3 V, 5 V, 12 V
TPS2226A	Yes	Yes	No	Yes	No	No	3.3 V, 5 V, 12 V
TPS2228	Yes	Yes	No	Yes	No	No	1.8 V, 3.3 V, 5 V

(1) Selected by MODE pin.

P^2C is a trademark of Texas Instruments.
PC Card and CardBus are trademarks of PCMCIA (Personal Computer Memory Card International Association).

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	PACKAGED DEVICES		
	PLASTIC SMALL OUTLINE (DB)	POWERPAD™ PLASTIC SMALL OUTLINE (DAP−32)	POWERPAD™ PLASTIC SMALL OUTLINE (PWP−24)
−40°C to 85°C	TPS2206ADB	TPS2206ADAP	TPS2204APWP TPS2210APWP

(1) The DB, PWP, and DAP packages are available taped and reeled. Add R suffix to device type (e.g., TPS2206ADBR) for taped and reeled.

PACKAGE DISSIPATION RATINGS

PACKAGE(1)	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DB (30)	821.46 mW	10.95 mW/°C	328.58 mW	164.29 mW
DAP (32)	3191.4 mW	42.55 mW/°C	1276.5 mW	638.29 mW
PWP (24)	2491.6 mW	33.22 mW/°C	996.67 mW	498.33 mW

(1) These devices are mounted on an JEDEC low-k board (2-oz. traces on surface).

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

			UNITS
Input voltage range for card power	$V_{I(3.3V)}$	−0.3 V to 5.5	V
	$V_{I(5V)}$	−0.3 V to 5.5	V
	$V_{I(12V)}$	−0.3 V to 14	V
Logic input/output voltage		−0.3 V to 6	V
Output voltage	$V_{O(xVCC)}$	−0.3 V to 6	V
	$V_{O(xVPP)}$	−0.3 V to 14	V
Continuous total power dissipation		See Dissipation Rating Table	
Output current	$I_{O(xVCC)}$	Internally Limited	
	$I_{O(xVPP)}$	Internally Limited	
Operating virtual junction temperature range, T_J		−40°C to 100	°C
Storage temperature range, T_{STG}		−55°C to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds)		260	°C
$\overline{OC}$ sink current		10	mA

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

PowerPAD is a trademark of Texas Instruments.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
Input voltage, $V_{I(3.3V)}$ is required for all circuit operations. 5 V and 12 V are only required for their respective functions.	$V_{I(3.3V)}$(1)	3	3.6	V
	$V_{I(5V)}$	3	5.5	V
	$V_{I(12V)}$	7	13.5	V
Output current, I_O	$I_{O(xVCC)}$ at T_J = 100°C		1	A
	$I_{O(xVPP)}$ at T_J = 100°C		100	mA
Clock frequency, $f_{(clock)}$			2.5	MHz
Pulse duration, t_W	Data	200		ns
	Latch	250		ns
	Clock	100		ns
	Reset	100		ns
Data-to-clock hold time, t_h (see Figure 2)		100		ns
Data-to-clock setup time, t_{su} (see Figure 2)		100		ns
Latch delay time, $t_{d(latch)}$ (see Figure 2)		100		ns
Clock delay time, $t_{d(clock)}$ (see Figure 2)		250		ns
Operating virtual junction temperature, T_J (maximum to be calculated at worst case P_D at 85°C ambient)		−40	100	°C

(1) It is understood that for $V_{I(3.3V)}$< 3 V, voltages within the absolute maximum ratings applied to pin 5 V or pin 12 V will not damage the IC.

ELECTRICAL CHARACTERISTICS

T_J = 25°C, $V_{I(5V)}$ = 5 V, $V_{I(3.3V)}$ = 3.3 V, $V_{I(12V)}$ = 12 V, all outputs unloaded (unless otherwise noted)

POWER SWITCH

PARAMETER			TEST CONDITIONS(1)		MIN	TYP	MAX	UNIT
$r_{DS(on)}$	Static drain-source on-state resistance	3.3V to xVCC (2)	I_O = 750 mA each			85	110	mΩ
			I_O = 750 mA each, T_J = 100°C			110	140	mΩ
		5V to xVCC(2)	I_O = 500 mA each			95	130	mΩ
			I_O = 500 mA each, T_J = 100°C			120	160	mΩ
		3.3V or 5V to xVPP(2)	I_O = 50 mA each			0.8	1	Ω
			I_O = 50 mA each, T_J = 100°C			1	1.3	Ω
		12V to xVPP (2)	I_O = 50 mA each			2	2.5	Ω
			I_O = 50 mA each, T_J = 100°C			2.5	3.4	Ω
	Output discharge resistance	Discharge at xVCC	$I_{O(disc)}$ = 1 mA		0.5	0.7	1	kΩ
		Discharge at xVPP	$I_{O(disc)}$ = 1 mA		0.2	0.4	0.5	kΩ
I_{OS}	Short-circuit output current		Limit (steady-state value), output powered into a short circuit	$I_{OS(xVCC)}$	1	1.4	2	A
				$I_{OS(xVPP)}$	120	200	300	mA
			Limit (steady-state value), output powered into a short circuit, T_J = 100°C	$I_{OS(xVCC)}$	1	1.4	2	A
				$I_{OS(xVPP)}$	120	200	300	mA
	Thermal shutdown temperature(2)	Thermal trip point, T_J	Rising temperature			135		°C
		Hysteresis, T_J				10		°C
	Current-limit response time (3)(4)		5V to xVCC = 5 V, with 100-mΩ short to GND			10		µs
			5V to xVPP = 5 V, with 100-mΩ short to GND			3		µs

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.
(2) TPS2204A and TPS2206A: two switches on. TPS2210A: one switch on.
(3) Specified by design; not tested in production.
(4) From application of short to 110% of final current limit.

ELECTRICAL CHARACTERISTICS Continued

T_J = 25°C, $V_{I(5V)}$ = 5 V, $V_{I(3.3V)}$ = 3.3 V, $V_{I(12V)}$ = 12 V, all outputs unloaded (unless otherwise noted)

PARAMETER				TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_I	Input current, quiescent	Normal operation	$I_{I(3.3V)}$	V_O(xVCC) = V_O(xVPP) = 3.3 V and also for RESET = 0 V			140	200	μA
			$I_{I(5V)}$				8	12	
			$I_{I(12V)}$				100	180	
		Shutdown mode	$I_{I(3.3V)}$	V_O(xVCC) = V_O(xVPP) = Hi-Z			0.3	2	
			$I_{I(5V)}$				0.1	2	
			$I_{I(12V)}$				0.3	2	
I_{lkg}	Leakage current, output off state	Shutdown mode		$V_{O(xVCC)}$ = 5 V, $V_{I(5V)}$ = $V_{I(12V)}$ = 0 V				10	μA
					T_J = 100°C			50	
				$V_{O(xVPP)}$ = 12 V, $V_{I(5V)}$ = $V_{I(12V)}$ = 0 V				10	
					T_J = 100°C			50	

LOGIC SECTION (CLOCK, DATA, LATCH, $\overline{\text{RESET}}$, $\overline{\text{SHDN}}$, $\overline{\text{OC}}$)							
PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_I	Input current, logic	$I_{I(\overline{RESET})}$(1)	$\overline{\text{RESET}}$ = 5.5 V	−1		1	μA
			$\overline{\text{RESET}}$ = 0 V	−30	−20	−10	
		$I_{I(\overline{SHDN})}$(1)	$\overline{\text{SHDN}}$ = 5.5 V	−1		1	
			$\overline{\text{SHDN}}$ = 0 V	−50		−3	
		$I_{I(LATCH)}$(1)	LATCH = 5.5 V			50	
			LATCH = 0 V	−1		1	
		$I_{I(CLOCK, DATA)}$	0 V to 5.5 V	−1		1	
V_{IH}	High-level input voltage, logic			2			V
V_{IL}	Low-level input voltage, logic					0.8	V
$V_{O(sat)}$	Output saturation voltage at $\overline{\text{OC}}$		I_O = 2 mA		0.14	0.4	V
I_{lkg}	Leakage current at $\overline{\text{OC}}$		$V_{O(/OC)}$ = 5.5 V		0	1	μA

(1) LATCH has low current pulldown. $\overline{\text{RESET}}$ and $\overline{\text{SHDN}}$ have low-current pullup.

UVLO AND POR (POWER-ON RESET)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{I(3.3V)}$	Input voltage at 3.3V pin, UVLO	3.3-V level below which all switches are Hi-Z	2.4	2.7	2.9	V
$V_{hys(3.3V)}$	UVLO hysteresis voltage at VA (1)			100		mV
$V_{I(5V)}$	Input voltage at 5V pin, UVLO	5-V level below which only 5V switches are Hi-Z	2.3	2.5	2.9	V
$V_{hys(5V)}$	UVLO hysteresis voltage at 5 V(1)			100		mV
t_{df}	Delay time for falling response, UVLO(1)	Delay from voltage hit (step from 3 V to 2.3 V) to Hi-Z control (90% V_G to GND)		4		μs
$V_{I(POR)}$	Input voltage, power-on reset(1)	3.3-V voltage below which POR is asserted causing a RESET internally with all line switches open and all discharge switches closed.			1.7	V

(1) Specified by design; not tested in production.

SWITCHING CHARACTERISTICS

V_{CC} = 5 V, T_A = 25°C, $V_{I(3.3V)}$ = 3.3 V, $V_{I(5V)}$ = 5 V, $V_{I(12)}$ = 12 V (not applicable for TPS2223A) all outputs unloaded (unless otherwise noted)

PARAMETER(1)		LOAD CONDITION	TEST CONDITIONS(2)		MIN	TYP	MAX	UNIT
t_r	Output rise times(3)	$C_{L(xVCC)}$= 0.1 µF, $C_{L(xVPP)}$= 0.1 µF, $I_{O(xVCC)}$ = 0 A, $I_{O(xVPP)}$ = 0 A	$V_{O(xVCC)}$ = 5 V			0.9		ms
			$V_{O(xVPP)}$ = 12 V			0.26		
		$C_{L(xVCC)}$= 150 µF, $C_{L(xVPP)}$= 10 µF, $I_{O(xVCC)}$ = 0.75 A, $I_{O(xVPP)}$ = 50 mA	$V_{O(xVCC)}$ = 5 V			1.1		
			$V_{O(xVPP)}$ = 12 V			0.6		
t_f	Output fall times(3)	$C_{L(xVCC)}$= 0.1 µF, $C_{L(xVPP)}$= 0.1 µF, $I_{O(xVCC)}$ = 0 A, $I_{O(xVPP)}$ = 0 A	$V_{O(xVCC)}$ = 5 V, Discharge switches ON			0.5		ms
			$V_{O(xVPP)}$ = 12 V, Discharge switches ON			0.2		
		$C_{L(xVCC)}$= 150 µF, $C_{L(xVPP)}$= 10 µF, $I_{O(xVCC)}$ = 0.75 A, $I_{O(xVPP)}$ = 50 mA	$V_{O(xVCC)}$ = 5 V			2.35		
			$V_{O(xVPP)}$ = 12 V			3.9		
t_{pd}	Propagation delay times(3)	$C_{L(xVCC)}$= 0.1 µF, $C_{L(xVPP)}$= 0.1 µF, $I_{O(xVCC)}$ = 0 A, $I_{O(xVPP)}$ = 0 A	Latch↑ to xVPP (12 V)	t_{pdon}		2		ms
				t_{pdoff}		0.62		
			Latch↑ to xVPP (5 V)	t_{pdon}		0.77		
				t_{pdoff}		0.51		
			Latch↑ to xVPP (3.3 V)	t_{pdon}		0.75		
				t_{pdoff}		0.52		
			Latch↑ to xVCC (5 V)	t_{pdon}		0.3		
				t_{pdoff}		2.5		
			Latch↑ to xVCC (3.3V)	t_{pdon}		0.3		
				t_{pdoff}		2.8		
		$C_{L(xVCC)}$= 150 µF, $C_{L(xVPP)}$= 10 µF, $I_{O(xVCC)}$ = 0.75 A, $I_{O(xVPP)}$ = 50 mA	Latch↑ to xVPP (12 V)	t_{pdon}		2.2		ms
				t_{pdoff}		0.8		
			Latch↑ to xVPP (5 V)	t_{pdon}		0.8		
				t_{pdoff}		0.6		
			Latch↑ to xVPP (3.3 V)	t_{pdon}		0.8		
				t_{pdoff}		0.6		
			Latch↑ to xVCC (5 V)	t_{pdon}		0.6		
				t_{pdoff}		2.5		
			Latch↑ to xVCC (3.3V)	t_{pdon}		0.5		
				t_{pdoff}		2.6		

(1) Refer to Parameter Measurement Information in Figure 1.
(2) No card inserted, assumes a 0.1-µF output capacitor (see Figure 1).
(3) Specified by design; not tested in production.

TEXAS INSTRUMENTS
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PIN ASSIGNMENTS

TPS2206A
DB PACKAGE
(TOP VIEW)

5V	1	30	5V
5V	2	29	NC
DATA	3	28	NC
CLOCK	4	27	NC
LATCH	5	26	NC
NC	6	25	$\overline{\text{SHDN}}$
12V	7	24	12V
AVPP	8	23	BVPP
AVCC	9	22	BVCC
AVCC	10	21	BVCC
AVCC	11	20	BVCC
GND	12	19	NC
NC	13	18	$\overline{\text{OC}}$
$\overline{\text{RESET}}$	14	17	3.3V
3.3V	15	16	3.3V

NC − No internal connection

TPS2206A
DAP PACKAGE
(TOP VIEW)

5V	1	32	5V
5V	2	31	NC
NC	3	30	NC
DATA	4	29	NC
CLOCK	5	28	NC
LATCH	6	27	NC
NC	7	26	$\overline{\text{SHDN}}$
12V	8	25	12V
AVPP	9	24	BVPP
AVCC	10	23	BVCC
AVCC	11	22	BVCC
AVCC	12	21	BVCC
GND	13	20	$\overline{\text{OC}}$
$\overline{\text{RESET}}$	14	19	NC
NC	15	18	3.3V
3.3V	16	17	3.3V

TPS2204A
PWP PACKAGE
(TOP VIEW)

5V	1	24	5V
5V	2	23	NC
DATA	3	22	NC
CLOCK	4	21	$\overline{\text{SHDN}}$
LATCH	5	20	12V
NC	6	19	BVPP
12V	7	18	BVCC
AVPP	8	17	BVCC
AVCC	9	16	NC
AVCC	10	15	$\overline{\text{OC}}$
GND	11	14	3.3V
$\overline{\text{RESET}}$	12	13	3.3V

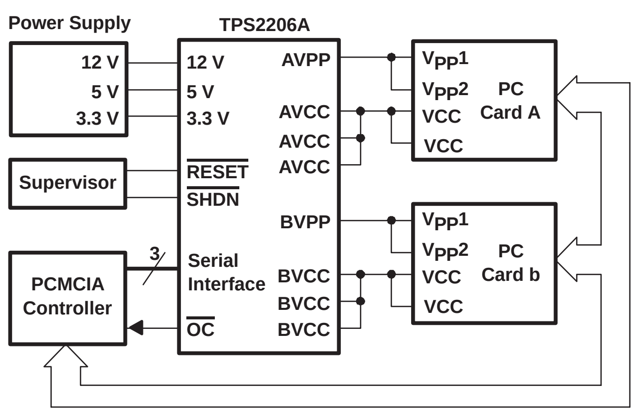
TPS2210A
PWP PACKAGE
(TOP VIEW)

5V	1	24	NC
5V	2	23	NC
DATA	3	22	NC
CLOCK	4	21	$\overline{\text{SHDN}}$
LATCH	5	20	12V
NC	6	19	NC
12V	7	18	NC
AVPP	8	17	NC
AVCC	9	16	NC
AVCC	10	15	$\overline{\text{OC}}$
GND	11	14	NC
$\overline{\text{RESET}}$	12	13	3.3V

TERMINAL FUNCTIONS

TERMINAL					I/O	DESCRIPTION
NAME	NUMBER					
	TPS2204A	TPS2206A		TPS2210A		
	PWP	DB	DAP	PWP		
3.3V	13, 14	15, 16, 17	16, 17, 18	13	I	3.3-V input for card power and chip power
5V	1, 2, 24	1, 2, 30	1, 2, 32	1, 2	I	5-V V_{CC} input for card power
12V	7, 20	7, 24	8, 25	7, 20	I	12-V V_{PP} input for card power (xVPP). The two 12-V pins must be externally connected.
AVCC	9, 10	9, 10, 11	10, 11, 12	9, 10	O	Switched output that delivers 0 V, 3.3 V, 5 V, or high impedance to card.
AVPP	8	8	9	8	O	Switched output that delivers 0 V, 3.3 V, 5 V, 12 V, or high impedance to card.
BVCC	17, 18	20, 21, 22	21, 22, 23	−−	O	Switched output that delivers 0 V, 3.3 V, 5 V, or high impedance.
BVPP	19	23	24	−−	O	Switched output that delivers 0 V, 3.3 V, 5 V, 12 V, or high impedance.
CLOCK	4	4	5	4	I	Logic-level clock for serial data word
DATA	3	3	4	3	I	Logic-level serial data word
GND	11	12	13	11		Ground
LATCH	5	5	6	5	I	Logic-level latch for serial data word, internal pulldown
NC	6, 16, 22, 23	13, 19, 26−29	3, 7, 15, 19, 27−31	6, 14, 16 − 19, 22−24		No internal connection
$\overline{\text{OC}}$	15	18	20	15	O	Open-drain overcurrent reporting output that goes low when an overcurrent condition exists. An external pullup is required.
$\overline{\text{SHDN}}$	21	25	26	21	I	Hi-Z (open) all switches. Identical function to serial D8. Asynchronous active-low command, internal pullup
$\overline{\text{RESET}}$	12	14	14	12	I	Logic-level RESET input active low. Do not connect if terminal 6 is used.

TYPICAL PC CARD POWER−DISTRIBUTION APPLICATION



PARAMETER MEASUREMENT INFORMATION

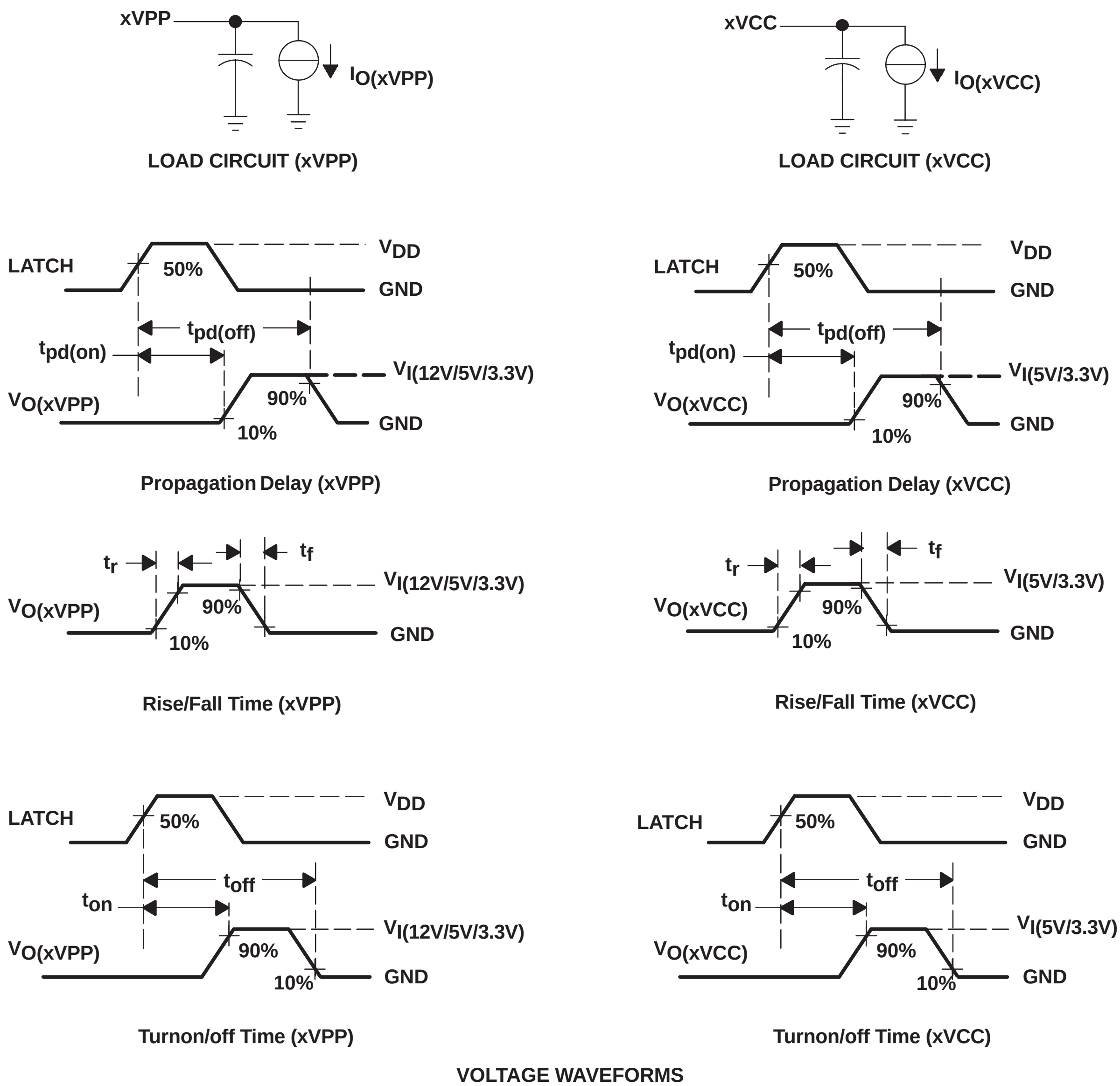
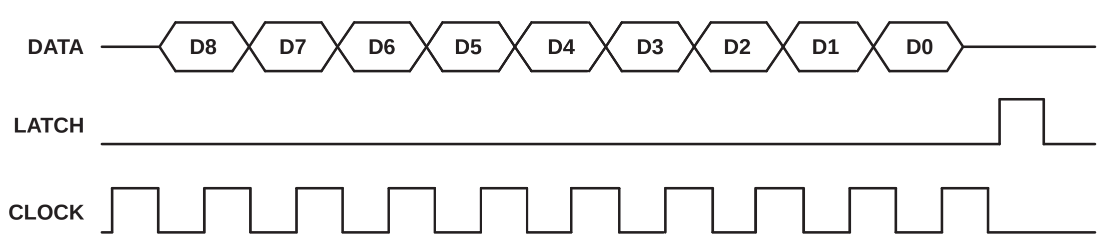


Figure 1. Test Circuits and Voltage Waveforms



NOTE: Data is clocked in on the positive edge of the clock. The latch should occur before the next positive leading edge of the clock. For definition of D0to D8, see the control logic table.

Figure 2. Serial-Interface Timing for TPS2206A

TABLE OF GRAPHS

		FIGURE
Short-circuit response, short applied to powered-on 5-V xVCC-switch output	vs Time	3
Short-circuit response, short applied to powered-on 12-V xVPP-switch output	vs Time	4
$\overline{OC}$ response with ramped overcurrent-limit load on 5-V xVCC-switch output	vs Time	5
$\overline{OC}$ response with ramped overcurrent-limit load on 12-V xVPP-switch output	vs Time	6
Turnon propagation delay time, xVCC (C_L = 150 µF)	vs Junction temperature	7
Turnoff propagation delay time, xVCC (C_L = 150 µF)	vs Junction temperature	8
Turnon propagation delay time, xVPP (C_L = 10 µF)	vs Junction temperature	9
Turnoff propagation delay time, xVPP (C_L = 10 µF)	vs Junction temperature	10
Turnon propagation delay time, xVCC (T_J = 25°C)	vs Load capacitance	11
Turnoff propagation delay time, xVCC (T_J = 25°C)	vs Load capacitance	12
Turnon propagation delay time, xVPP (T_J = 25°C)	vs Load capacitance	13
Turnoff propagation delay time, xVPP (T_J = 25°C)	vs Load capacitance	14
Rise time, xVCC (C_L = 150 µF)	vs Junction temperature	15
Fall time, xVCC (C_L = 150 µF)	vs Junction temperature	16
Rise time, xVPP (C_L = 10 µF)	vs Junction temperature	17
Fall time, xVPP (C_L = 10 µF)	vs Junction temperature	18
Rise time, xVCC (T_J = 25°C)	vs Load capacitance	19
Fall time, xVCC (T_J = 25°C)	vs Load capacitance	20
Rise time, xVPP (T_J = 25°C)	vs Load capacitance	21
Fall time, xVPP (T_J = 25°C)	vs Load capacitance	22

SHORT-CIRCUIT RESPONSE, SHORT APPLIED TO POWERED-ON 5-V xVCC-SWITCH OUTPUT vs TIME

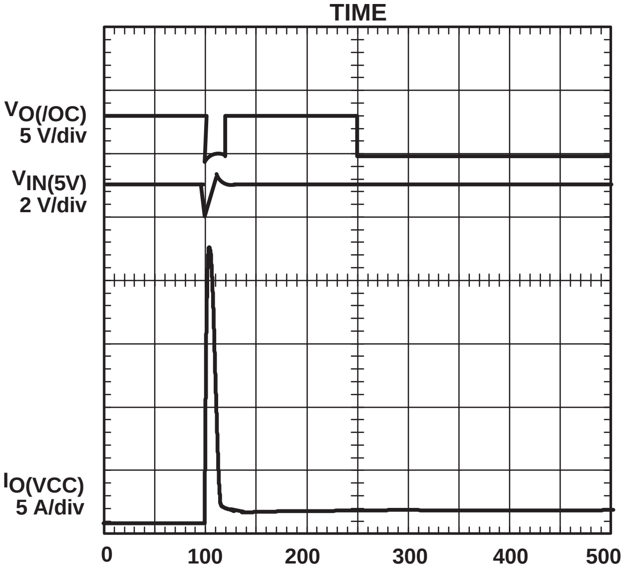


Figure 3

SHORT-CIRCUIT RESPONSE, SHORT APPLIED TO POWERED-ON 12-V xVPP-SWITCH OUTPUT vs TIME

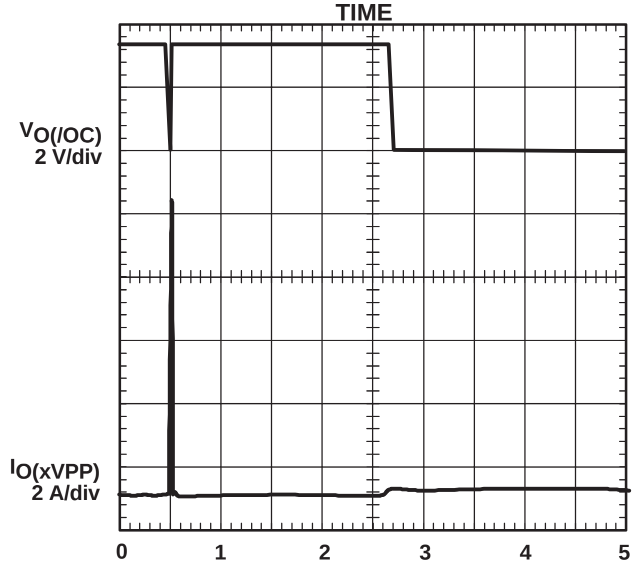


Figure 4

$\overline{OC}$ RESPONSE WITH RAMPED OVERCURRENT-LIMIT LOAD ON 5-V xVCC-SWITCH OUTPUT
vs
TIME

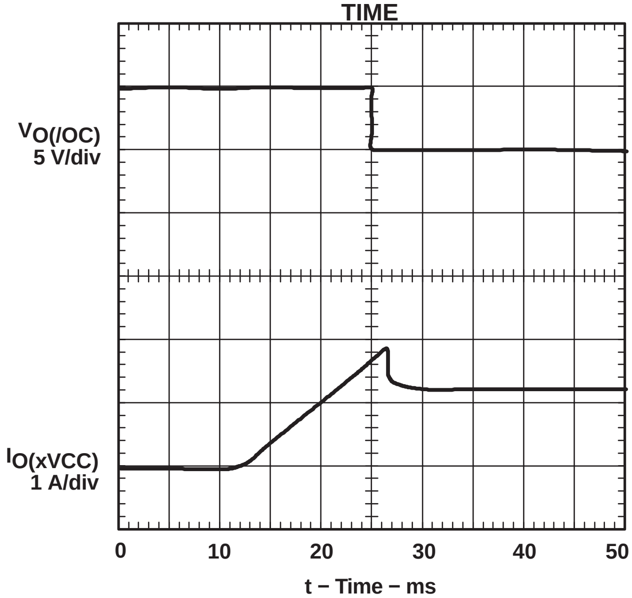


Figure 5

$\overline{OC}$ RESPONSE WITH RAMPED OVERCURRENT-LIMIT LOAD ON 12-V xVPP-SWITCH OUTPUT
vs
TIME

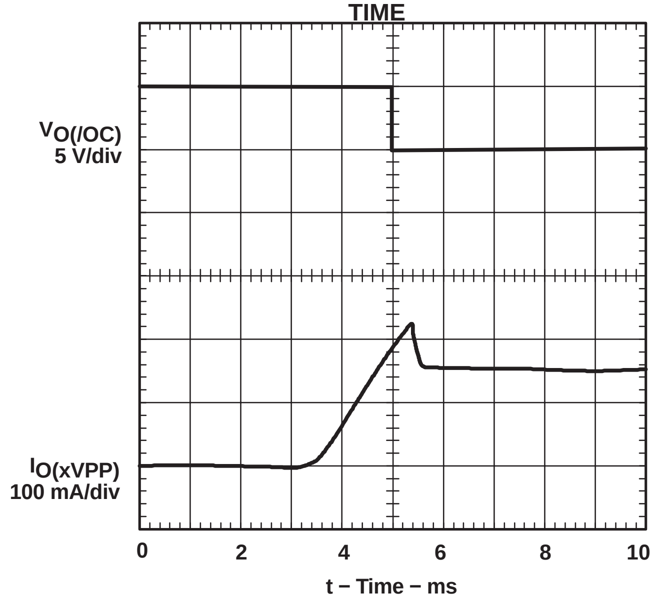


Figure 6

TURNON PROPAGATION DELAY TIME, xVCC
vs
JUNCTION TEMPERATURE

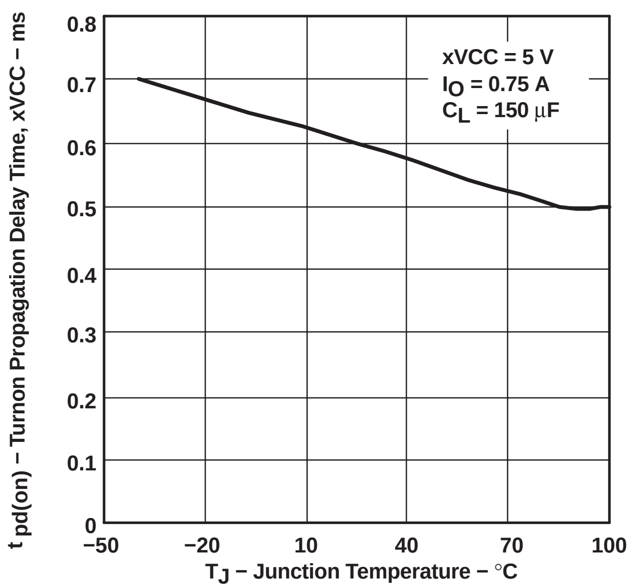


Figure 7

TURNOFF PROPAGATION DELAY TIME, xVCC
vs
JUNCTION TEMPERATURE

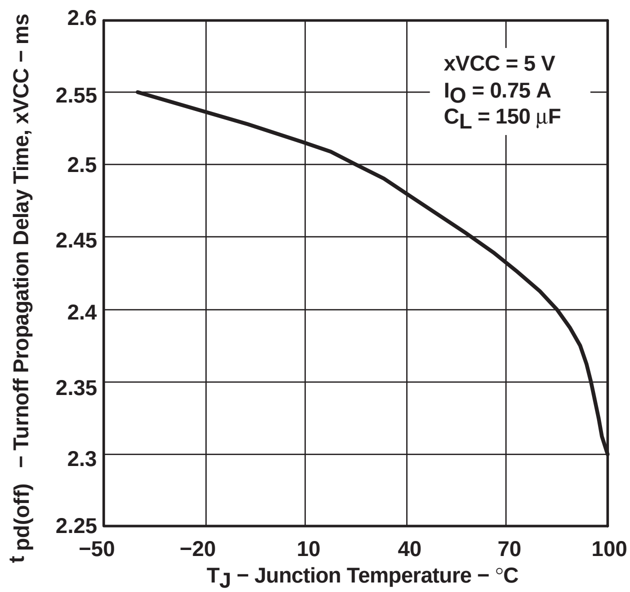


Figure 8

TURNON PROPAGATION DELAY TIME, xVPP
vs
JUNCTION TEMPERATURE

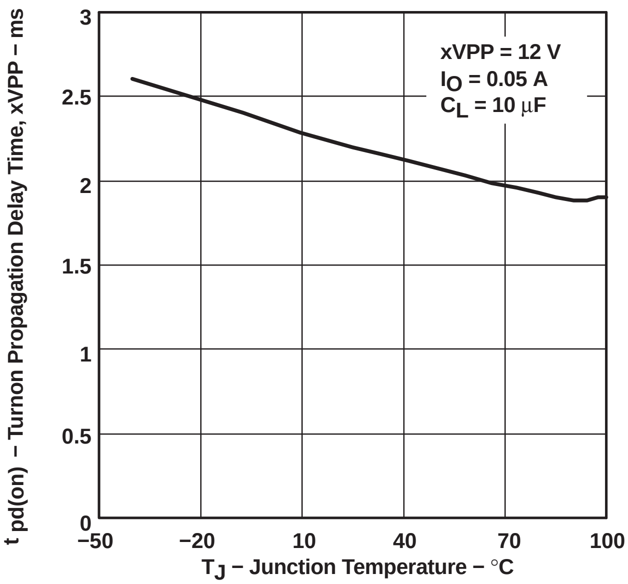


Figure 9

TURNOFF PROPAGATION DELAY TIME, xVPP
vs
JUNCTION TEMPERATURE

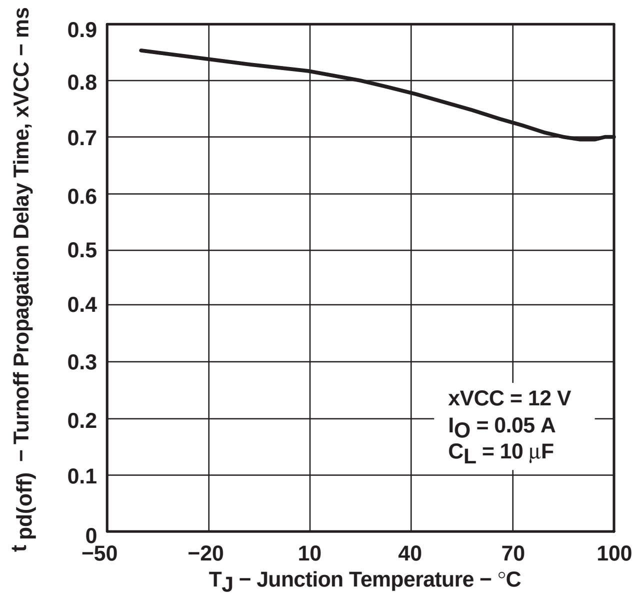


Figure 10

TURNON PROPAGATION DELAY TIME, xVCC
vs
LOAD CAPACITANCE

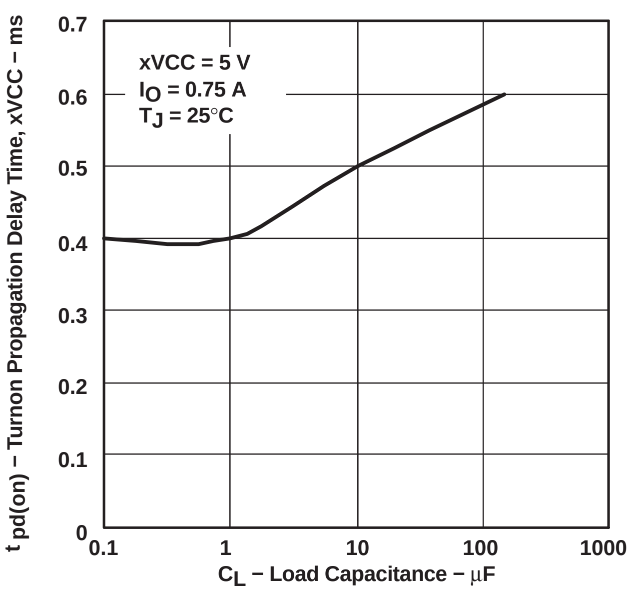


Figure 11

TURNOFF PROPAGATION DELAY TIME, xVCC
vs
LOAD CAPACITANCE

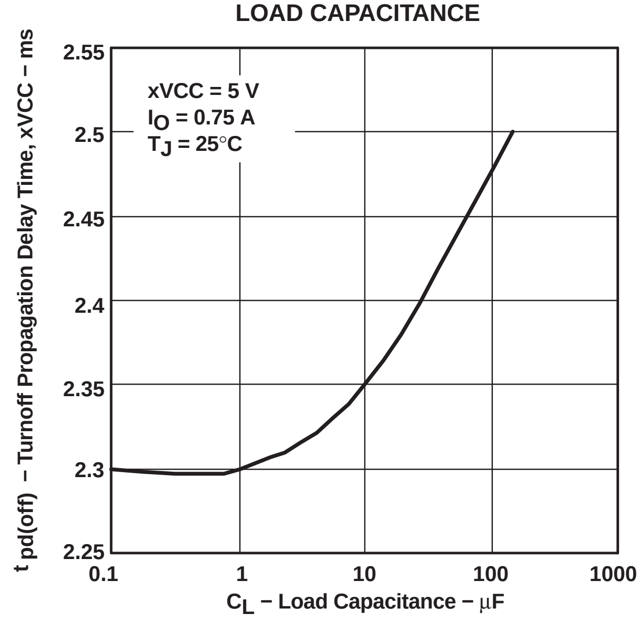


Figure 12

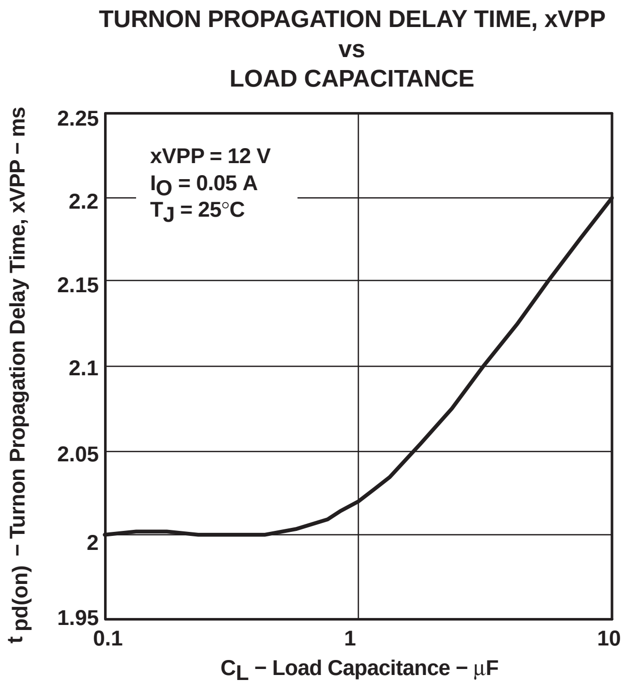


Figure 13

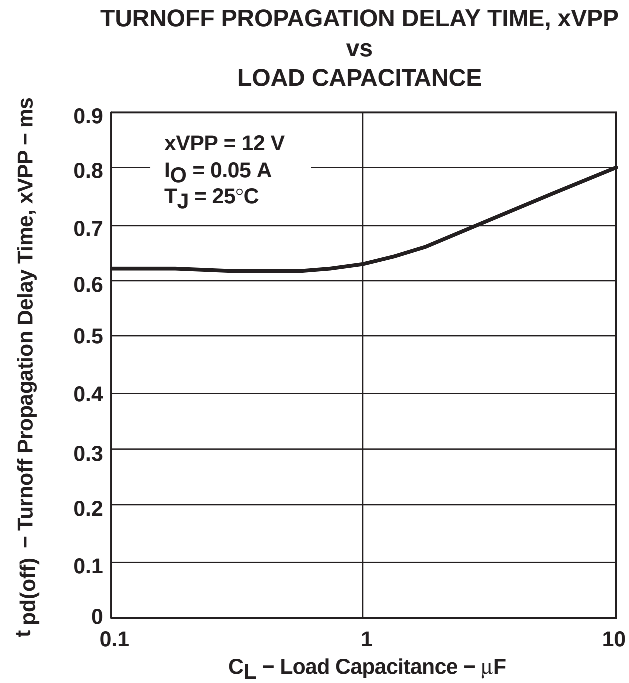


Figure 14

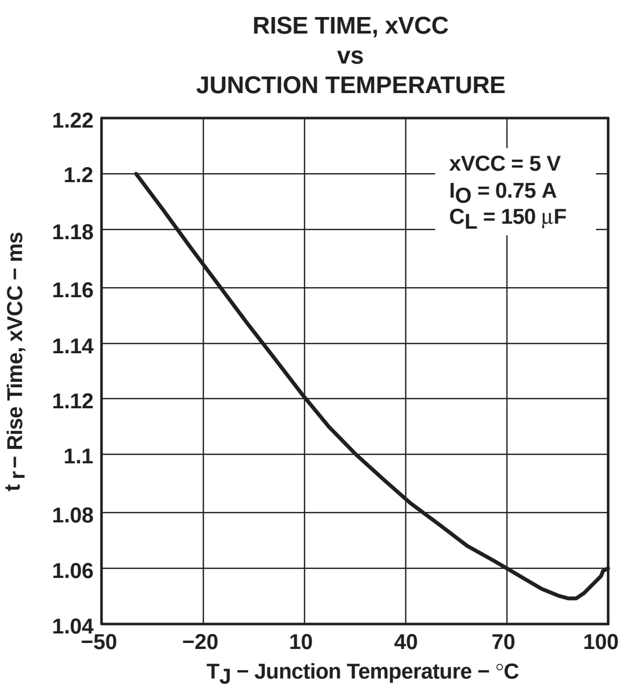


Figure 15

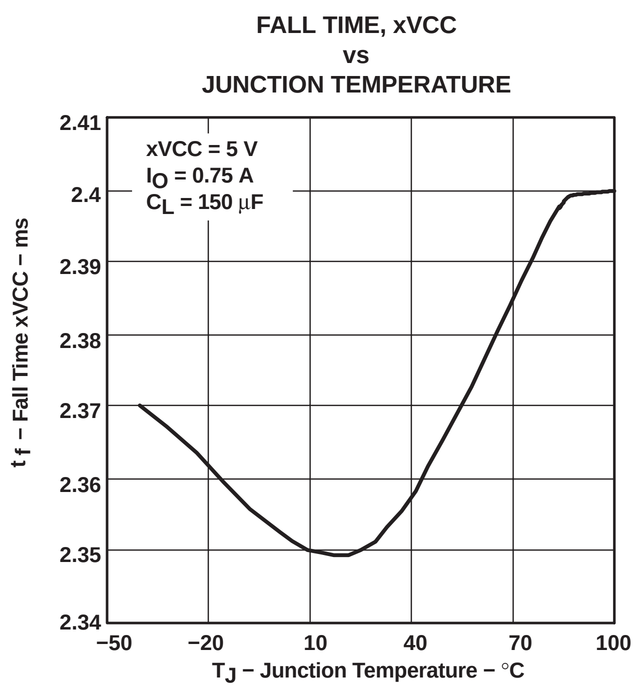


Figure 16

RISE TIME, xVPP
vs
JUNCTION TEMPERATURE

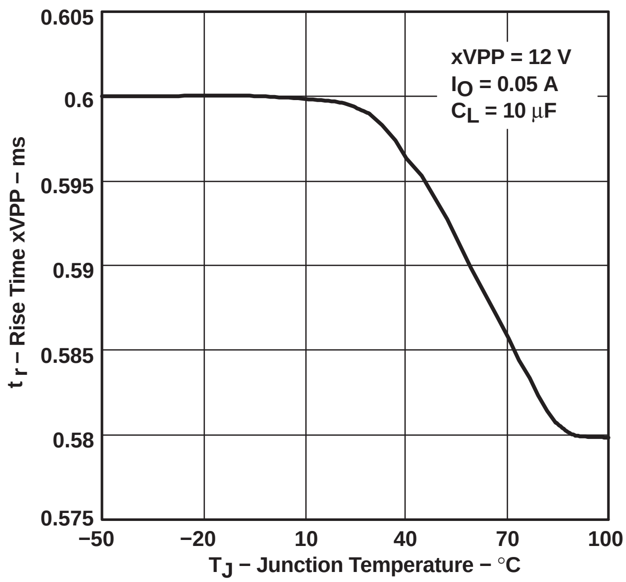


Figure 17

FALL TIME, xVPP
vs
JUNCTION TEMPERATURE

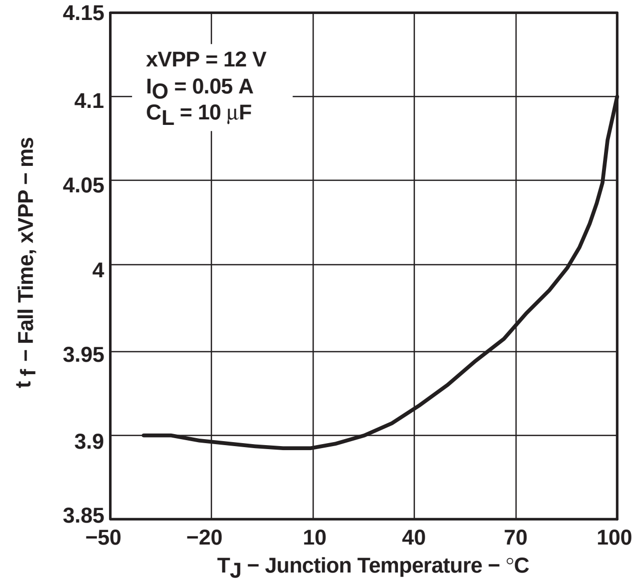


Figure 18

RISE TIME, xVCC
vs
LOAD CAPACITANCE

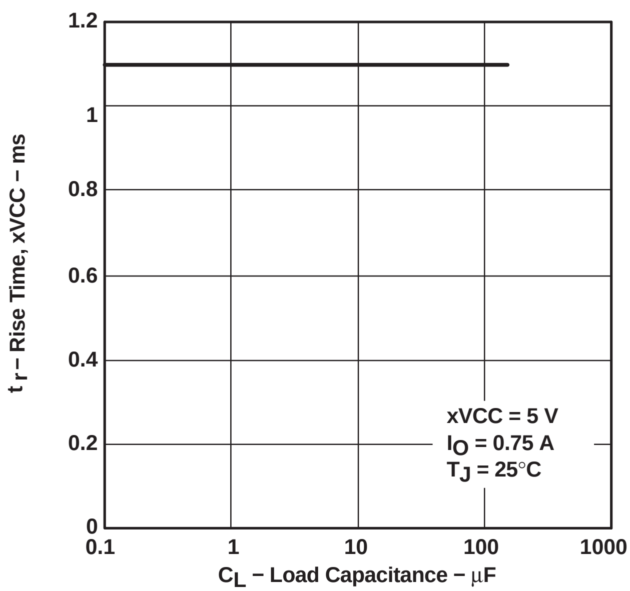


Figure 19

FALL TIME, xVCC
vs
LOAD CAPACITANCE

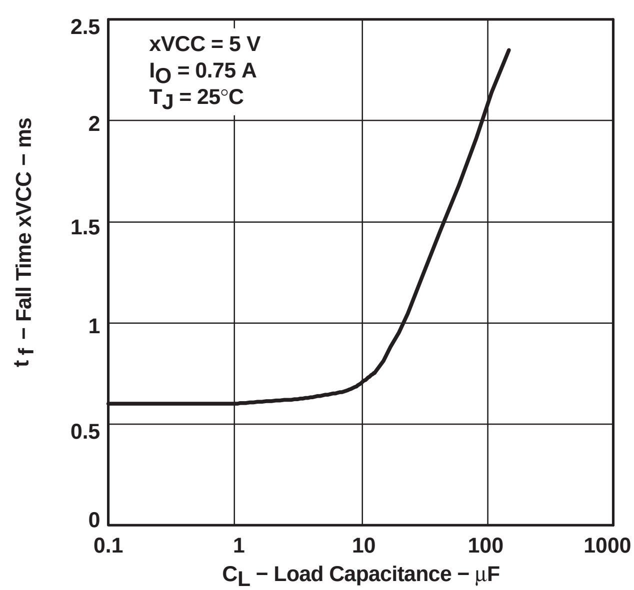


Figure 20

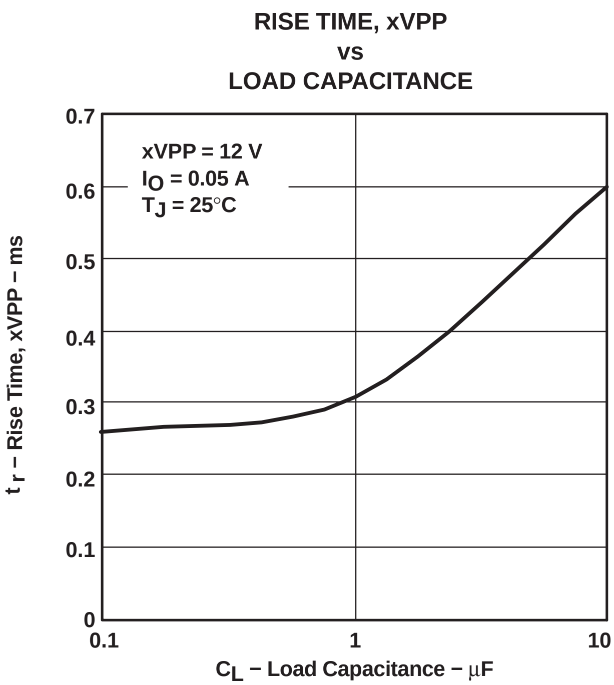


Figure 21

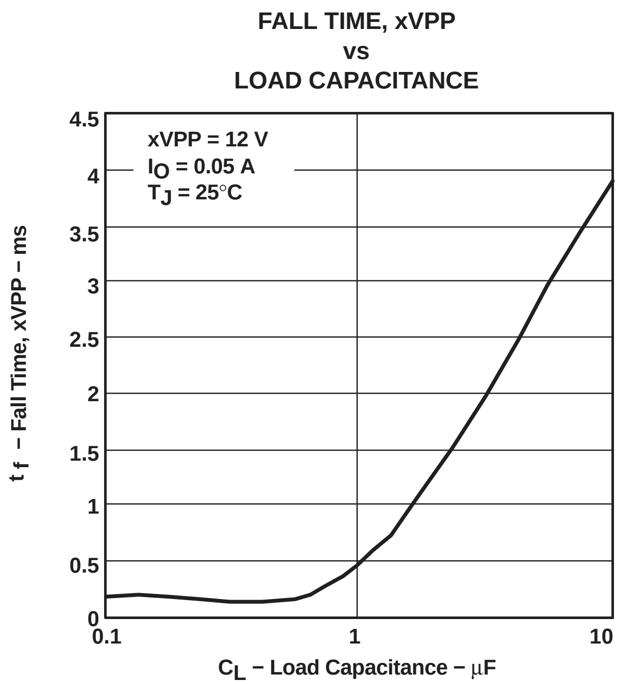


Figure 22

TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

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INPUT CURRENT, xVCC = 3.3 V
vs
JUNCTION TEMPERATURE

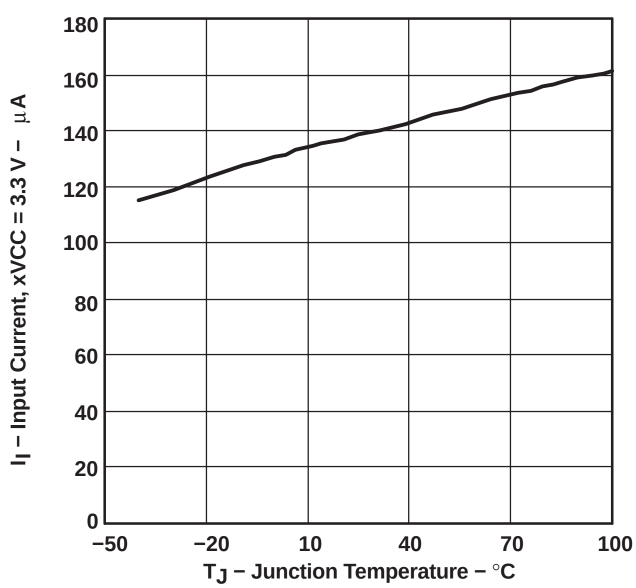


Figure 23

INPUT CURRENT, xVCC = 5 V
vs
JUNCTION TEMPERATURE

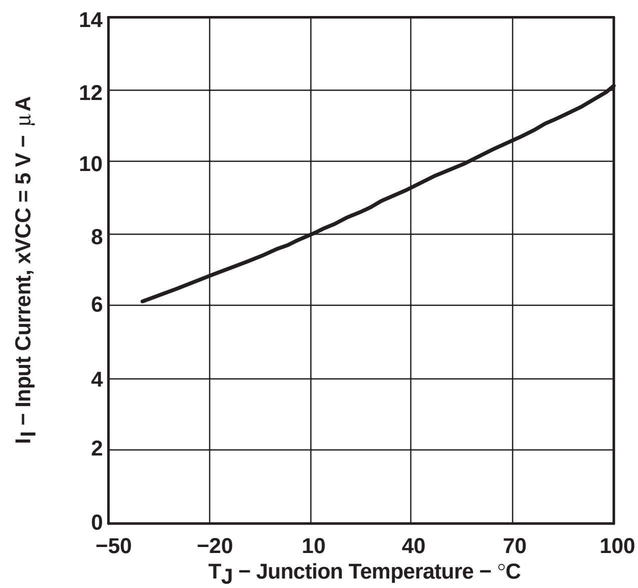


Figure 24

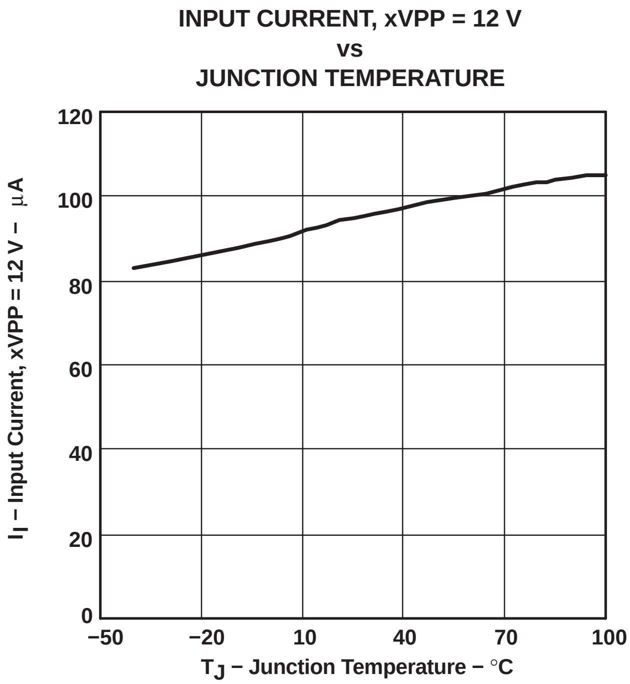


Figure 25

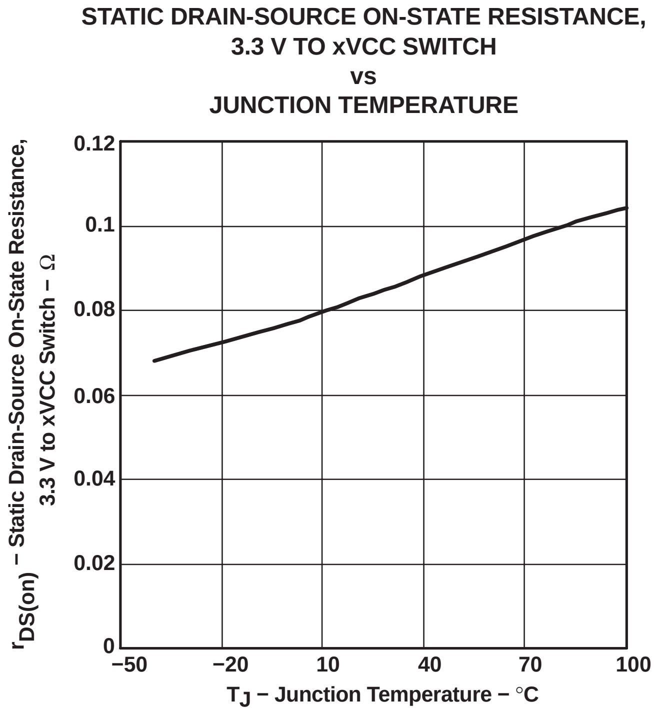


Figure 26

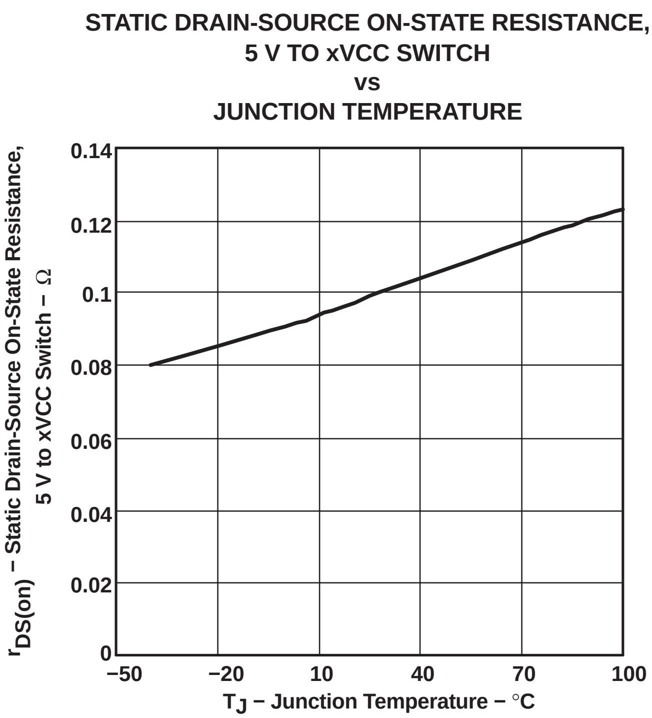


Figure 27

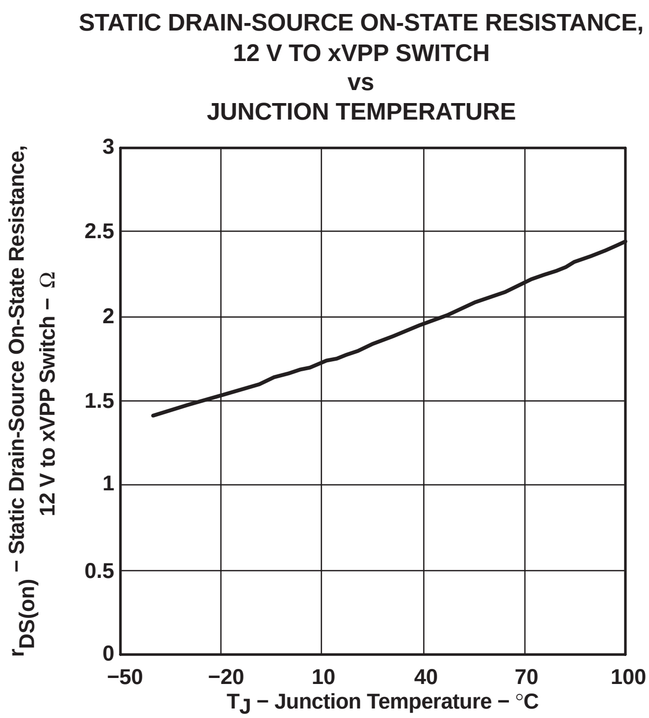


Figure 28

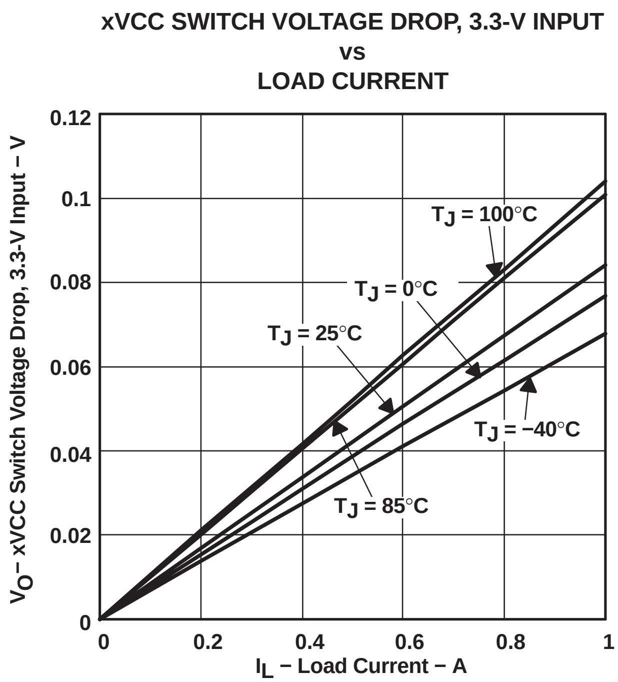


Figure 29

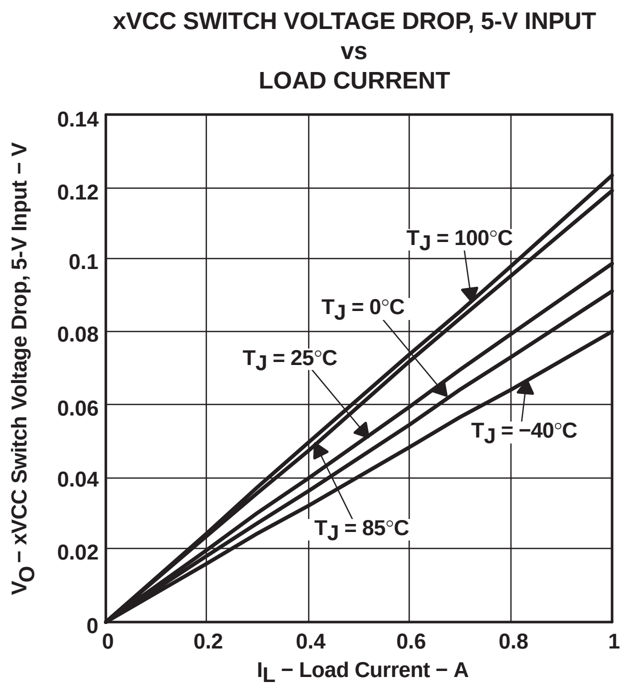


Figure 30

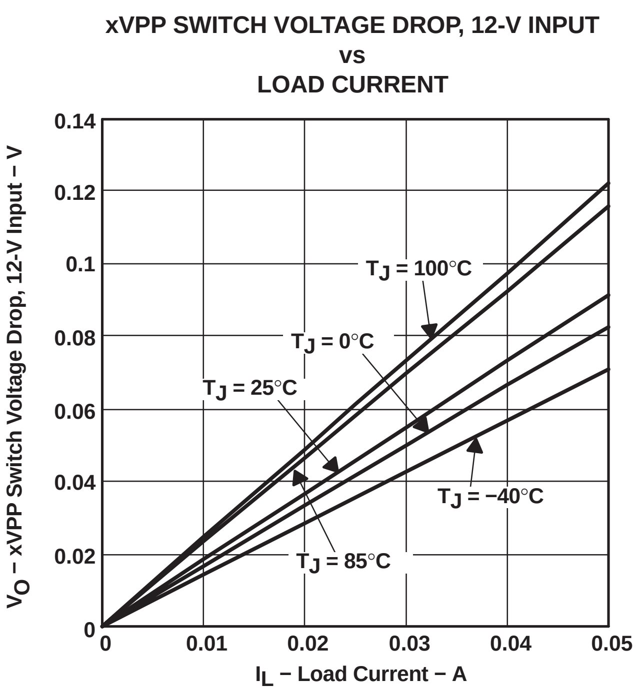


Figure 31

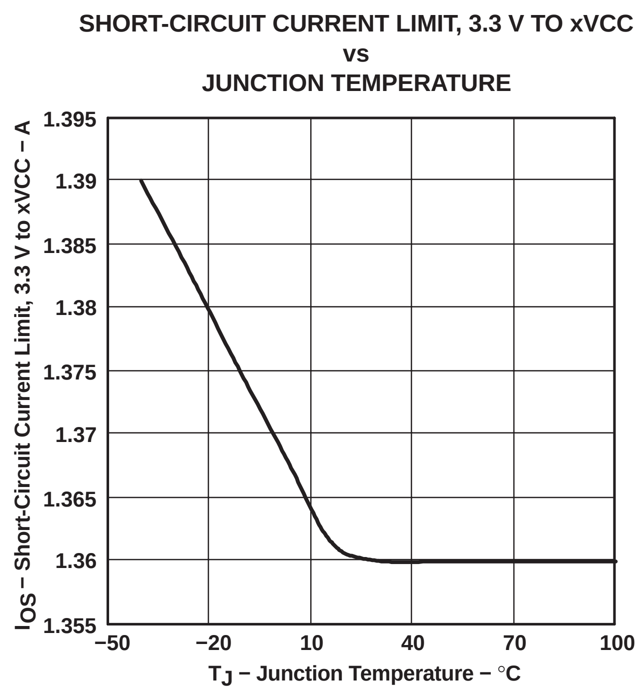


Figure 32

SHORT-CIRCUIT CURRENT LIMIT, 5 V TO xVCC
vs
JUNCTION TEMPERATURE

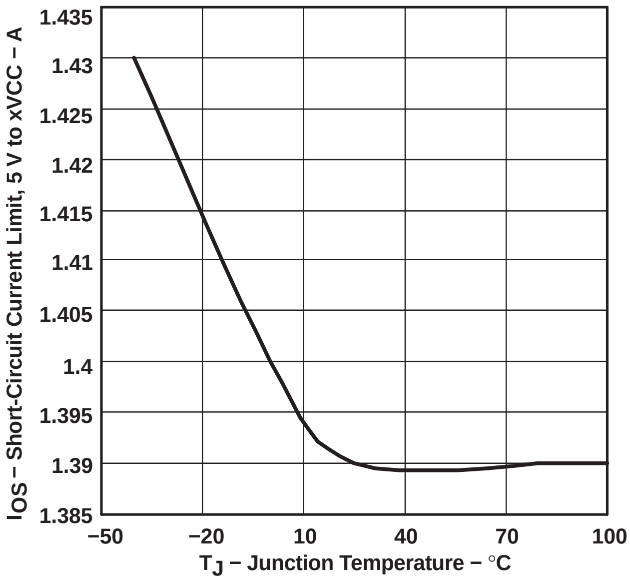


Figure 33

SHORT-CIRCUIT CURRENT LIMIT, 12 V TO xVPP
vs
JUNCTION TEMPERATURE

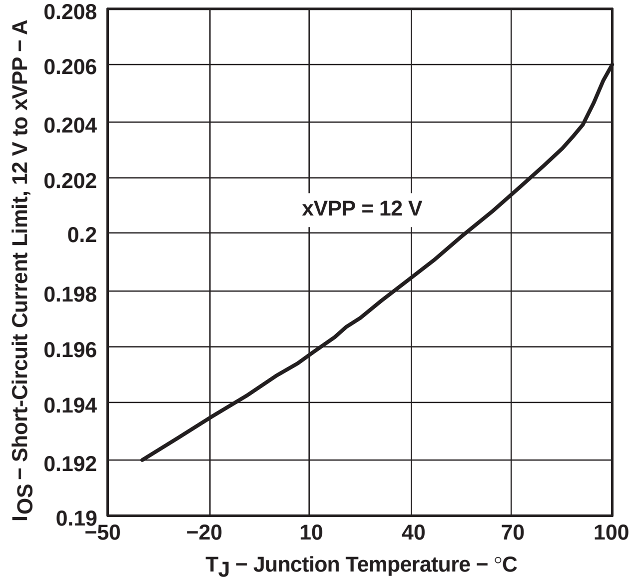


Figure 34

APPLICATION INFORMATION

OVERVIEW

PC Cards were initially introduced as a means to add flash memory to portable computers. The idea of add-in cards quickly took hold, and modems, wireless LANs, global positioning satellite system (GPS), multimedia, and hard-disk versions were soon available. As the number of PC Card applications grew, the engineering community quickly recognized the need for a standard to ensure compatibility across platforms. To this end, the PCMCIA (Personal Computer Memory Card International Association) was established, comprising members from leading computer, software, PC Card, and semiconductor manufacturers. One key goal was to realize the *plug-and-play* concept, so that cards and hosts from different vendors would be transparently compatible.

PC CARD POWER SPECIFICATION

System compatibility also means power compatibility. The most current set of specifications (PC Card Standard) set forth by the PCMCIA committee states that power is to be transferred between the host and the card through eight of the 68 terminals of the PC Card connector. This power interface consists of two V_{CC}, two V_{pp}, and four ground terminals. Multiple V_{CC} and ground terminals minimize connector-terminal and line resistance. The two V_{pp} terminals were originally specified as separate signals, but are normally tied together in the host to form a single node to minimize voltage losses. Card primary power is supplied through the V_{CC} terminals; flash-memory programming and erase voltage are supplied through the V_{pp} terminals.

DESIGNING FOR VOLTAGE REGULATION

The current PCMCIA specification for output voltage regulation, $V_{O(reg)}$, of the 5-V output is 5% (250 mV). In a typical PC power-system design, the power supply has an output-voltage regulation, $V_{PS(reg)}$, of 2% (100 mV). Also, a voltage drop from the power supply to the PC Card results from resistive losses, V_{PCB}, in the PCB traces and the PCMCIA connector. A typical design would limit the total of these resistive losses to less than 1% (50 mV) of the output voltage. Therefore, the allowable voltage drop, V_{DS}, for the device would be the PCMCIA voltage regulation less the power supply regulation and less the PCB and connector resistive drops:

$$V_{DS} = V_{O(reg)} - V_{PS(reg)} - V_{PCB}$$

Typically, this would leave 100 mV for the allowable voltage drop across the TPS2204A, TPS2206A, or TPS2210A. The voltage drop is the output current multiplied by the switch resistance of the device. Therefore, the maximum output current, I_O max, that can be delivered to the PC Card in regulation is the allowable voltage drop across the device, divided by the output-switch resistance.

$$I_O max = \frac{V_{DS}}{r_{DS(on)}}$$

The xVCC outputs have been designed to deliver the peak and average currents defined by the PC Card specification within regulation over the operating temperature range. The xVPP outputs have been designed to deliver 100 mA continuously.

OVERCURRENT AND OVERTEMPERATURE PROTECTION

PC Cards are inherently subject to damage that can result from mishandling. Host systems require protection against short-circuited cards that could lead to power-supply or PCB trace damage. Even extremely robust systems could undergo rapid battery discharge into a damaged PC Card, resulting in the rather sudden and unacceptable loss of system power. The reliability of fused systems is poor, in comparison, as blown fuses require troubleshooting and repair, usually by the manufacturer.

The TPS2204A, TPS2206A, and TPS2210A take a two-pronged approach to overcurrent protection. Overcurrent protection is designed to activate if an output is shorted or when an overcurrent condition is present when switches are powered up. First, instead of fuses, sense FETs monitor each of the xVCC and xVPP power outputs. Unlike sense resistors or polyfuses, these FETs do not add to the series resistance of the switch; therefore voltage and power losses are reduced. Overcurrent sensing is applied to each output separately. Excessive current generates an error signal that limits the output current of only the affected output, preventing damage to the host. Each xVCC output overcurrent limits from 1 A to 2.2 A, typically around 1.6 A; the xVPP outputs limit from 100 mA to 250 mA, typically around 200 mA.

Second, when an overcurrent condition is detected, the device asserts an active low $\overline{\text{OC}}$ signal that can be monitored by the microprocessor or controller to initiate diagnostics and/or send the user a warning message. If an overcurrent condition persists, causing the IC to exceed its maximum junction temperature, thermal-protection circuitry activates, shutting down all power outputs until the device cools to within a safe operating region, which is ensured by a thermal shutdown hysteresis. Thermal limiting prevents destruction of the IC from overheating beyond the package power-dissipation ratings.

During power up, the devices control the rise times of the xVCC and xVPP outputs and limit the inrush current into a large load capacitance, faulty card, or connector.

12-V SUPPLY NOT REQUIRED

Some PC Card switches use the externally supplied 12 V to power gate drive and other chip functions, which requires that power be present at all times. The TPS2204A, TPS2206A, and TPS2210A offer considerable power savings by using an internal charge pump to generate the required higher gate drive voltages from the 3.3-V input. Therefore, the external 12-V supply can be disabled except when needed by the PC Card in the slot, thereby extending battery lifetime. A special feature in the 12-V circuitry actually helps to reduce the supply current demanded from the 3.3-V input. When 12 V is supplied and requested at the V_{pp} output, a voltage selection circuit draws the charge-pump drive current for the 12-V FETs from the 12-V input. This selection is automatic and effectively reduces demand fluctuations on the normal 3.3-V V_{CC} rail. For proper operation of this feature, a minimum 3.3-V input capacitance of 4.7 µF is recommended, and a minimum 12-V input ramp-up rate of 12 V/50 ms (240 V/s) is required. Additional power savings are realized during a software shutdown in which quiescent current drops to a maximum of 1 µA.

BACKWARD COMPATIBILITY

The TPS2206A is backward compatible with the TPS2206 product, with the following considerations. An active low /SHDN is added to provide fast shutdown capability. Also, the TPS2206A does not have the active−high RESET input, which is left as no connect.

3.3–V input is required for device operation of TPS2206A.

VOLTAGE-TRANSITIONING REQUIREMENT

PC Cards, like portables, are migrating from 5 V to 3.3 V to minimize power consumption, optimize board space, and increase logic speeds. The TPS2204A, TPS2206A, and TPS2210A meet all combinations of power delivery as currently defined in the PCMCIA standard. The latest protocol accommodates mixed 3.3-V/5-V systems by first powering the card with 5 V, then polling it to determine its 3.3-V compatibility. The PCMCIA specification requires that the capacitors on 3.3-V-compatible cards be discharged to below 0.8 V before applying 3.3-V power. This action ensures that sensitive 3.3-V circuitry is not subjected to any residual 5-V charge and functions as a power $\overline{\text{RESET}}$. PC Card specification requires that V_{CC} be discharged within 100 ms. PC Card resistance cannot be relied on to provide a discharge path for voltages stored on PC Card capacitance because of possible high-impedance isolation by power-management schemes. The devices include discharge transistors on all xVCC and xVPP outputs to meet the specification requirement.

SHUTDOWN MODE

In the shutdown mode, which can be controlled by $\overline{\text{SHDN}}$ or bit D8 of the input serial DATA word, each of the xVCC and xVPP outputs is forced to a high-impedance state. In this mode, the chip quiescent current is reduced to 1 µA or less to conserve battery power.

POWER-SUPPLY CONSIDERATIONS

These switches have multiple pins for each 3.3-V (except for the TPS2210A) and 5-V power input and for the switched xVCC outputs. Any individual pin can conduct the rated input or output current. Unless all pins are connected in parallel, the series resistance is higher than that specified, resulting in increased voltage drops and power loss. It is recommended that all input and output power pins be paralleled for optimum operation.

To increase the noise immunity of the TPS2204A, TPS2206A, and TPS2210A, the power-supply inputs should be bypassed with at least a 4.7-µF electrolytic or tantalum capacitor paralleled by a 0.047-µF to 0.1-µF ceramic capacitor. It is strongly recommended that the switched outputs be bypassed with a 0.1-µF (or larger) ceramic capacitor; doing so improves the immunity of the IC to electrostatic discharge (ESD). Care should be taken to minimize the inductance of PCB traces between the devices and the load. High switching currents can produce large negative voltage transients, which forward biases substrate diodes, resulting in unpredictable performance. Similarly, no pin should be taken below −0.3 V.

$\overline{\text{RESET}}$ INPUT

To ensure that cards are in a known state after power brownouts or system initialization, the PC Cards should be reset at the same time as the host by applying low-impedance paths from xVCC and xVPP terminals to ground. A low-impedance output state allows discharging of residual voltage remaining on PC Card filter capacitance, permitting the system (host and PC Cards) to be powered up concurrently. The active low $\overline{\text{RESET}}$ input closes internal ground switches S1, S4, S7, and S11 with all other switches left open. The devices remain in the low-impedance output state until the signal is deasserted and new data is clocked in and latched. The input serial data cannot be latched during reset mode. $\overline{\text{RESET}}$ is provided for direct compatibility with systems that use an active-low reset voltage supervisor. The $\overline{\text{RESET}}$ pin has an internal 150-kΩ pullup resistor.

CALCULATING JUNCTION TEMPERATURE

The switch resistance, $r_{DS(on)}$, is dependent on the junction temperature, T_J, of the die. The junction temperature is dependent on both $r_{DS(on)}$ and the current through the switch. To calculate T_J, first find $r_{DS(on)}$ from Figures 26 through 28, using an initial temperature estimate about 30°C above ambient. Then calculate the power dissipation for each switch, using the formula:

$$P_D = r_{DS(on)} \times I^2$$

Next, sum the power dissipation of all switches and calculate the junction temperature:

$$T_J = \left(\sum P_D \times R_{\theta JA}\right) + T_A,\ R_{\theta JA} = 108°C/W$$

Compare the calculated junction temperature with the initial temperature estimate. If the temperatures are not within a few degrees of each other, recalculate using the calculated temperature as the initial estimate.

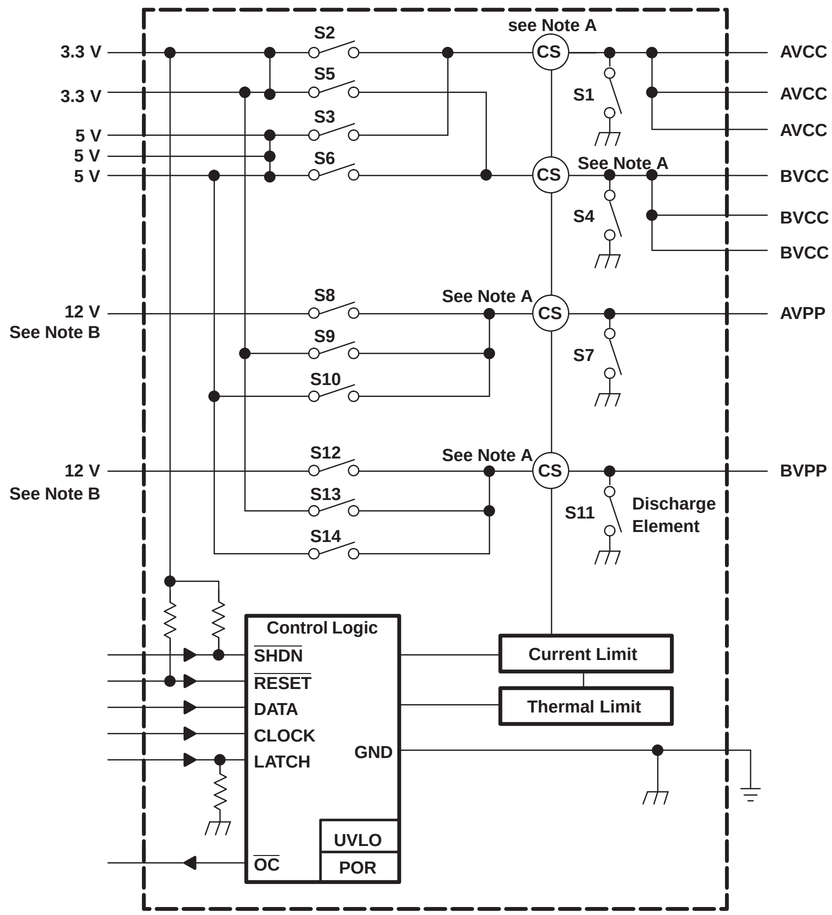
LOGIC INPUTS AND OUTPUTS

The serial interface consists of the DATA, CLOCK, and LATCH leads. The data is clocked in on the positive edge of the clock (see Figure 2). The 9-bit (D0−D8) serial data word is loaded during the positive edge of the latch signal. The latch signal should occur before the next positive edge of the clock.

The shutdown bit of the data word places all V_{CC} and V_{pp} outputs in a high-impedance state and reduces chip quiescent current to 1 μA to conserve battery power.

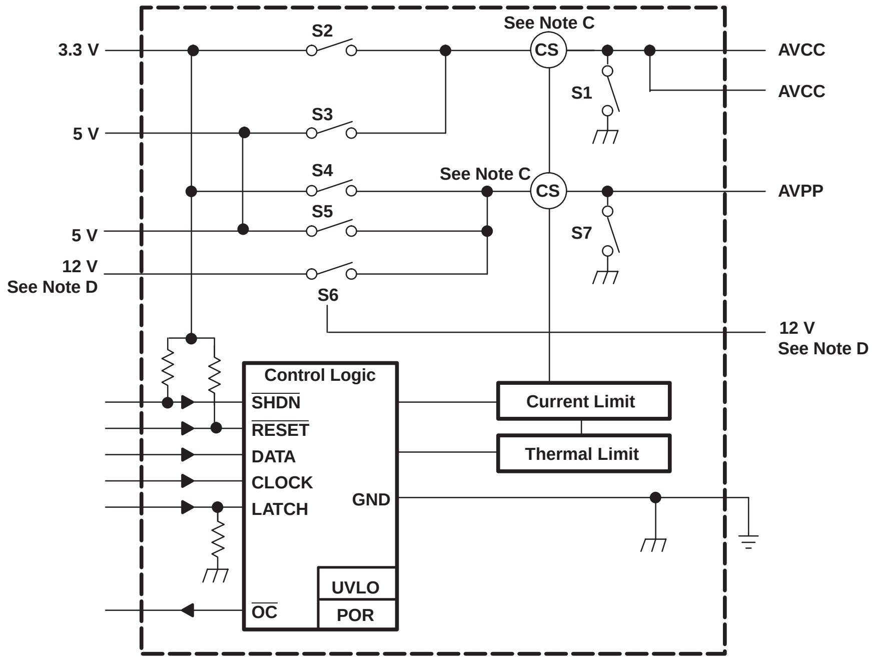
The serial interface is designed to be compatible with serial-interface PCMCIA controllers and current PCMCIA and Japan Electronic Industry Development Association (JEIDA) standards.

An overcurrent output ($\overline{OC}$) is provided to indicate an overcurrent or overtemperature condition in any of the V_{CC} and V_{PP} outputs as previously discussed.



NOTES: A. Current sense
B. The two 12-V pins must be externally connected.

Figure 35. Internal Switching Matrix, TPS2204A and TPS2206A



NOTES: C. Current sense
D. The two 12-V pins must be externally connected.

Figure 36. Internal Switching Matrix, TPS2210A

CONTROL LOGIC

AVPP

CONTROL SIGNALS			OUTPUT
D8 ($\overline{\text{SHDN}}$)	**D0**	**D1**	**VAVPP**
1	0	0	0 V
1	0	1	AVCC[1]
1	1	0	12 V
1	1	1	Hi–Z
0	X	X	Hi–Z

(1) Output depends on AVCC

BVPP

CONTROL SIGNALS			OUTPUT
D8 $\overline{\text{SHDN}}$)	**D4**	**D5**	**VBVPP**
1	0	0	0 V
1	0	1	BVCC[2]
1	1	0	12 V
1	1	1	Hi–Z
0	X	X	Hi–Z

(2) Output depends on BVCC

AVCC

CONTROL SIGNALS			OUTPUT
D8 $\overline{\text{SHDN}}$)	**D3**	**D2**	**VAVCC**
1	0	0	0 V
1	0	1	3.3 V
1	1	0	5 V
1	1	1	0 V
0	X	X	Hi–Z

BVCC

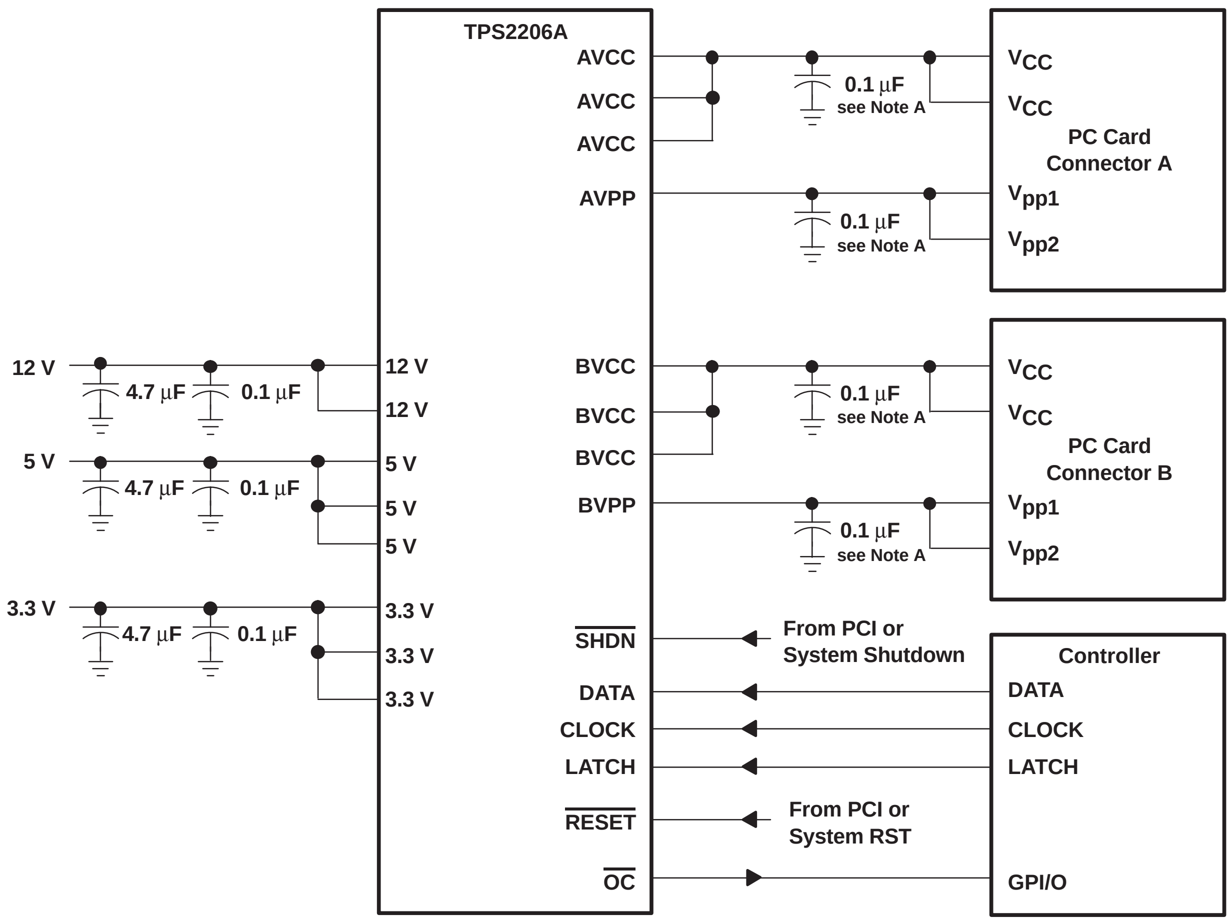
CONTROL SIGNALS			OUTPUT
D8 $\overline{\text{SHDN}}$)	**D6**	**D7**	**VBVCC**
1	0	0	0 V
1	0	1	3.3 V
1	1	0	5 V
1	1	1	0 V
0	X	X	Hi–Z

USING THE DEVICES WITH 11-BIT SERIAL DATA INTERFACE CONTROLLERS

Even though the control logic table only shows a 9-bit interface, it can be used with most 11-bit serial data interface controllers. With the use of the latch input, the TPS2204A, TPS2206A, and TPS2210A only latch the last 9 bits from the serial stream. This means that for an 11-bit serial stream, bits 9 and 10 are ignored. 11-bit serial interface controllers use bits 9 and 10 for independent voltage selection of 3.3 V and 5 V between xV_{CC} and xV_{PP}.

ESD PROTECTIONS (see FIGURE 37)

All TPS2206A inputs and outputs of these devices incorporate ESD-protection circuitry designed to withstand a 2-kV human-body-model discharge as defined in MIL-STD-883C, Method 3015. The xVCC and xVPP outputs can be exposed to potentially higher discharges from the external environment through the PC Card connector. Bypassing the outputs with 0.1-µF capacitors protects the devices from discharges up to 10 kV.



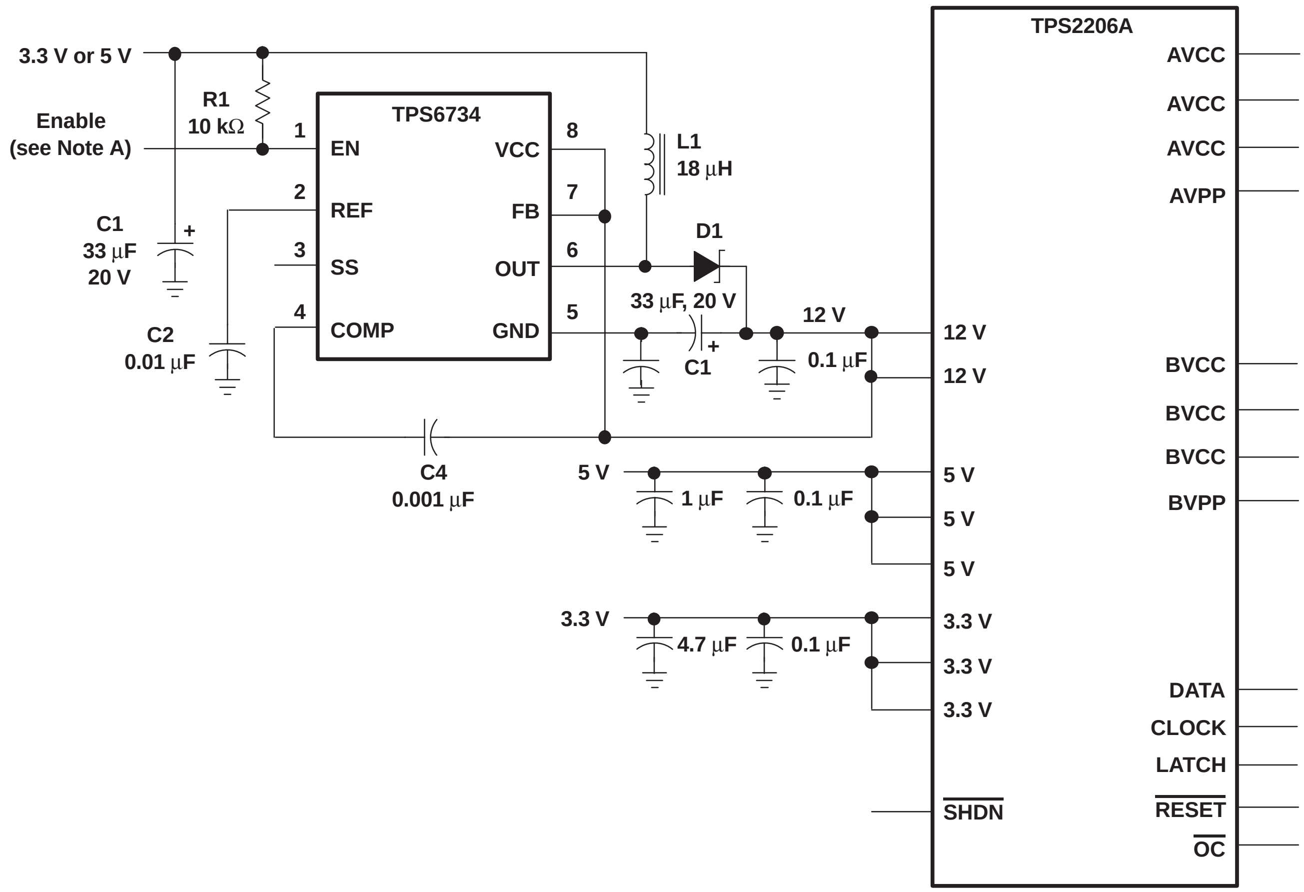
NOTE A: Maximum recommended output capacitance for xVCC is 220 µF including card capacitance, and for xVPP is 10 µF, without $\overline{OC}$ glitch when switches are powered on.

Figure 37. Detailed Interconnections and Capacitor Recommendations

12-V FLASH MEMORY SUPPLY

The TPS6734 is a fixed 12-V output boost converter capable of delivering 120 mA from inputs as low as 2.7 V. The device is pin-for-pin compatible with the MAX734 regulator and offers the following advantages: lower supply current, wider operating input-voltage range, and higher output currents. As shown in Figure 36, the only external components required are: an inductor, a Schottky rectifier, an output filter capacitor, an input filter capacitor, and a small capacitor for loop compensation. The entire converter occupies less than 0.7 in^2 of PCB space when implemented with surface-mount components. An enable input is provided to shut the converter down and reduce the supply current to 3 µA when 12 V is not needed.

The TPS6734 is a 170-kHz current-mode PWM (pulse-width modulation) controller with an n-channel MOSFET power switch. Gate drive for the switch is derived from the 12-V output after start-up to minimize the die area needed to realize the 0.7-Ω MOSFET and improve efficiency at input voltages below 5 V. Soft start is accomplished with the addition of one small capacitor. A 1.22-V reference, pin 2 of TPS6734, is brought out for external use. For additional information, see the TPS6734 data sheet (SLVS127).



NOTE A: The enable terminal can be tied to a general-purpose I/O terminal on the PCMCIA controller or tied high.

Figure 38. TPS2206A With TPS6734 12-V, 120-mA Supply

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPS2204APWP	ACTIVE	HTSSOP	PWP	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Request Free Samples
TPS2204APWPG4	ACTIVE	HTSSOP	PWP	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Request Free Samples
TPS2206ADAP	ACTIVE	HTSSOP	DAP	32	46	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Request Free Samples
TPS2206ADAPG4	ACTIVE	HTSSOP	DAP	32	46	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Request Free Samples
TPS2206ADB	ACTIVE	SSOP	DB	30	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
TPS2206ADBG4	ACTIVE	SSOP	DB	30	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
TPS2206ADBR	ACTIVE	SSOP	DB	30	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
TPS2206ADBRG4	ACTIVE	SSOP	DB	30	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
TPS2210APWP	ACTIVE	HTSSOP	PWP	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Request Free Samples
TPS2210APWPG4	ACTIVE	HTSSOP	PWP	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Request Free Samples
TPS2210APWPR	ACTIVE	HTSSOP	PWP	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples
TPS2210APWPRG4	ACTIVE	HTSSOP	PWP	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

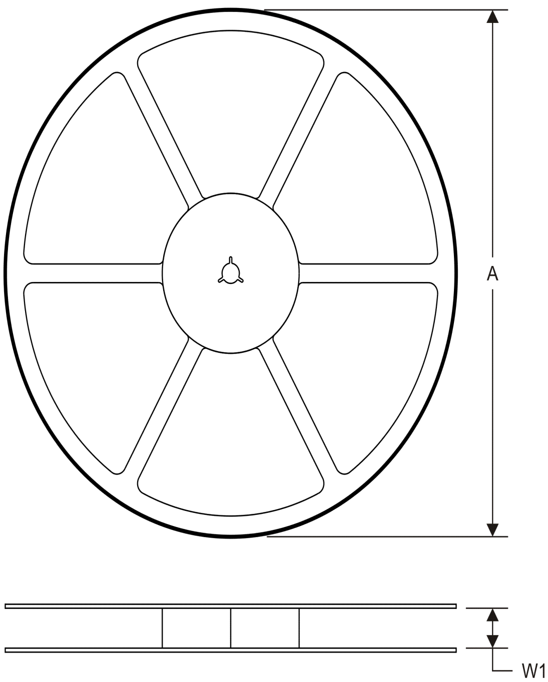
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

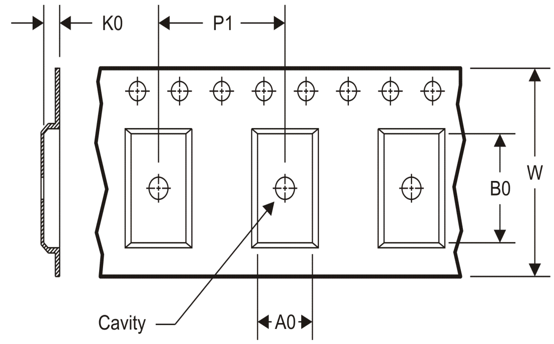
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



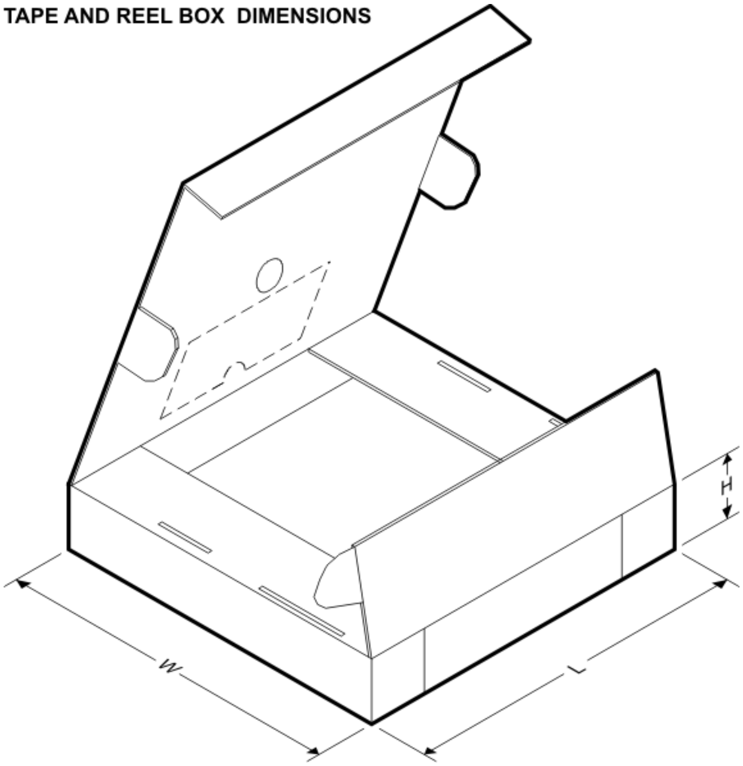
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2206ADBR	SSOP	DB	30	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TPS2210APWPR	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

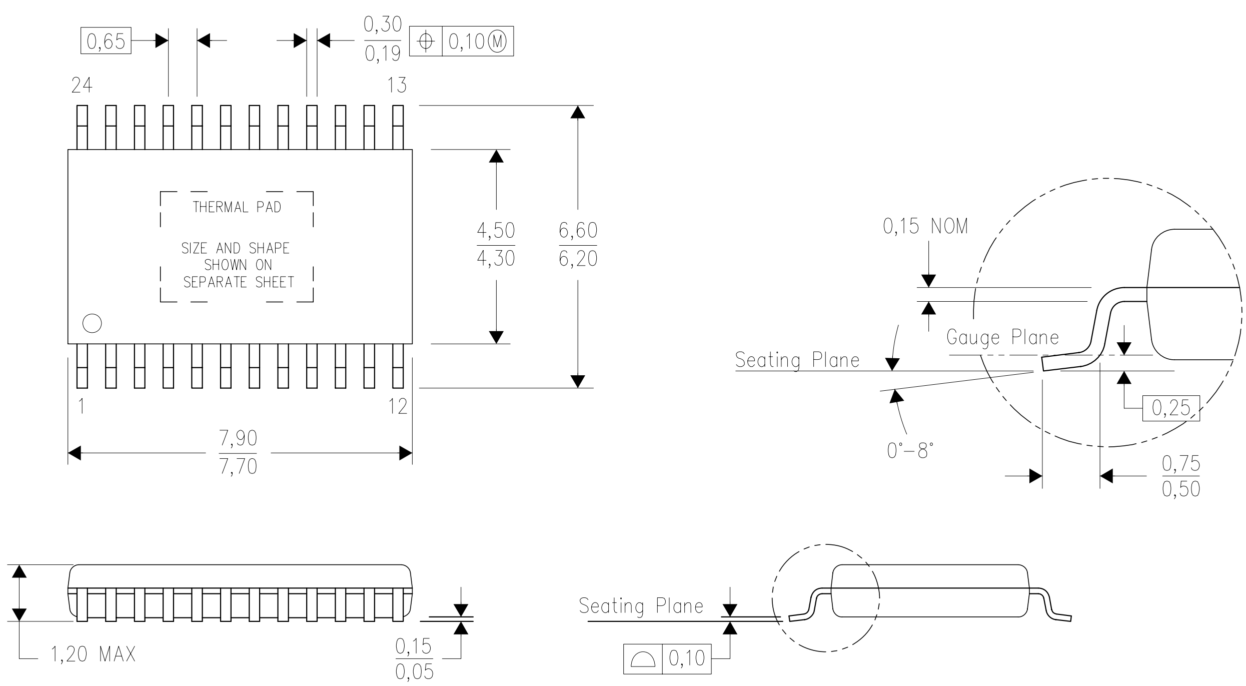
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2206ADBR	SSOP	DB	30	2000	367.0	367.0	38.0
TPS2210APWPR	HTSSOP	PWP	24	2000	367.0	367.0	38.0

PWP (R-PDSO-G24) PowerPAD™ PLASTIC SMALL OUTLINE



4073225-5/I 05/11

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

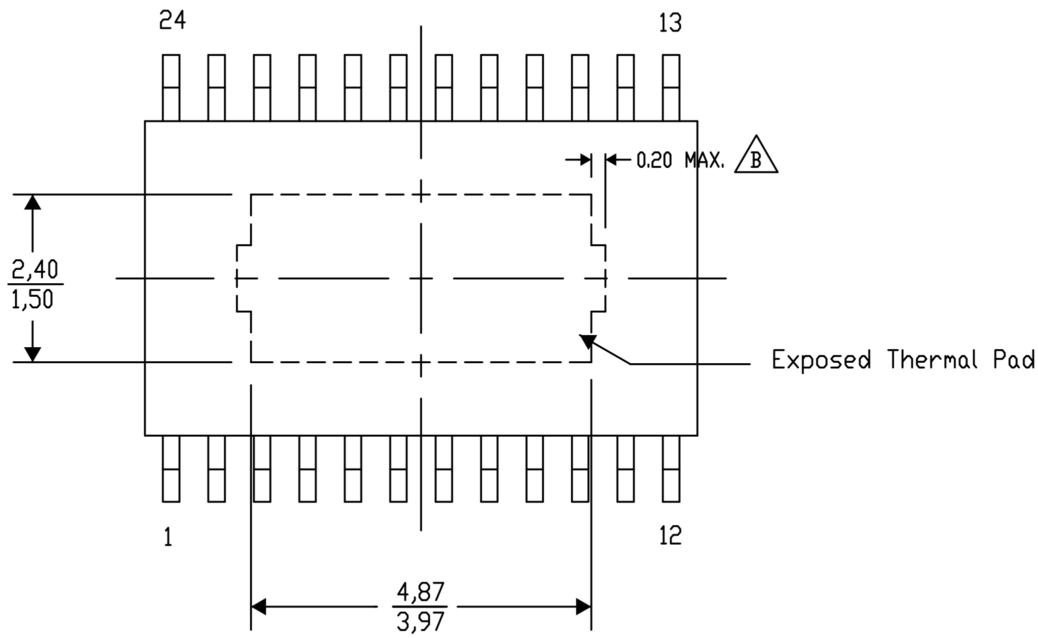
PWP (R-PDSO-G24) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

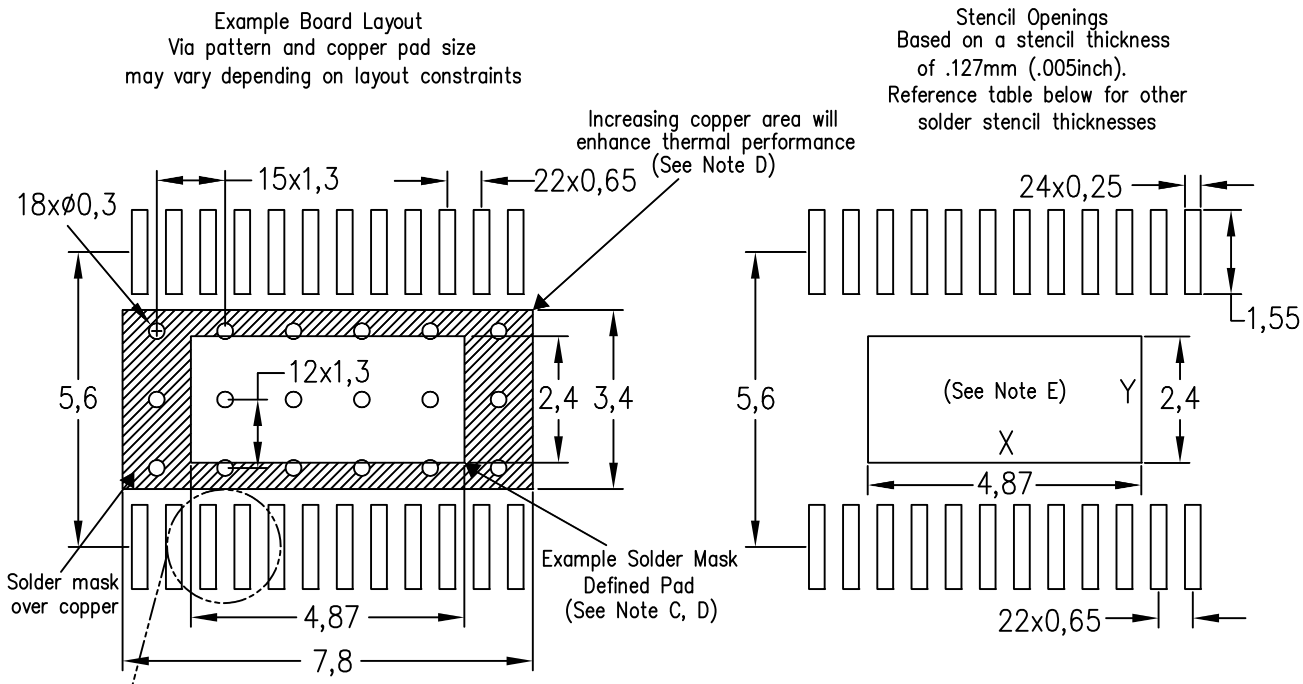
Exposed Thermal Pad Dimensions

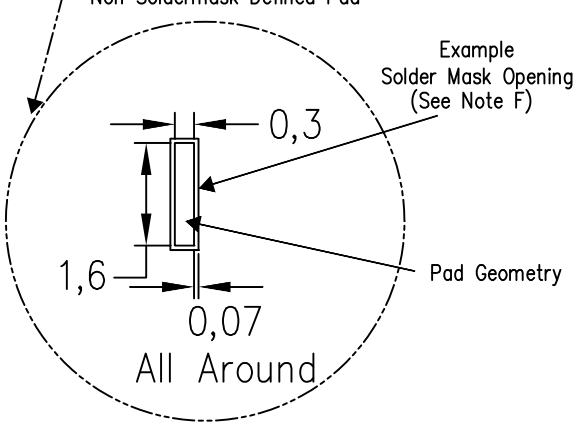
4206332-29/AC 07/12

NOTE: A. All linear dimensions are in millimeters
B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G24) PowerPAD™ PLASTIC SMALL OUTLINE



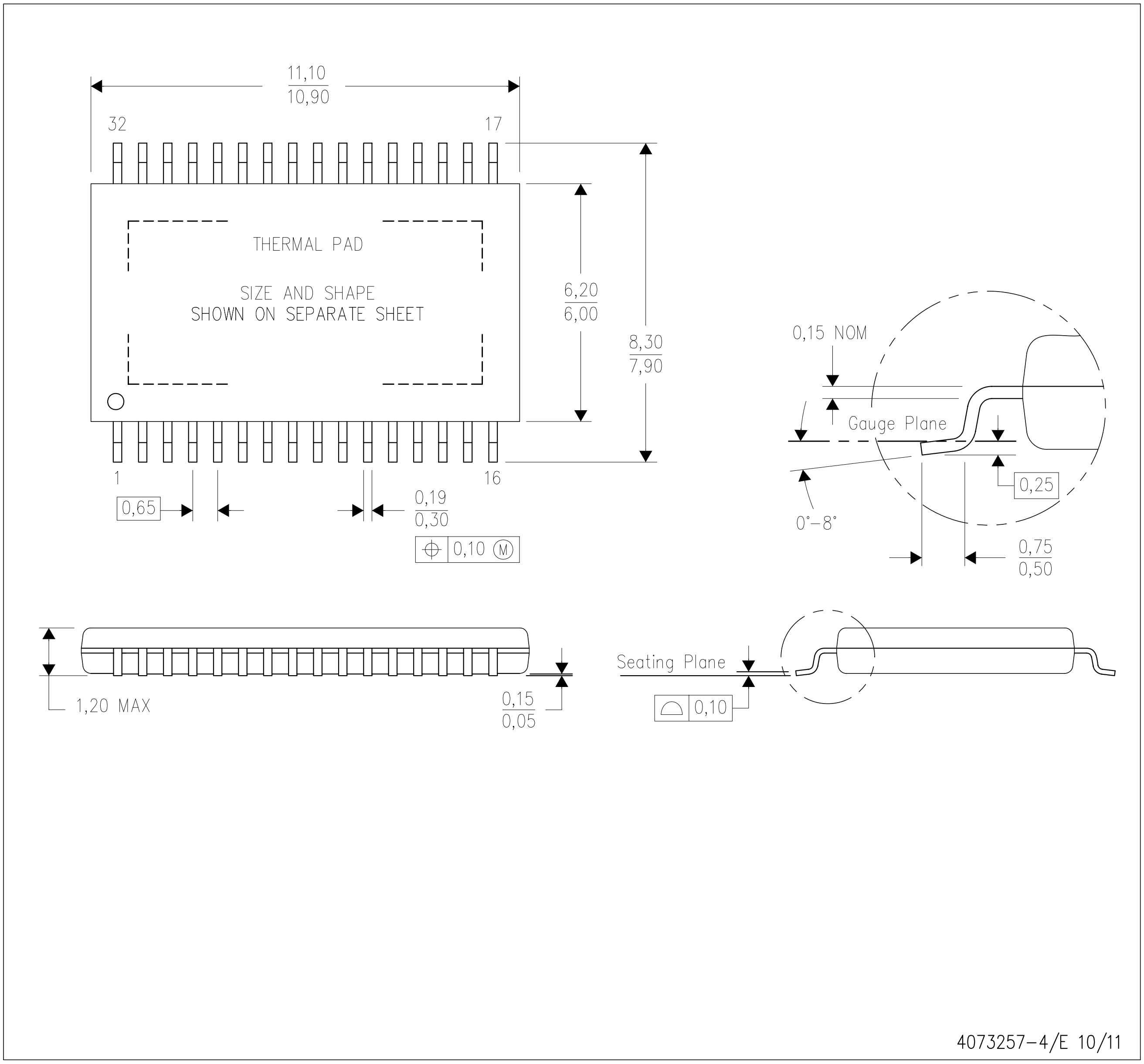


Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	5.4	2.6
0.127mm	4.87	2.4
0.152mm	4.6	2.2
0.178mm	4.3	2.1

4207609–16/R 07/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DAP (R-PDSO-G32) PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
F. Falls within JEDEC MO-153 Variation DCT.

PowerPAD is a trademark of Texas Instruments.

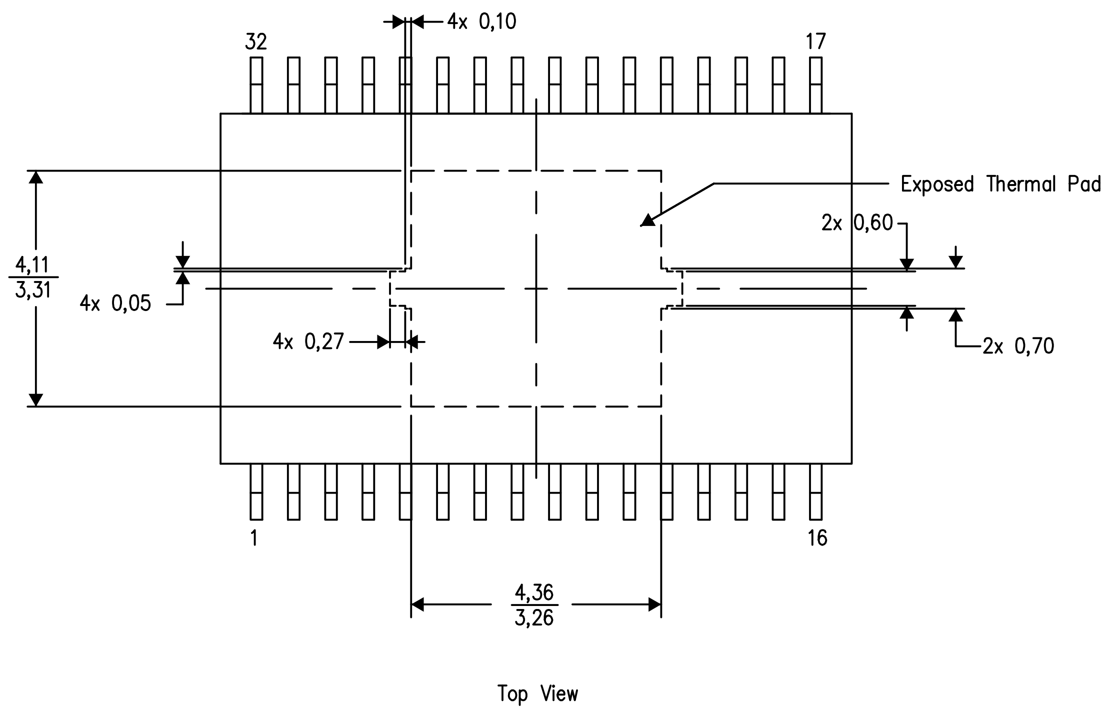
DAP (R–PDSO–G32) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

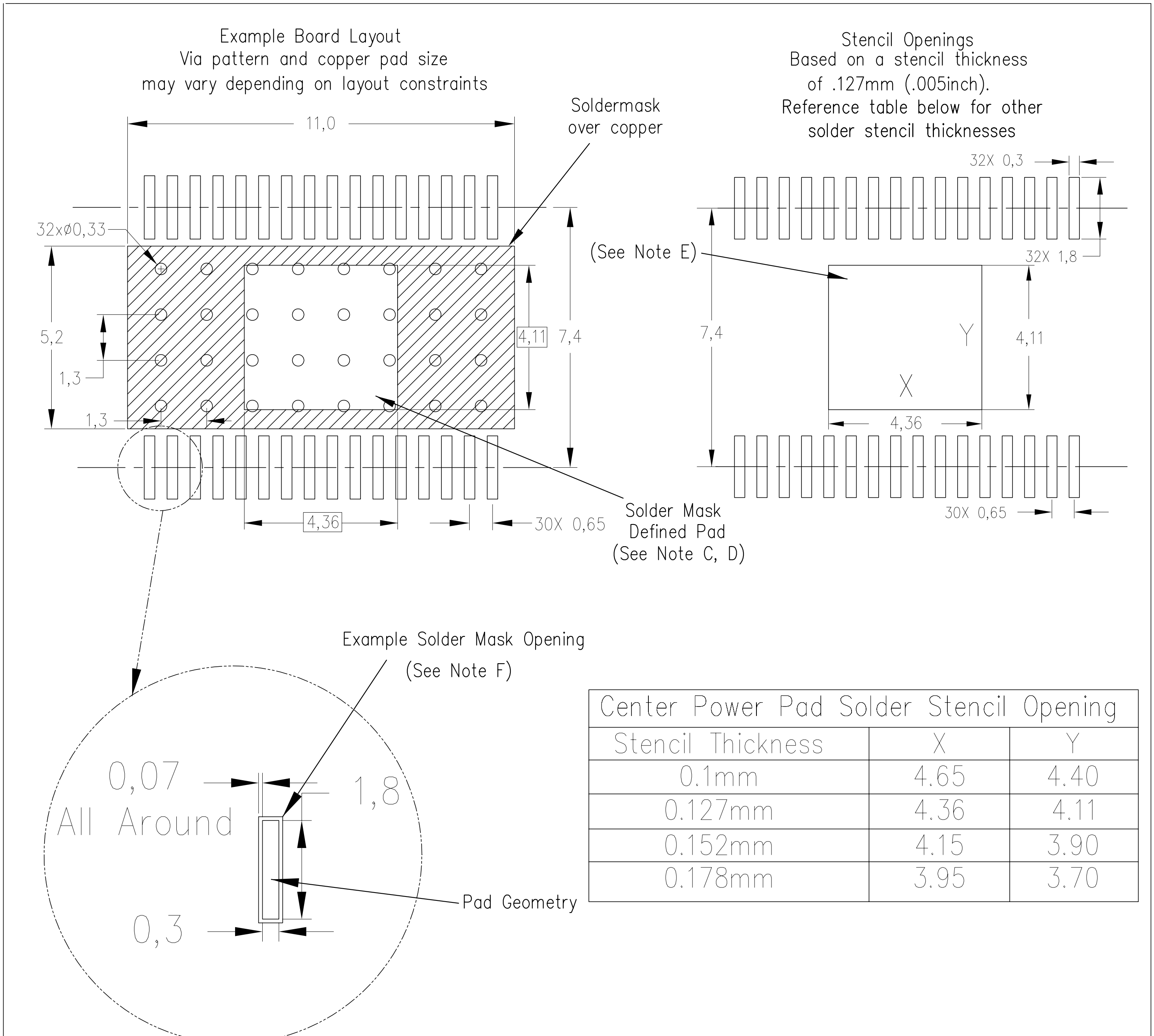


Exposed Thermal Pad Dimensions

4206319–3/K 04/12

NOTE: All linear dimensions are in millimeters

DAP (R-PDSO-G32) PowerPAD™ PLASTIC SMALL OUTLINE PACKAGE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	4.65	4.40
0.127mm	4.36	4.11
0.152mm	4.15	3.90
0.178mm	3.95	3.70

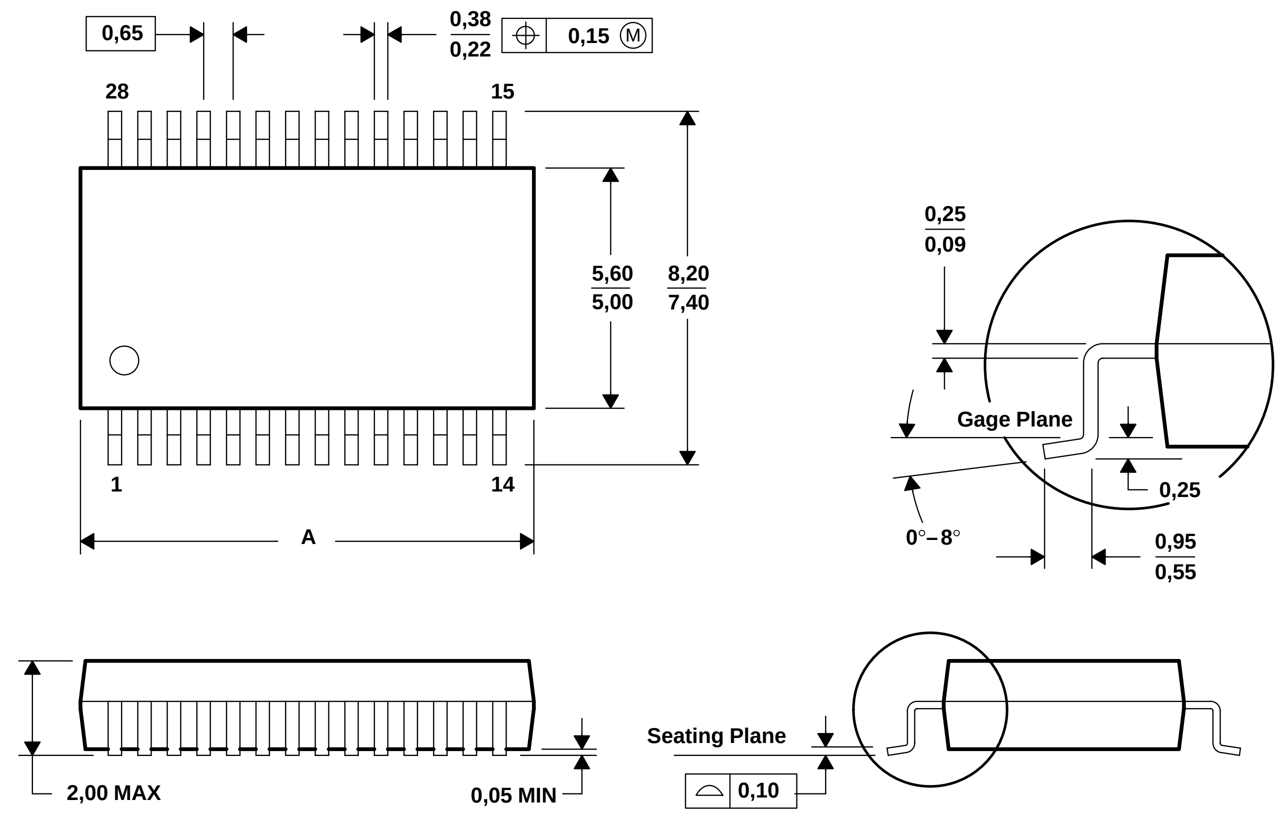
4210213-2/D 02/12

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
- F. Contact the board fabrication site for recommended soldermask tolerances.

PowerPAD is a trademark of Texas Instruments

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



PINS ** / DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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