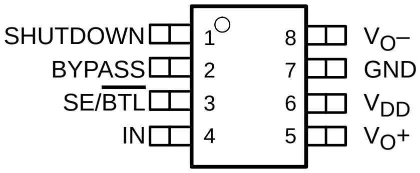
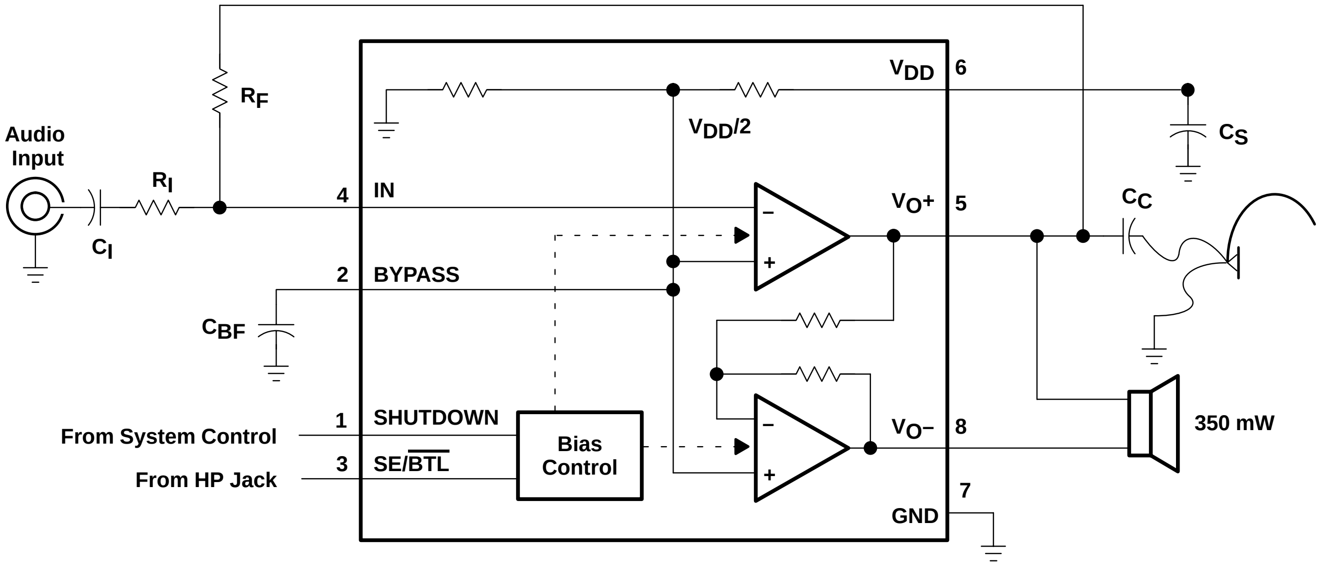
- **Fully Specified for 3.3-V and 5-V Operation**
- **Wide Power Supply Compatibility 2.5 V – 5.5 V**
- **Output Power for R_L = 8 Ω**
  - **350 mW at V_{DD} = 5 V, BTL**
  - **250 mW at V_{DD} = 5 V, SE**
  - **250 mW at V_{DD} = 3.3 V, BTL**
  - **75 mW at V_{DD} = 3.3 V, SE**
- **Shutdown Control**
  - **I_{DD} = 7 μA at 3.3 V**
  - **I_{DD} = 60 μA at 5 V**
- **BTL to SE Mode Control**
- **Integrated Depop Circuitry**
- **Thermal and Short-Circuit Protection**
- **Surface Mount Packaging**
  - **SOIC**
  - **PowerPAD™ MSOP**

D OR DGN PACKAGE
(TOP VIEW)



description

The TPA311 is a bridge-tied load (BTL) or single-ended (SE) audio power amplifier developed especially for low-voltage applications where internal speakers and external earphone operation are required. Operating with a 3.3-V supply, the TPA311 can deliver 250-mW of continuous power into a BTL 8-Ω load at less than 1% THD+N throughout voice band frequencies. Although this device is characterized out to 20 kHz, its operation was optimized for narrower band applications such as cellular communications. The BTL configuration eliminates the need for external coupling capacitors on the output in most applications, which is particularly important for small battery-powered equipment. A unique feature of the TPA311 is that it allows the amplifier to switch from BTL to SE *on the fly* when an earphone drive is required. This eliminates complicated mechanical switching or auxiliary devices just to drive the external load. This device features a shutdown mode for power-sensitive applications with special depop circuitry to virtually eliminate speaker noise when exiting shutdown mode and during power cycling. The TPA311 is available in an 8-pin SOIC surface-mount package and the surface-mount PowerPAD MSOP, which reduces board space by 50% and height by 40%.



PowerPAD is a trademark of Texas Instruments.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES		MSOP Symbolization
	SMALL OUTLINE[†] (D)	MSOP[†] (DGN)	
–40°C to 85°C	TPA311D	TPA311DGN	AAB

[†] The D and DGN packages are available taped and reeled. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA311DR).

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BYPASS	2	I	BYPASS is the tap to the voltage divider for internal mid-supply bias. This terminal should be connected to a 0.1-µF to 1-µF capacitor when used as an audio amplifier.
GND	7		GND is the ground connection.
IN	4	I	IN is the audio input terminal.
SE/$\overline{\text{BTL}}$	3	I	When SE/$\overline{\text{BTL}}$ is held low, the TPA311 is in BTL mode. When SE/$\overline{\text{BTL}}$ is held high, the TPA311 is in SE mode.
SHUTDOWN	1	I	SHUTDOWN places the entire device in shutdown mode when held high (I_{DD} = 60 µA, V_{DD} = 5 V).
V_{DD}	6		V_{DD} is the supply voltage terminal.
V_O+	5	O	V_O+ is the positive output for BTL and SE modes.
V_O-	8	O	V_O- is the negative output in BTL mode and a high-impedance output in SE mode.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[‡]

Supply voltage, V_{DD}	6 V
Input voltage, V_I	–0.3 V to V_{DD} +0.3 V
Continuous total power dissipation	internally limited (see Dissipation Rating Table)
Operating free-air temperature range, T_A (see Table 3)	–40°C to 85°C
Operating junction temperature range, T_J	–40°C to 150°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

[‡] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$	DERATING FACTOR	T_A = 70°C	T_A = 85°C
D	725 mW	5.8 mW/°C	464 mW	377 mW
DGN	2.14 W[§]	17.1 mW/°C	1.37 W	1.11 W

[§] Please see the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (literature number SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of the before mentioned document.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		2.5	5.5	V
High-level voltage, V_{IH}	SHUTDOWN	0.9 V_{DD}		V
	$SE/\overline{BTL}$	0.9 V_{DD}		
Low-level voltage, V_{IL}	SHUTDOWN		0.1 V_{DD}	V
	$SE/\overline{BTL}$		0.1 V_{DD}	
Operating free-air temperature, T_A (see Table 3)		–40	85	°C

electrical characteristics at specified free-air temperature, $V_{DD} = 3.3$ V, $T_A = 25°$C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\|V_{OO}\|$	Output offset voltage (measured differentially)	SHUTDOWN = 0 V, $SE/\overline{BTL}$ = 0 V, $R_L = 8\ \Omega$, $R_F = 10\ k\Omega$			5	20	mV
PSRR	Power supply rejection ratio	V_{DD} = 3.2 V to 3.4 V	BTL mode		85		dB
			SE mode		83		
I_{DD}	Supply current (see Figure 6)	SHUTDOWN = 0 V, $SE/\overline{BTL}$ = 0.33 V, $R_F = 10\ k\Omega$	BTL mode		0.7	1.5	mA
		SHUTDOWN = 0 V, $SE/\overline{BTL}$ = 2.97 V, $R_F = 10\ k\Omega$	SE mode		0.35	0.75	
$I_{DD(SD)}$	Supply current, shutdown mode (see Figure 7)	SHUTDOWN = V_{DD}, $SE/\overline{BTL}$ = 0 V, $R_F = 10\ k\Omega$			7	50	µA
$\|I_{IH}\|$	High-level input current	SHUTDOWN, V_{DD} = 3.3 V, $V_I = V_{DD}$				1	µA
		$SE/\overline{BTL}$, V_{DD} = 3.3 V, $V_I = V_{DD}$				1	
$\|I_{IL}\|$	Low-level input current	SHUTDOWN, V_{DD} = 3.3 V, V_I = 0 V				1	µA
		$SE/\overline{BTL}$, V_{DD} = 3.3 V, V_I = 0 V				1	

operating characteristics, $V_{DD} = 3.3$ V, $T_A = 25°$C, $R_L = 8\ \Omega$

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
P_O	Output power, see Note 1	THD = 0.5%,	BTL mode,	See Figure 14		250		mW
		THD = 0.5%,	SE mode			110		
THD + N	Total harmonic distortion plus noise	P_O = 250 mW, See Figure 12	f = 20 Hz to 4 kHz,	A_V = – 2 V/V,		1.3%		
B_{OM}	Maximum output power bandwidth	A_V = – 2 V/V,	THD = 3%,	See Figure 12		10		kHz
B_1	Unity-gain bandwidth	Open loop,	See Figure 36			1.4		MHz
	Supply ripple rejection ratio	f = 1 kHz, See Figure 5	C_B = 1 µF,	BTL mode,		71		dB
		f = 1 kHz, See Figure 3	C_B = 1 µF,	SE mode,		86		
V_n	Noise output voltage	A_V = – 1 V/V, BTL,	C_B = 0.1 µF, See Figure 42	$R_L = 32\ \Omega$,		15		µV(rms)

NOTE 1: Output power is measured at the output terminals of the device at f = 1 kHz.

electrical characteristics at specified free-air temperature, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\lvert V_{OO} \rvert$	Output offset voltage (measured differentially)	SHUTDOWN = 0 V, SE/$\overline{\text{BTL}}$ = 0 V, R_L = 8 Ω, R_F = 10 kΩ			5	20	mV
PSRR	Power supply rejection ratio	V_{DD} = 4.9 V to 5.1 V	BTL mode		78		dB
			SE mode		76		
I_{DD}	Supply current (see Figure 6)	SHUTDOWN = 0 V, SE/$\overline{\text{BTL}}$ = 0.5 V, R_F = 10 kΩ	BTL mode		0.7	1.5	mA
		SHUTDOWN = 0 V, SE/$\overline{\text{BTL}}$ = 4.5 V, R_F = 10Ω	SE mode		0.35	0.75	
$I_{DD(SD)}$	Supply current, shutdown mode (see Figure 7)	SHUTDOWN = V_{DD}, SE/$\overline{\text{BTL}}$ = 0 V, R_F = 10 kΩ,			60	100	µA
$\lvert I_{IH} \rvert$	High-level input current	SHUTDOWN, V_{DD} = 5.5 V, V_I = V_{DD}				1	µA
		SE/$\overline{\text{BTL}}$, V_{DD} = 5.5 V, V_I = V_{DD}				1	
$\lvert I_{IL} \rvert$	Low-level input current	SHUTDOWN, V_{DD} = 5.5 V, V_I = 0 V				1	µA
		SE/$\overline{\text{BTL}}$, V_{DD} = 5.5 V, V_I = 0 V				1	

operating characteristics, V_{DD} = 5 V, T_A = 25°C, R_L = 8 Ω

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
P_O	Output power, see Note 2	THD = 0.5%,	BTL mode,	See Figure 18		700		mW
		THD = 0.5%,	SE mode			300		
THD + N	Total harmonic distortion plus noise	P_O = 350 mW, See Figure 16	f = 20 Hz to 4 kHz,	A_V = – 2 V/V,		1%		
B_{OM}	Maximum output power bandwidth	A_V = – 2 V/V,	THD = 2%,	See Figure 16		10		kHz
B_1	Unity-gain bandwidth	Open loop,	See Figure 37			1.4		MHz
	Supply ripple rejection ratio	f = 1 kHz, See Figure 5	C_B = 1 µF,	BTL mode,		65		dB
		f = 1 kHz, See Figure 4	C_B = 1 µF,	SE mode,		75		
V_n	Noise output voltage	A_V = – 1 V/V, BTL,	C_B = 0.1 µF, See Figure 43	R_L = 32 Ω,		15		µV(rms)

NOTE 2: Output power is measured at the output terminals of the device at f = 1 kHz.

PARAMETER MEASUREMENT INFORMATION

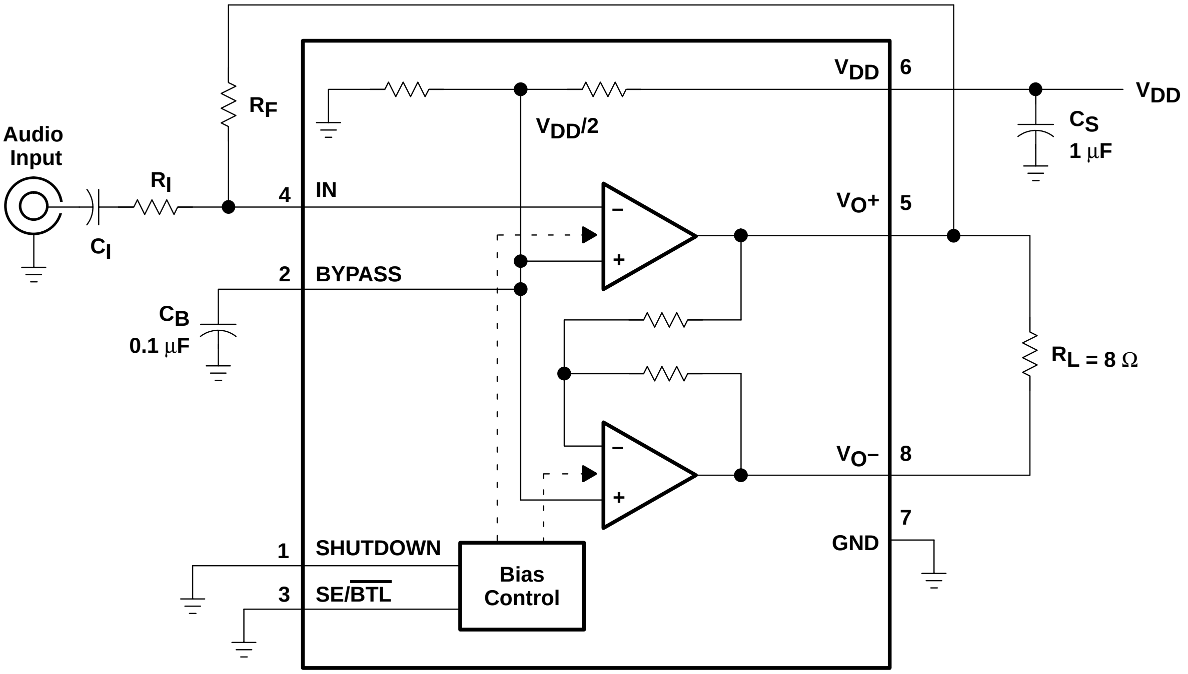


Figure 1. BTL Mode Test Circuit

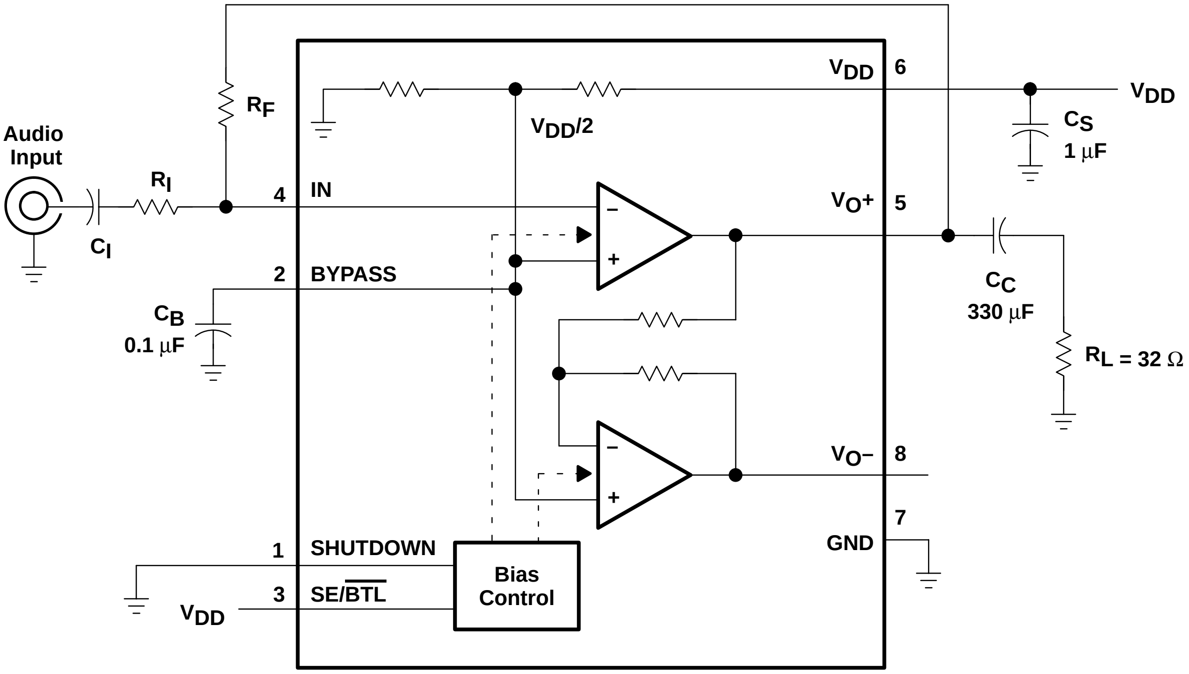


Figure 2. SE Mode Test Circuit

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
	Supply voltage rejection ratio	vs Frequency	3, 4, 5
I_{DD}	Supply current	vs Supply voltage	6, 7
P_O	Output power	vs Supply voltage	8, 9
		vs Load resistance	10, 11
THD + N	Total harmonic distortion plus noise	vs Frequency	12, 13, 16, 17, 20, 21, 24, 25, 28, 29, 32, 33
		vs Output power	14, 15, 18, 19, 22, 23, 26, 27, 30, 31, 34, 35
	Open loop gain and phase	vs Frequency	36, 37
	Closed loop gain and phase	vs Frequency	38, 39, 40, 41
V_n	Output noise voltage	vs Frequency	42, 43
P_D	Power dissipation	vs Output power	44, 45, 46, 47

SUPPLY VOLTAGE REJECTION RATIO
vs
FREQUENCY

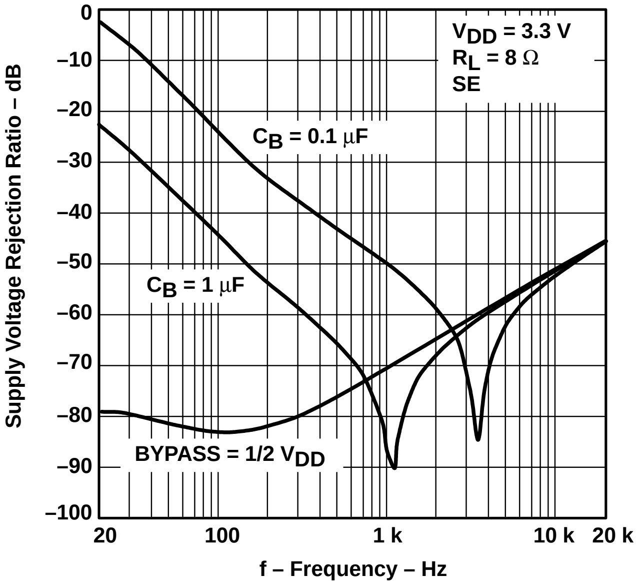


Figure 3

SUPPLY VOLTAGE REJECTION RATIO
vs
FREQUENCY

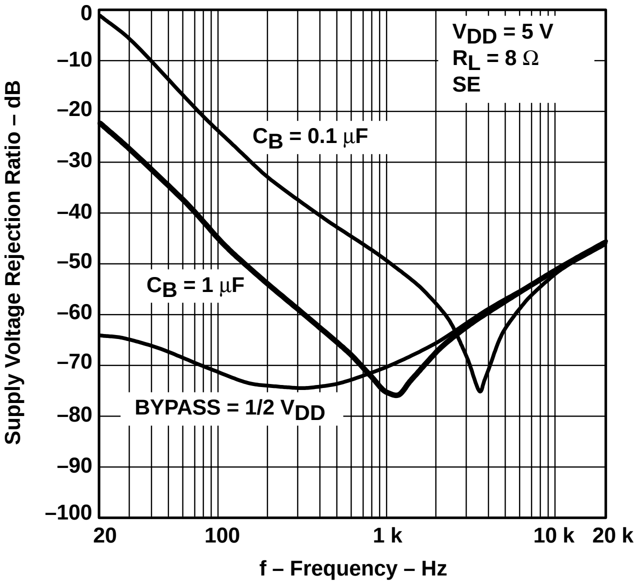


Figure 4

TYPICAL CHARACTERISTICS

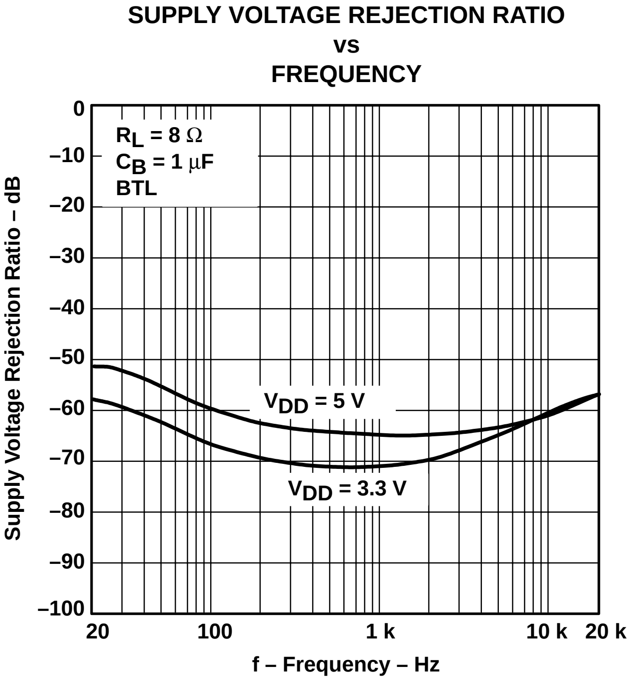


Figure 5

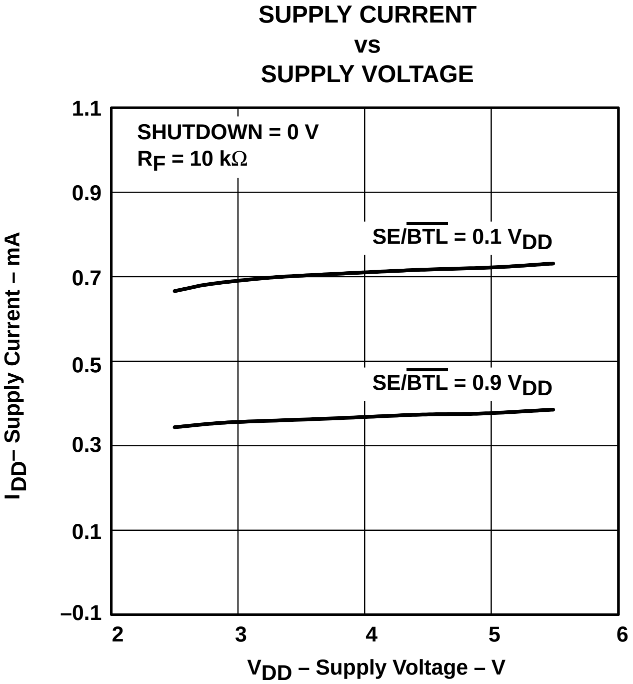


Figure 6

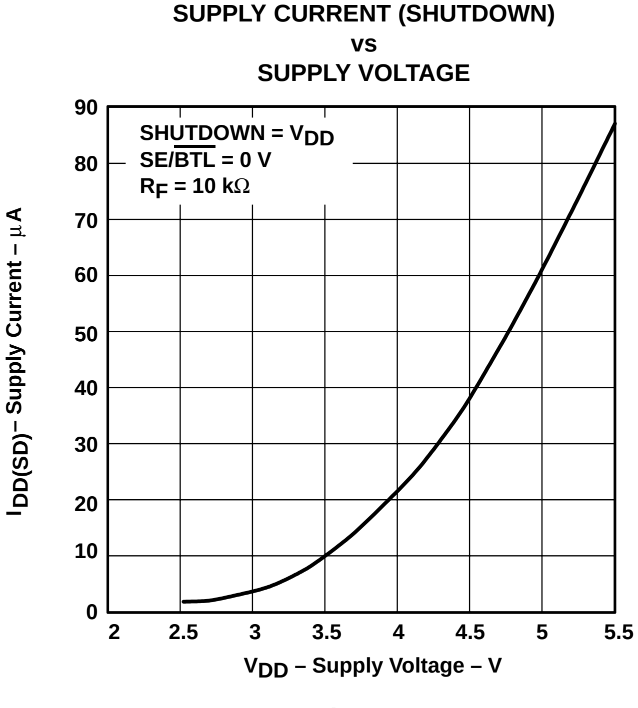


Figure 7

TYPICAL CHARACTERISTICS

OUTPUT POWER
vs
SUPPLY VOLTAGE

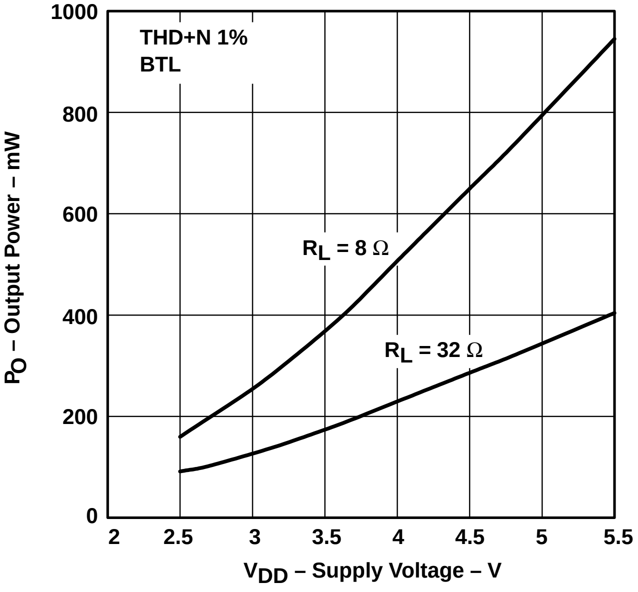


Figure 8

OUTPUT POWER
vs
SUPPLY VOLTAGE

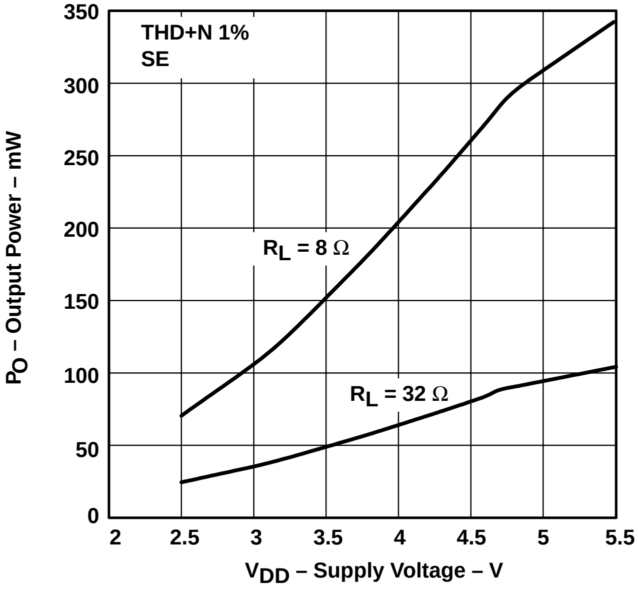


Figure 9

OUTPUT POWER
vs
LOAD RESISTANCE

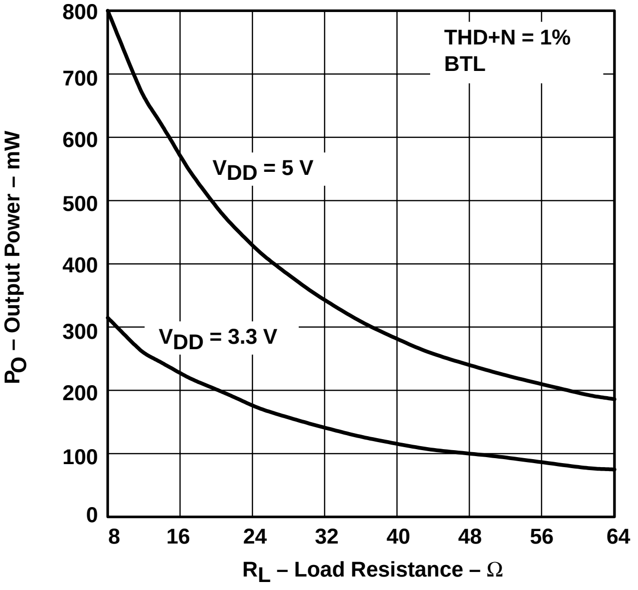


Figure 10

OUTPUT POWER
vs
LOAD RESISTANCE

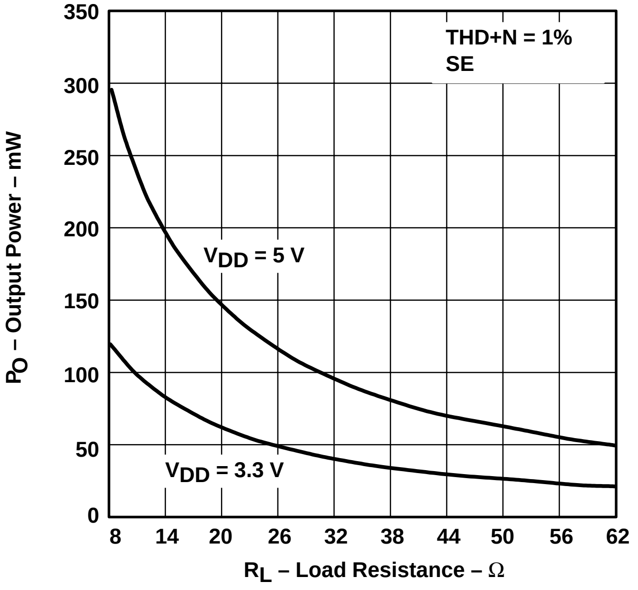


Figure 11

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

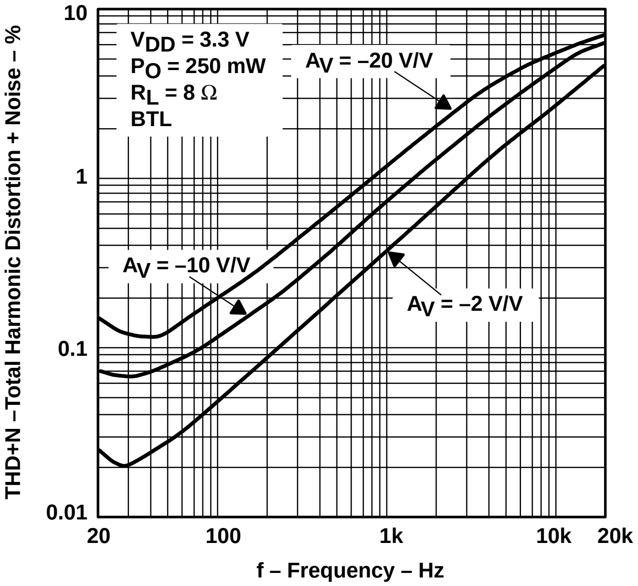


Figure 12

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

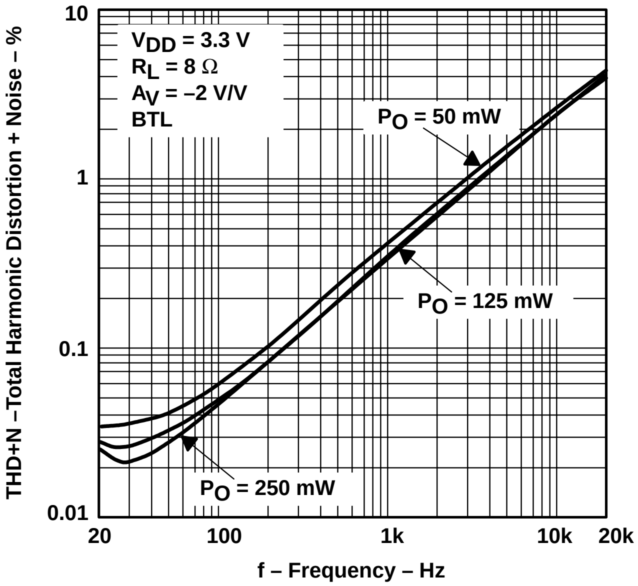


Figure 13

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

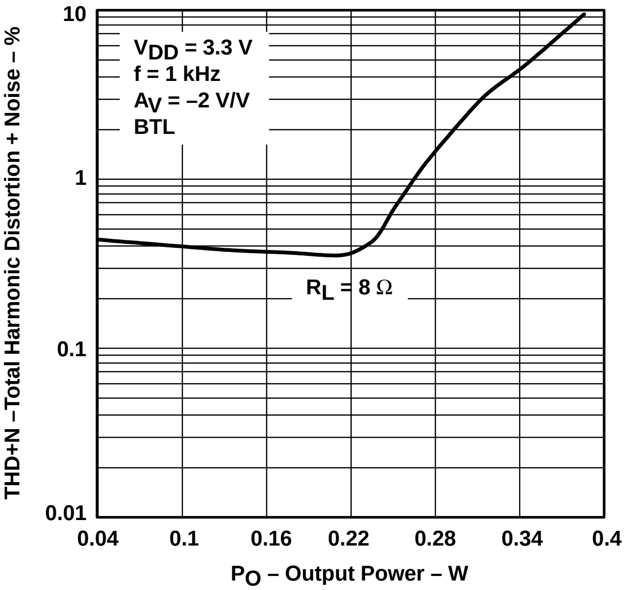


Figure 14

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

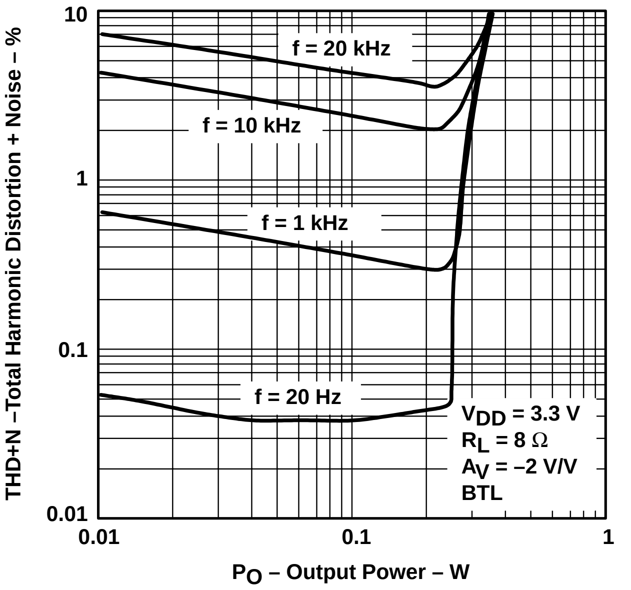


Figure 15

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

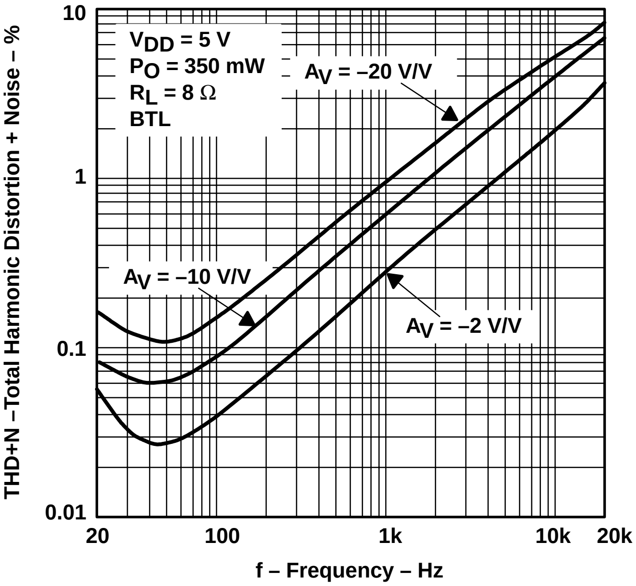


Figure 16

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

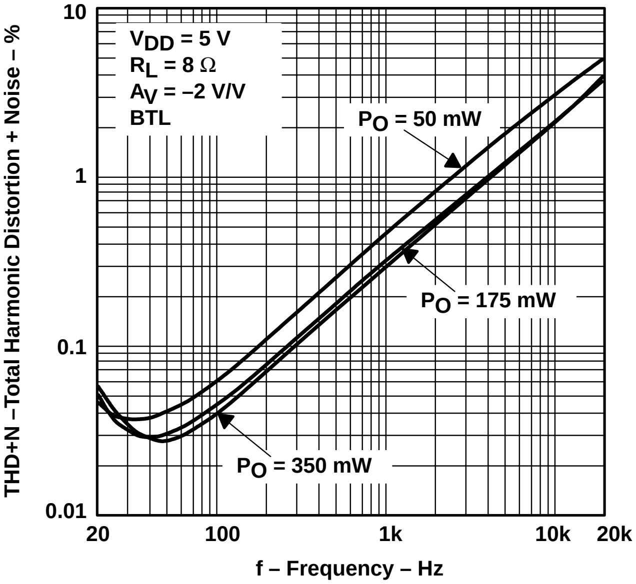


Figure 17

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

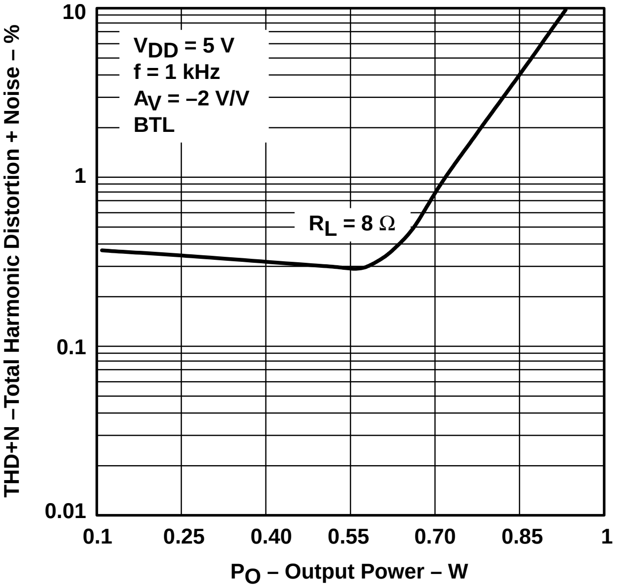


Figure 18

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

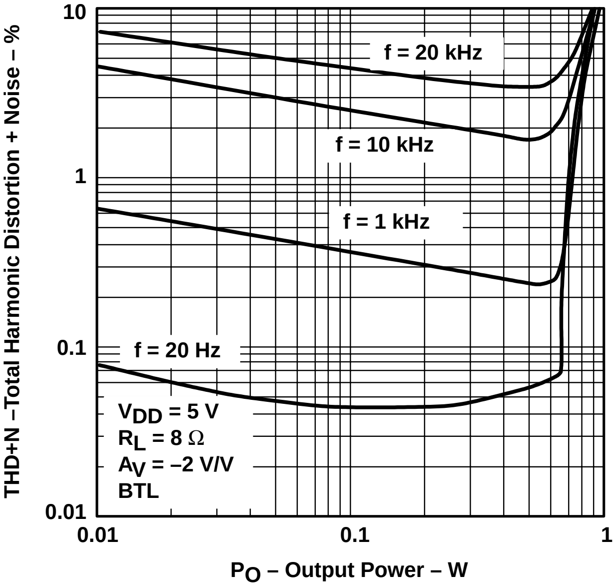


Figure 19

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

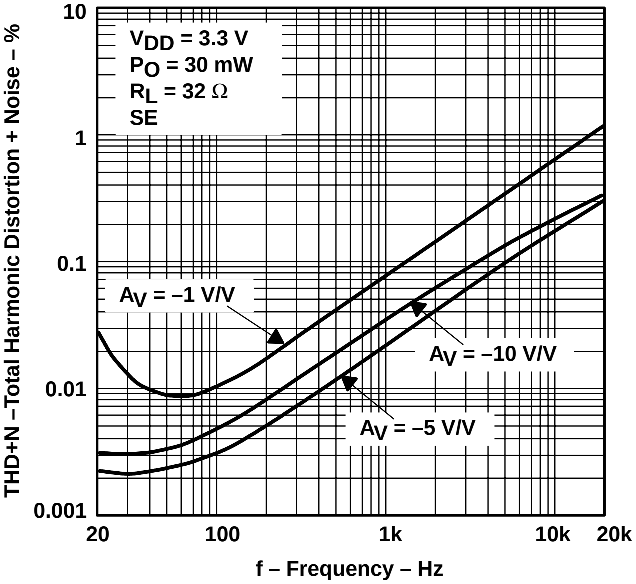


Figure 20

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

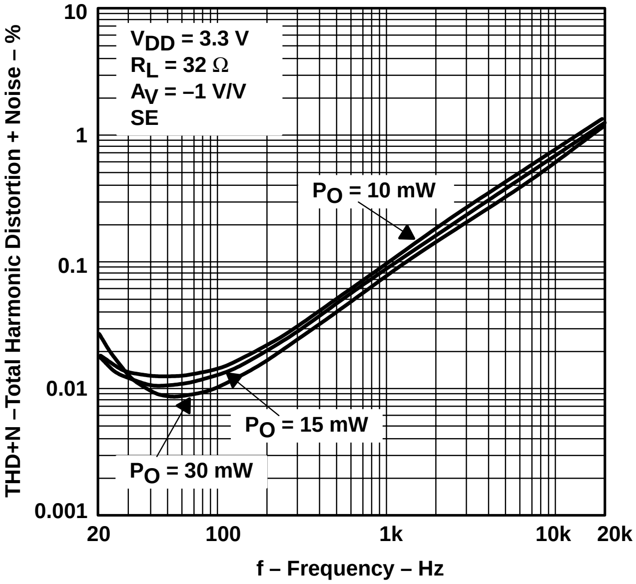


Figure 21

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

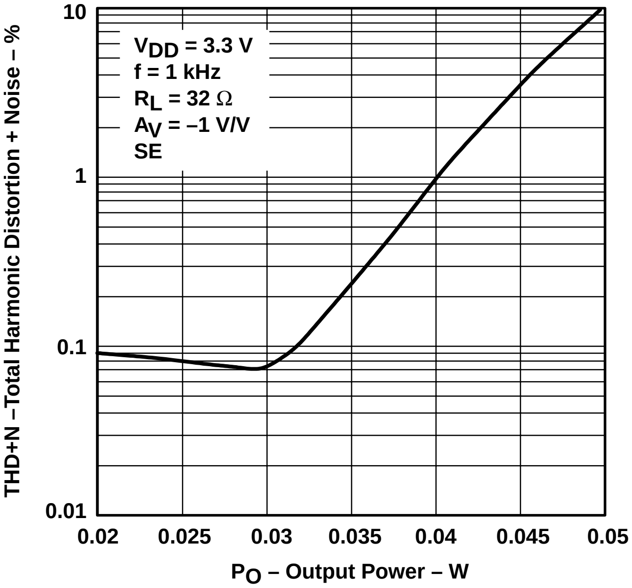


Figure 22

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

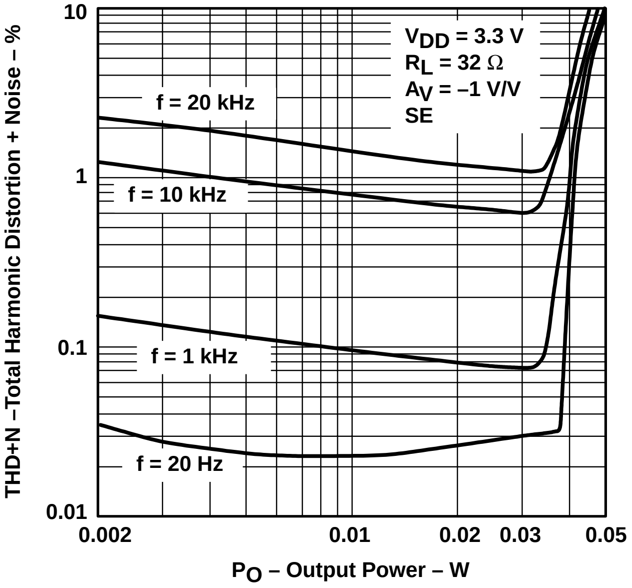


Figure 23

TYPICAL CHARACTERISTICS

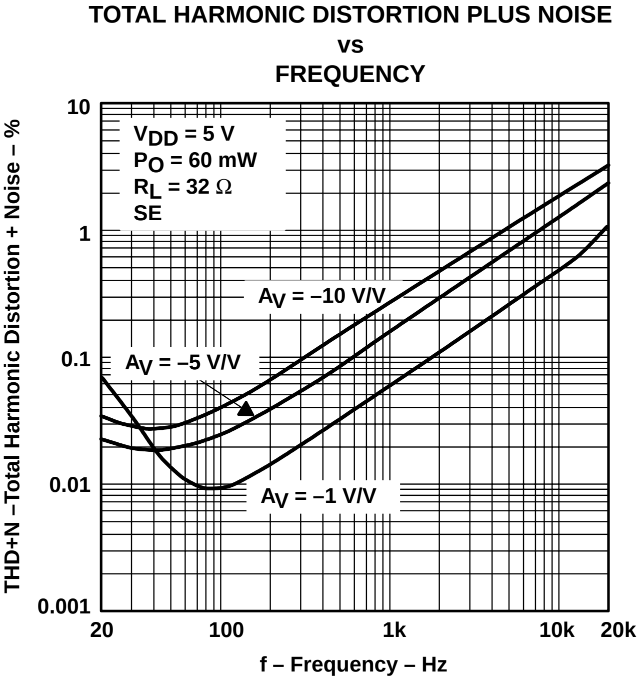


Figure 24

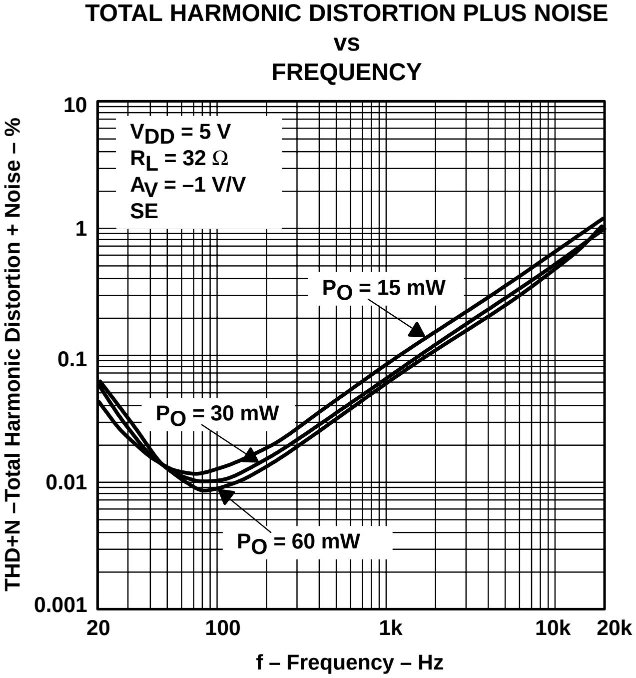


Figure 25

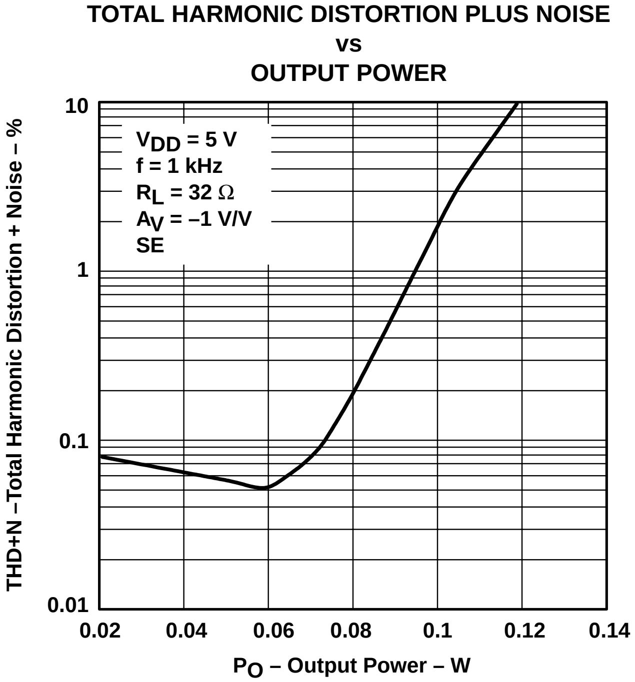


Figure 26

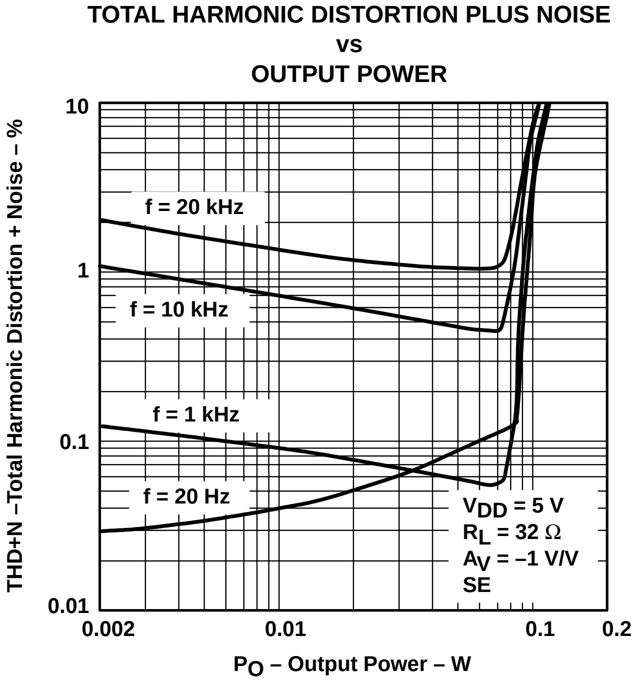


Figure 27

TYPICAL CHARACTERISTICS

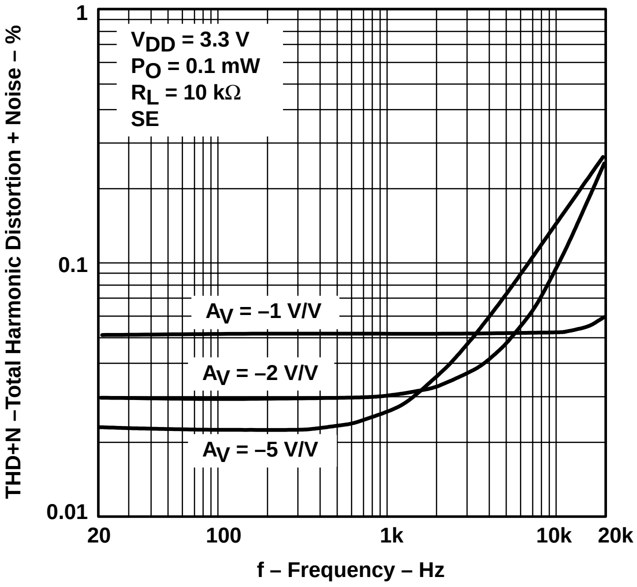

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

Figure 28

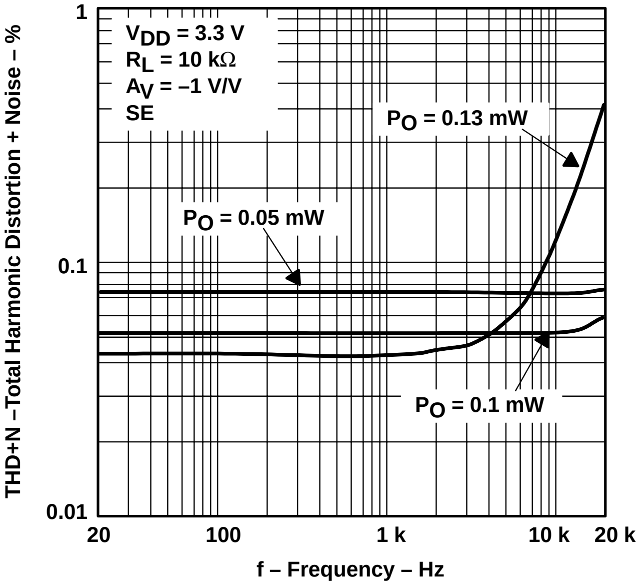

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

Figure 29

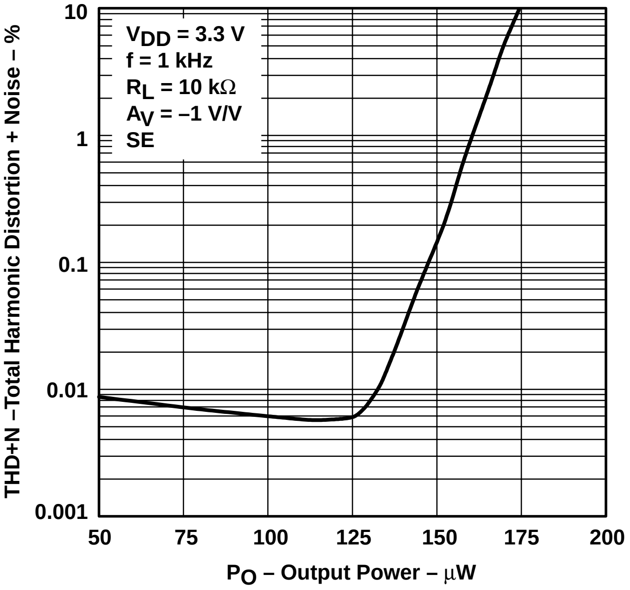

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

Figure 30

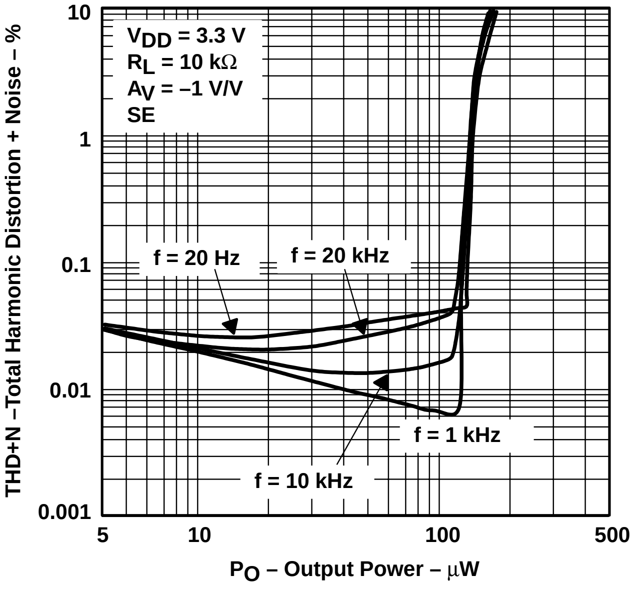

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

Figure 31

TYPICAL CHARACTERISTICS

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

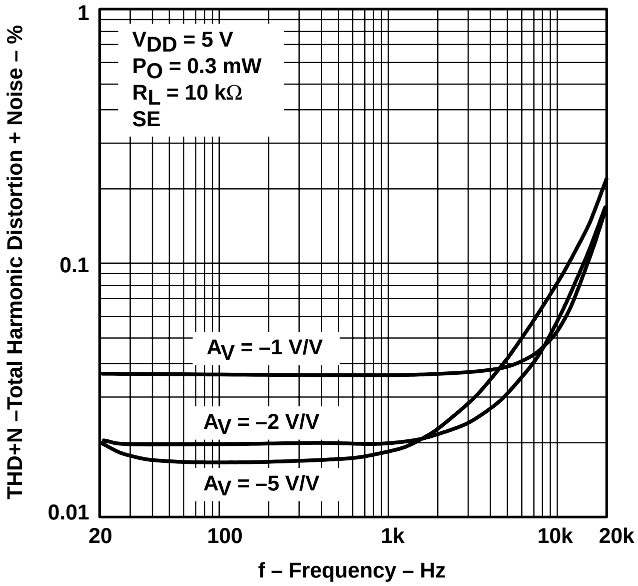


Figure 32

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
FREQUENCY

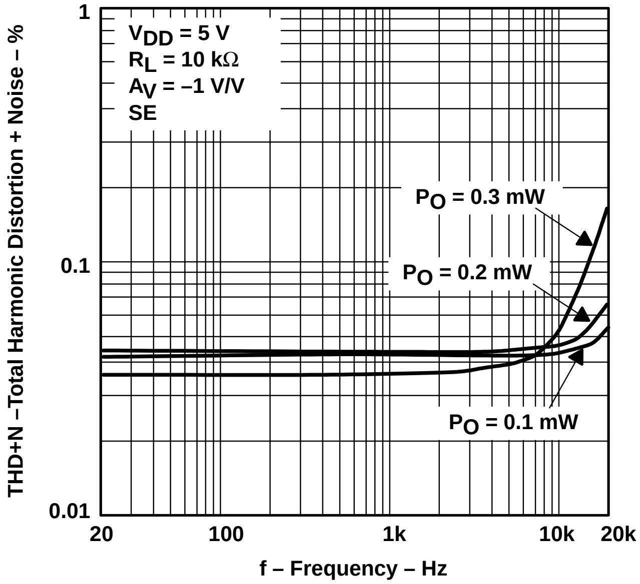


Figure 33

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

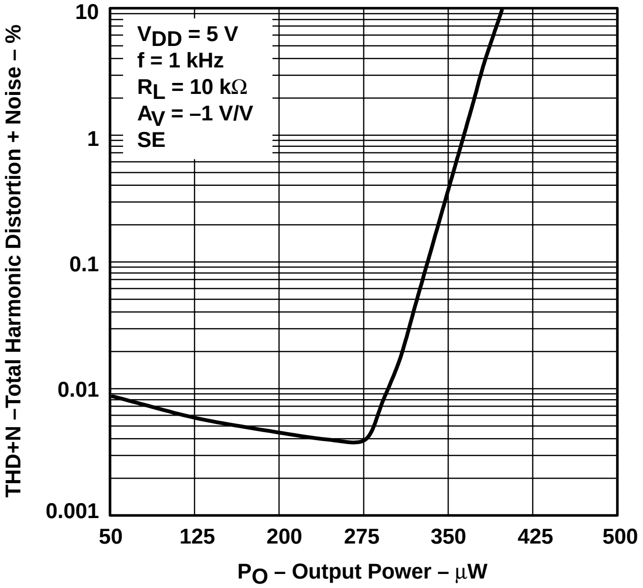


Figure 34

TOTAL HARMONIC DISTORTION PLUS NOISE
vs
OUTPUT POWER

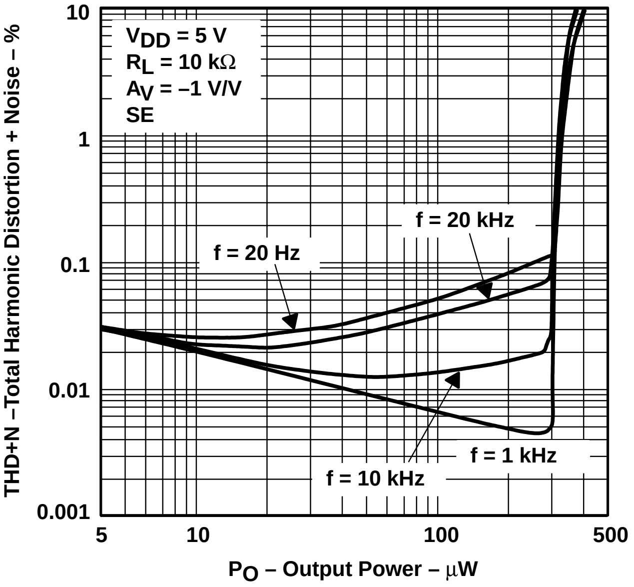


Figure 35

TYPICAL CHARACTERISTICS

OPEN-LOOP GAIN AND PHASE
vs
FREQUENCY

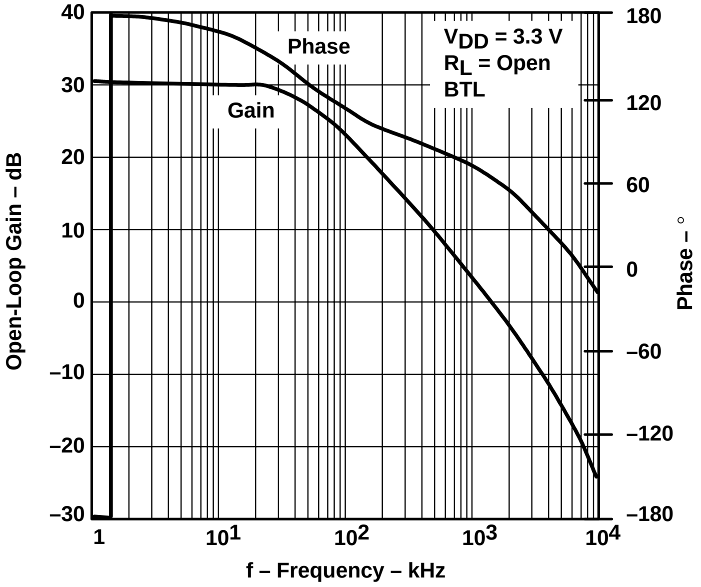


Figure 36

OPEN-LOOP GAIN AND PHASE
vs
FREQUENCY

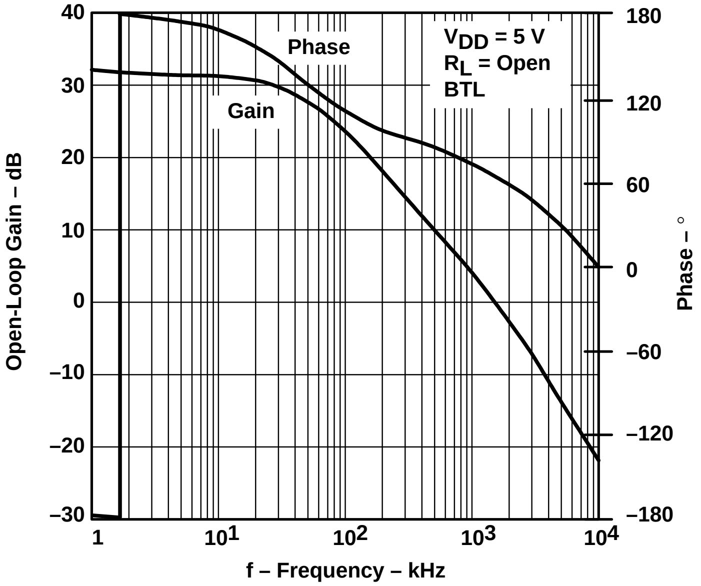


Figure 37

TYPICAL CHARACTERISTICS

CLOSED-LOOP GAIN AND PHASE vs FREQUENCY

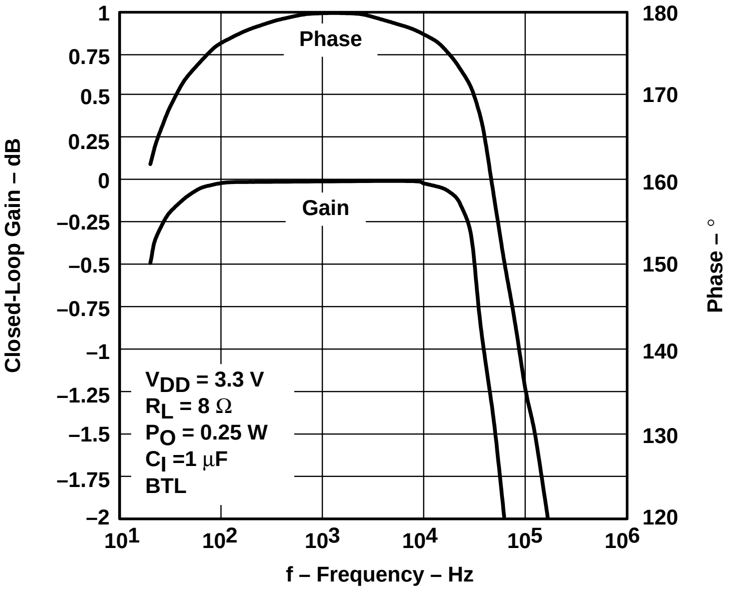


Figure 38

CLOSED-LOOP GAIN AND PHASE vs FREQUENCY

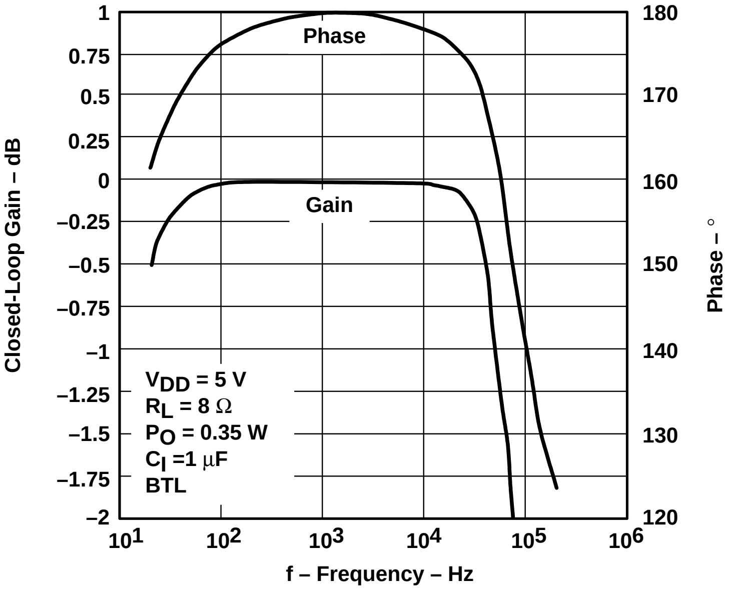


Figure 39

TYPICAL CHARACTERISTICS

CLOSED-LOOP GAIN AND PHASE
vs
FREQUENCY

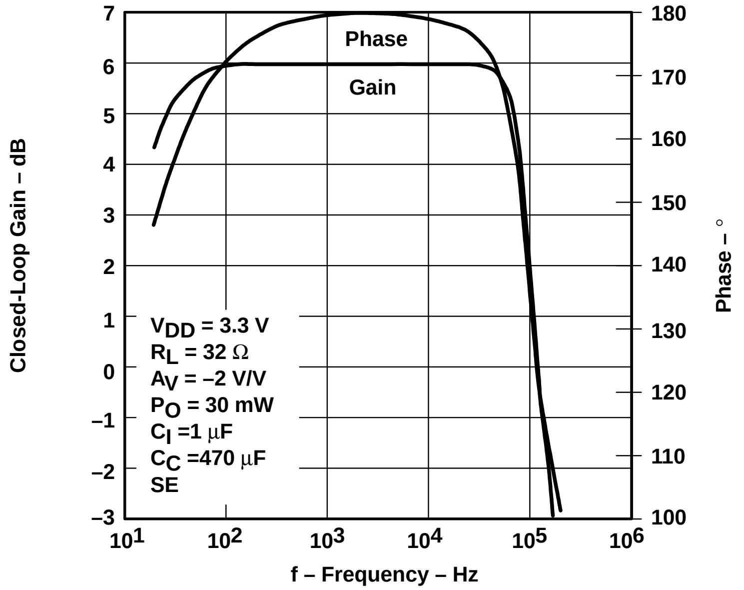


Figure 40

CLOSED-LOOP GAIN AND PHASE
vs
FREQUENCY

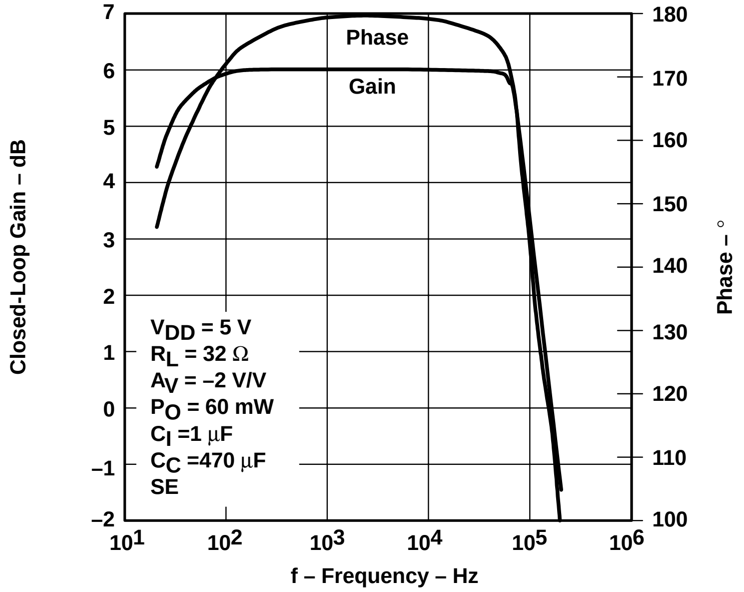


Figure 41

TYPICAL CHARACTERISTICS

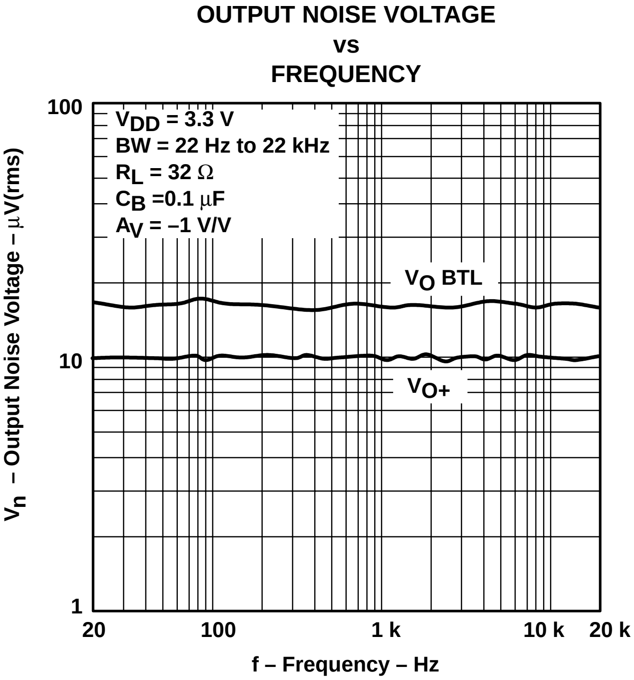


Figure 42

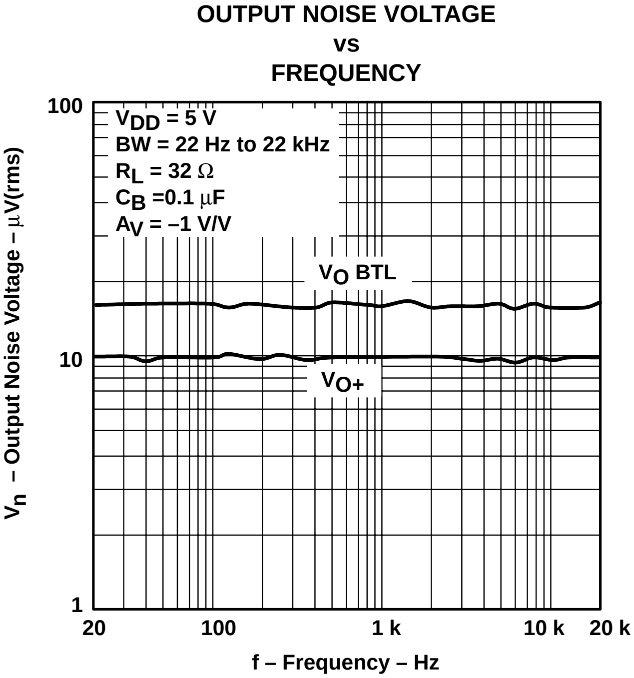


Figure 43

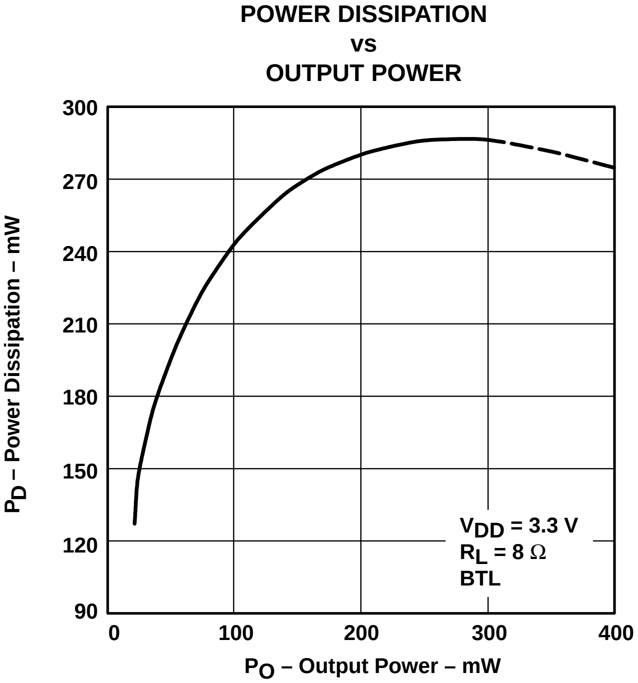


Figure 44

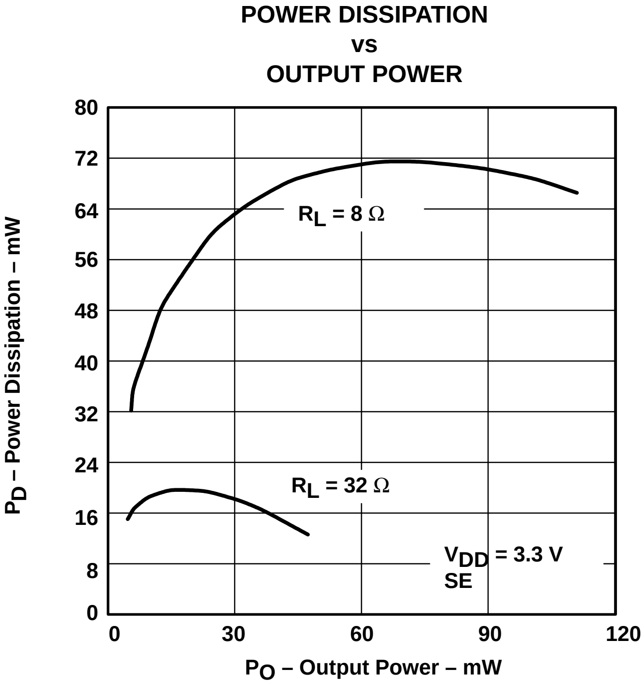


Figure 45

TYPICAL CHARACTERISTICS

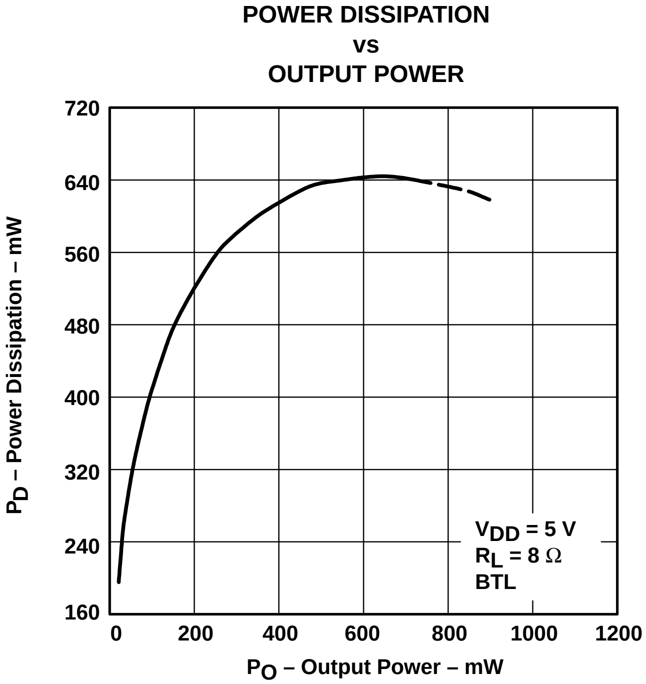


Figure 46

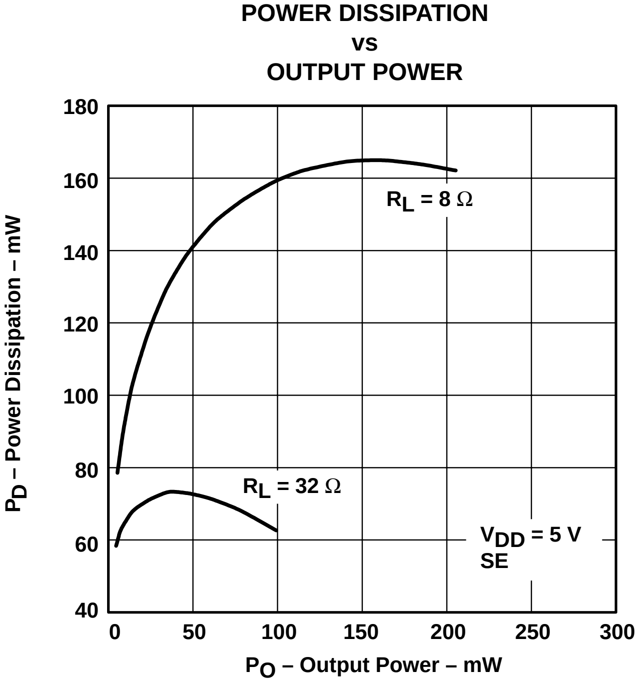


Figure 47

APPLICATION INFORMATION

bridge-tied load versus single-ended mode

Figure 48 shows a linear audio power amplifier (APA) in a BTL configuration. The TPA311 BTL amplifier consists of two linear amplifiers driving both ends of the load. There are several potential benefits to this differential drive configuration but initially consider power to the load. The differential drive to the speaker means that as one side is slewing up, the other side is slewing down, and vice versa. This in effect doubles the voltage swing on the load as compared to a ground referenced load. Plugging 2 × $V_{O(PP)}$ into the power equation, where voltage is squared, yields 4× the output power from the same supply rail and load impedance (see equation 1).

$$V_{(rms)} = \frac{V_{O(PP)}}{2\sqrt{2}}$$

$$\text{Power} = \frac{{V_{(rms)}}^2}{R_L} \tag{1}$$

APPLICATION INFORMATION

bridge-tied load versus single-ended mode (continued)

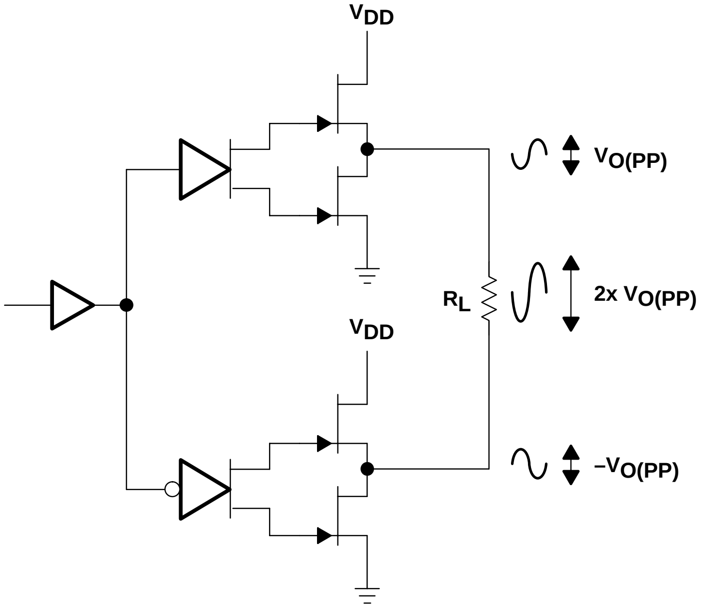


Figure 48. Bridge-Tied Load Configuration

In typical portable handheld equipment, a sound channel operating at 3.3 V and using bridging raises the power into an 8-Ω speaker from a single-ended (SE, ground reference) limit of 62.5 mW to 250 mW. In terms of sound power that is a 6-dB improvement, which is loudness that can be heard. In addition to increased power there are frequency response concerns. Consider the single-supply SE configuration shown in Figure 49. A coupling capacitor is required to block the dc offset voltage from reaching the load. These capacitors can be quite large (approximately 33 µF to 1000 µF), tend to be expensive, heavy, and occupy valuable PCB area. These capacitors also have the additional drawback of limiting low-frequency performance of the system. This frequency limiting effect is due to the high-pass filter network created with the speaker impedance and the coupling capacitance and is calculated with equation 2.

$$f_c = \frac{1}{2\pi R_L C_C} \tag{2}$$

For example, a 68-µF capacitor with an 8-Ω speaker would attenuate low frequencies below 293 Hz. The BTL configuration cancels the dc offsets, which eliminates the need for the blocking capacitors. Low-frequency performance is then limited only by the input network and speaker response. Cost and PCB space are also minimized by eliminating the bulky coupling capacitor.

APPLICATION INFORMATION

bridge-tied load versus single-ended mode (continued)

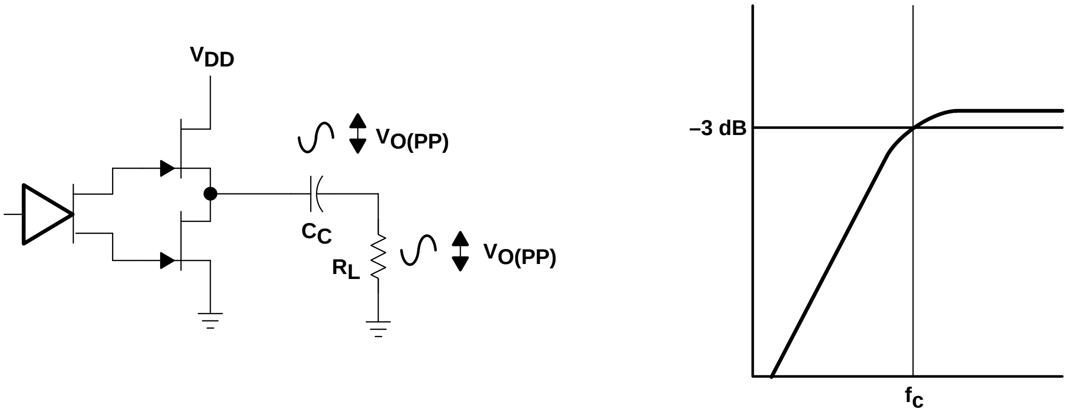


Figure 49. Single-Ended Configuration and Frequency Response

Increasing power to the load does carry a penalty of increased internal power dissipation. The increased dissipation is understandable, considering that the BTL configuration produces 4× the output power of the SE configuration. Internal dissipation versus output power is discussed further in the *thermal considerations* section.

BTL amplifier efficiency

Linear amplifiers are notoriously inefficient. The primary cause of these inefficiencies is voltage drop across the output stage transistors. There are two components of the internal voltage drop. One is the headroom or dc voltage drop that varies inversely to output power. The second component is due to the sinewave nature of the output. The total voltage drop can be calculated by subtracting the RMS value of the output voltage from V_{DD}. The internal voltage drop multiplied by the RMS value of the supply current, I_{DD}rms, determines the internal power dissipation of the amplifier.

An easy-to-use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load. To accurately calculate the RMS values of power in the load and in the amplifier, the current and voltage waveform shapes must first be understood (see Figure 50).

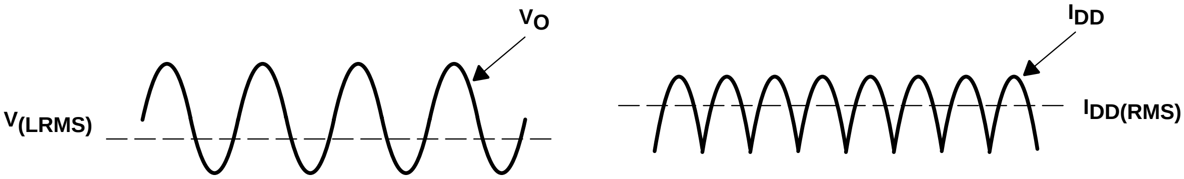


Figure 50. Voltage and Current Waveforms for BTL Amplifiers

APPLICATION INFORMATION

BTL amplifier efficiency (continued)

Although the voltages and currents for SE and BTL are sinusoidal in the load, currents from the supply are very different between SE and BTL configurations. In an SE application the current waveform is a half-wave rectified shape whereas, in BTL it is a full-wave rectified waveform. This means RMS conversion factors are different. Keep in mind that for most of the waveform, both the push and pull transistors are not on at the same time, which supports the fact that each amplifier in the BTL device only draws current from the supply for half the waveform. The following equations are the basis for calculating amplifier efficiency.

$$\text{Efficiency} = \frac{P_L}{P_{SUP}} \qquad (3)$$

where

$$P_L = \frac{V_L\text{rms}^2}{R_L} = \frac{V_p{}^2}{2R_L}$$

$$V_L\text{rms} = \frac{V_P}{\sqrt{2}}$$

$$P_{SUP} = V_{DD}\,I_{DD}\text{rms} = \frac{V_{DD}\,2V_P}{\pi\,R_L}$$

$$I_{DD}\text{rms} = \frac{2V_P}{\pi\,R_L}$$

$$\text{Efficiency of a BTL Configuration} = \frac{\pi\,V_P}{2V_{DD}} = \frac{\pi\left(\frac{P_L R_L}{2}\right)^{1/2}}{2V_{DD}} \qquad (4)$$

Table 1 employs equation 4 to calculate efficiencies for three different output power levels. The efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in a nearly flat internal power dissipation over the normal operating range. The internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design.

Table 1. Efficiency Vs Output Power in 3.3-V 8-Ω BTL Systems

OUTPUT POWER (W)	EFFICIENCY (%)	PEAK-TO-PEAK VOLTAGE (V)	INTERNAL DISSIPATION (W)
0.125	33.6	1.41	0.26
0.25	47.6	2.00	0.29
0.375	58.3	2.45†	0.28

† High-peak voltage values cause the THD to increase.

A final point to remember about linear amplifiers (either SE or BTL) is how to manipulate the terms in the efficiency equation to utmost advantage when possible. In equation 4, V_{DD} is in the denominator. This indicates that as V_{DD} goes down, efficiency goes up.

APPLICATION INFORMATION

application schematic

Figure 51 is a schematic diagram of a typical handheld audio application circuit, configured for a gain of –10 V/V.

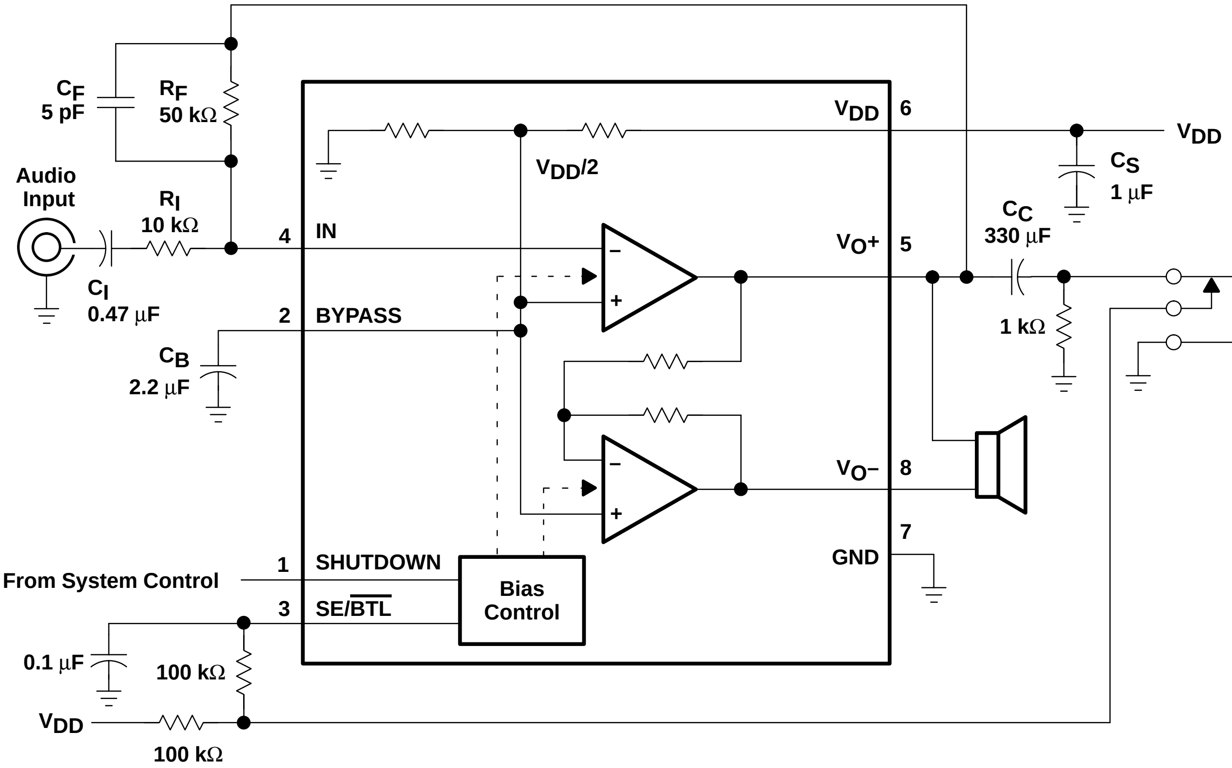


Figure 51. TPA311 Application Circuit

The following sections discuss the selection of the components used in Figure 51.

component selection

gain setting resistors, R_F and R_I

The gain for each audio input of the TPA311 is set by resistors R_F and R_I according to equation 5 for BTL mode.

$$\text{BTL Gain} = A_V = -2\left(\frac{R_F}{R_I}\right) \tag{5}$$

BTL mode operation brings about the factor 2 in the gain equation due to the inverting amplifier mirroring the voltage swing across the load. Given that the TPA311 is a MOS amplifier, the input impedance is very high, consequently input leakage currents are not generally a concern, although noise in the circuit increases as the value of R_F increases. In addition, a certain range of R_F values is required for proper start-up operation of the amplifier. Taken together it is recommended that the effective impedance seen by the inverting node of the amplifier be set between 5 kΩ and 20 kΩ. The effective impedance is calculated in equation 6.

$$\text{Effective Impedance} = \frac{R_F R_I}{R_F + R_I} \tag{6}$$

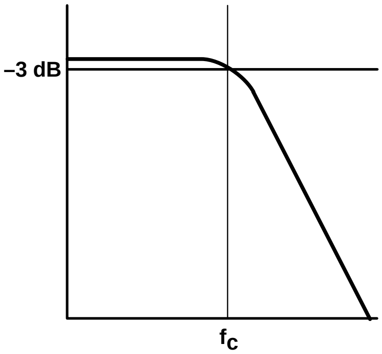
APPLICATION INFORMATION

component selection (continued)

As an example consider an input resistance of 10 kΩ and a feedback resistor of 50 kΩ. The BTL gain of the amplifier would be –10 V/V and the effective impedance at the inverting terminal would be 8.3 kΩ, which is well within the recommended range.

For high performance applications, metal film resistors are recommended because they tend to have lower noise levels than carbon resistors. For values of R_F above 50 kΩ the amplifier tends to become unstable due to a pole formed from R_F and the inherent input capacitance of the MOS input structure. For this reason, a small compensation capacitor, C_F, of approximately 5 pF should be placed in parallel with R_F when R_F is greater than 50 kΩ. This, in effect, creates a low pass filter network with the cutoff frequency defined in equation 7.

$$f_{c(lowpass)} = \frac{1}{2\pi R_F C_F} \tag{7}$$

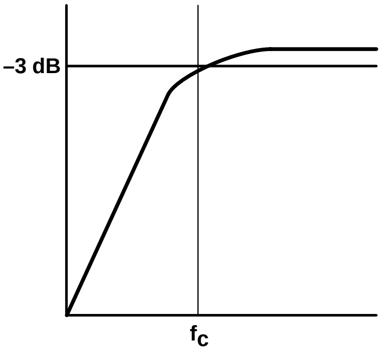


For example, if R_F is 100 kΩ and C_F is 5 pF then f_c is 318 kHz, which is well outside the audio range.

input capacitor, C_I

In the typical application an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and R_I form a high-pass filter with the corner frequency determined in equation 8.

$$f_{c(highpass)} = \frac{1}{2\pi R_I C_I} \tag{8}$$



The value of C_I is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where R_I is 10 kΩ and the specification calls for a flat bass response down to 40 Hz. Equation 8 is reconfigured as equation 9.

$$C_I = \frac{1}{2\pi R_I f_c} \tag{9}$$

APPLICATION INFORMATION

component selection (continued)

In this example, C_I is 0.40 µF, so one would likely choose a value in the range of 0.47 µF to 1 µF. A further consideration for this capacitor is the leakage path from the input source through the input network (R_I, C_I) and the feedback resistor (R_F) to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at $V_{DD}/2$, which is likely higher than the source dc level. It is important to confirm the capacitor polarity in the application.

power supply decoupling, C_S

The TPA311 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 µF placed as close as possible to the device V_{DD} lead, works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 µF or greater placed near the audio power amplifier is recommended.

midrail bypass capacitor, C_B

The midrail bypass capacitor, C_B, is the most critical capacitor and serves several important functions. During start-up or recovery from shutdown mode, C_B determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier, which appears as degraded PSRR and THD + N. The capacitor is fed from a 250-kΩ source inside the amplifier. To keep the start-up pop as low as possible, the relationship shown in equation 10 should be maintained, which insures the input capacitor is fully charged before the bypass capacitor is fuly charged and the amplifier starts up.

$$\frac{10}{\left(C_B \times 250\ \text{k}\Omega\right)} \le \frac{1}{\left(R_F + R_I\right) C_I} \tag{10}$$

As an example, consider a circuit where C_B is 2.2 µF, C_I is 0.47 µF, R_F is 50 kΩ and R_I is 10 kΩ. Inserting these values into the equation 10 we get: $18.2 \le 35.5$ which satisfies the rule. Bypass capacitor, C_B, values of 0.1 µF to 2.2 µF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

single-ended operation

In SE mode (see Figure 51), the load is driven from the primary amplifier output (V_O+, terminal 5).

In SE mode the gain is set by the R_F and R_I resistors and is shown in equation 11. Since the inverting amplifier is not used to mirror the voltage swing on the load, the factor of 2, from equation 5, is not included.

$$\text{SE Gain} = A_V = -\left(\frac{R_F}{R_I}\right) \tag{11}$$

APPLICATION INFORMATION

single-ended operation (continued)

The output coupling capacitor required in single-supply SE mode also places additional constraints on the selection of other components in the amplifier circuit. The rules described earlier still hold with the addition of the following relationship:

$$\frac{10}{\left(C_B \times 250\ k\Omega\right)} \le \frac{1}{\left(R_F + R_I\right) C_I} \ll \frac{1}{R_L C_C} \tag{12}$$

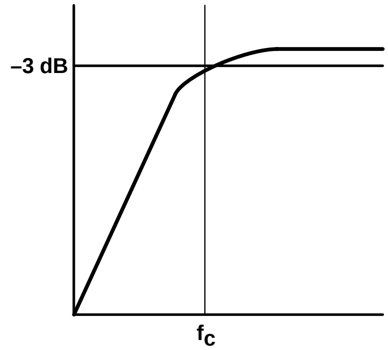
As an example, consider a circuit where C_B is 0.2.2 µF, C_I is 0.47 µF, C_C is 330 µF, R_F is 50 kΩR_L is 32 Ω, and R_I is 10 kΩ. Inserting these values into the equation 12 we get:

$18.2 < 35.5 \ll 94.7$ which satisfies the rule.

output coupling capacitor, C_C

In the typical single-supply SE configuration, an output coupling capacitor (C_C) is required to block the dc bias at the output of the amplifier, thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by equation 13.

$$f_{c(\text{high pass})} = \frac{1}{2\pi R_L C_C} \tag{13}$$



The main disadvantage, from a performance standpoint, is that the typically small load impedances drive the low-frequency corner higher degrading the bass response. Large values of C_C are required to pass low frequencies into the load. Consider the example where a C_C of 330 µF is chosen and loads vary from 8 Ω, 32 Ω, to 47 kΩ. Table 2 summarizes the frequency response characteristics of each configuration.

Table 2. Common Load Impedances vs Low Frequency Output Characteristics in SE Mode

R_L	C_C	LOWEST FREQUENCY
8 Ω	330 µF	60 Hz
32 Ω	330 µF	15 Hz
47,000 Ω	330 µF	0.01 Hz

As Table 2 indicates an 8-Ω load is adequate, earphone response is good, and drive into line level inputs (a home stereo for example) is exceptional.

APPLICATION INFORMATION

SE/$\overline{\text{BTL}}$ operation

The ability of the TPA311 to easily switch between BTL and SE modes is one of its most important cost saving features. This feature eliminates the requirement for an additional earphone amplifier in applications where internal speakers are driven in BTL mode but external earphone or speaker must be accommodated. Internal to the TPA311, two separate amplifiers drive V_O+ and $V_O–$. The SE/$\overline{\text{BTL}}$ input (terminal 3) controls the operation of the follower amplifier that drives $V_O–$ (terminal 8). When SE/$\overline{\text{BTL}}$ is held low, the amplifier is on and the TPA311 is in the BTL mode. When SE/$\overline{\text{BTL}}$ is held high, the $V_O–$ amplifier is in a high output impedance state, which configures the TPA311 as an SE driver from V_O+ (terminal 5). I_{DD} is reduced by approximately one-half in SE mode. Control of the SE/$\overline{\text{BTL}}$ input can be from a logic-level TTL source or, more typically, from a resistor divider network as shown in Figure 52.

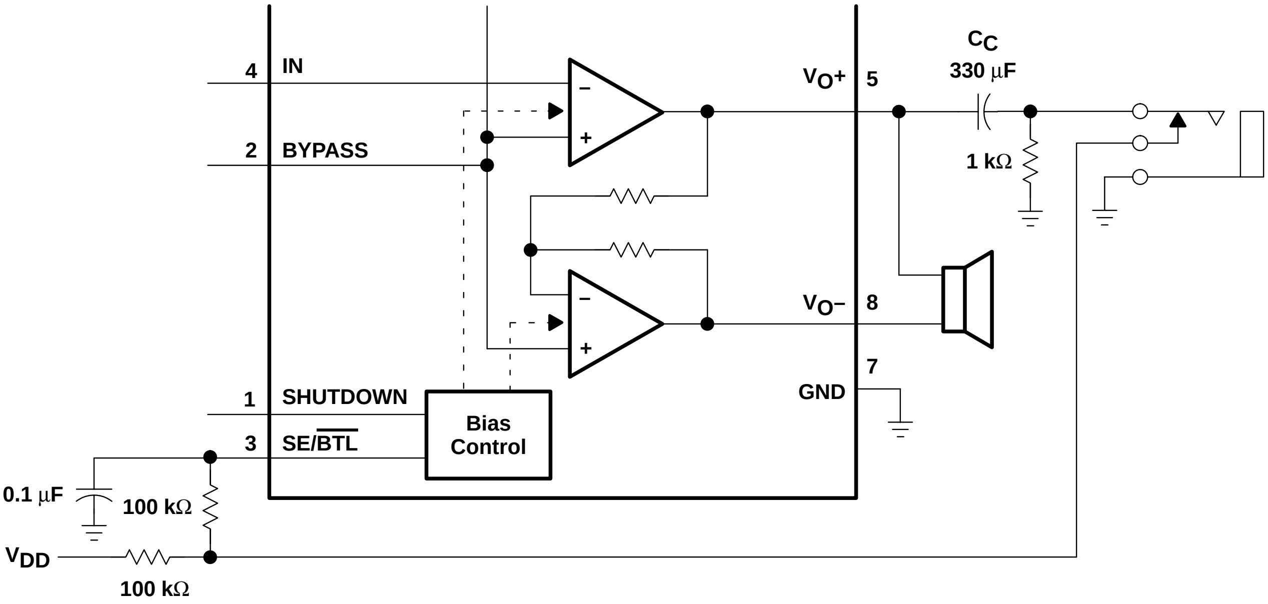


Figure 52. TPA311 Resistor Divider Network Circuit

Using a readily available 1/8-in. (3,5 mm) mono earphone jack, the control switch is closed when no plug is inserted. When closed the 100-kΩ/1-kΩ divider pulls the SE/$\overline{\text{BTL}}$ input low. When a plug is inserted, the 1-kΩ resistor is disconnected and the SE/$\overline{\text{BTL}}$ input is pulled high. When the input goes high, the $V_O–$ amplifier is shutdown causing the BTL speaker to mute (virtually open-circuits the speaker). The V_O+ amplifier then drives through the output capacitor (C_C) into the earphone jack.

using low-ESR capacitors

Low-ESR capacitors are recommended throughout this application. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

APPLICATION INFORMATION

5-V versus 3.3-V operation

The TPA311 operates over a supply range of 2.5 V to 5.5 V. This data sheet provides full specifications for 5-V and 3.3-V operation, as these are considered to be the two most common standard voltages. There are no special considerations for 3.3-V versus 5-V operation with respect to supply bypassing, gain setting, or stability. The most important consideration is that of output power. Each amplifier in TPA311 can produce a maximum voltage swing of V_{DD} – 1 V. This means, for 3.3-V operation, clipping starts to occur when $V_{O(PP)}$ = 2.3 V as opposed to $V_{O(PP)}$ = 4 V at 5 V. The reduced voltage swing subsequently reduces maximum output power into an 8-Ω load before distortion becomes significant.

Operation from 3.3-V supplies, as can be shown from the efficiency formula in equation 4, consumes approximately two-thirds the supply power for a given output-power level of operation from 5-V supplies.

headroom and thermal considerations

Linear power amplifiers dissipate a significant amount of heat in the package under normal operating conditions. A typical music CD requires 12 dB to 15 dB of dynamic headroom to pass the loudest portions without distortion as compared with the average power output. From the TPA311 data sheet, one can see that when the TPA311 is operating from a 5-V supply into a 8-Ω speaker that 350 mW peaks are available. Converting watts to dB:

$$\begin{aligned} P_{dB} &= 10\,\mathrm{Log}\left(\frac{P_W}{P_{ref}}\right) \\ &= 10\,\mathrm{Log}\left(\frac{350\ \mathrm{mW}}{1\ \mathrm{W}}\right) \\ &= -4.6\ \mathrm{dB} \end{aligned}$$

Subtracting the headroom restriction to obtain the average listening level without distortion yields:

$$\begin{aligned} -4.6\ \mathrm{dB} - 15\ \mathrm{dB} &= -\ 19.6\ \mathrm{dB}\ (15\ \mathrm{dB\ headroom}) \\ -4.6\ \mathrm{dB} - 12\ \mathrm{dB} &= -\ 16.6\ \mathrm{dB}\ (12\ \mathrm{dB\ headroom}) \\ -4.6\ \mathrm{dB} - 9\ \mathrm{dB} &= -\ 13.6\ \mathrm{dB}\ (9\ \mathrm{dB\ headroom}) \\ -4.6\ \mathrm{dB} - 6\ \mathrm{dB} &= -\ 10.6\ \mathrm{dB}\ (6\ \mathrm{dB\ headroom}) \\ -4.6\ \mathrm{dB} - 3\ \mathrm{dB} &= -\ 7.6\ \mathrm{dB}\ (3\ \mathrm{dB\ headroom}) \end{aligned}$$

Converting dB back into watts:

$$\begin{aligned} P_W &= 10^{PdB/10} \times P_{ref} \\ &= 11\ \mathrm{mW}\ (15\ \mathrm{dB\ headroom}) \\ &= 22\ \mathrm{mW}\ (12\ \mathrm{dB\ headroom}) \\ &= 44\ \mathrm{mW}\ (9\ \mathrm{dB\ headroom}) \\ &= 88\ \mathrm{mW}\ (6\ \mathrm{dB\ headroom}) \\ &= 175\ \mathrm{mW}\ (3\ \mathrm{dB\ headroom}) \end{aligned}$$

APPLICATION INFORMATION

headroom and thermal considerations (continued)

This is valuable information to consider when attempting to estimate the heat dissipation requirements for the amplifier system. Comparing the absolute worst case, which is 350 mW of continuous power output with 0 dB of headroom, against 12 dB and 15 dB applications drastically affects maximum ambient temperature ratings for the system. Using the power dissipation curves for a 5-V, 8-Ω system, the internal dissipation in the TPA311 and maximum ambient temperatures is shown in Table 3.

Table 3. TPA311 Power Rating, 5-V, 8-Ω, BTL

PEAK OUTPUT POWER (mW)	AVERAGE OUTPUT POWER	POWER DISSIPATION (mW)	MAXIMUM AMBIENT TEMPERATURE	
			0 CFM SOIC	0 CFM DGN
350	350 mW	600	46°C	114°C
350	175 mW (3 dB)	500	64°C	120°C
350	88 mW (6 dB)	380	85°C	125°C
350	44 mW (9 dB)	300	98°C	125°C
350	22 mW (12 dB)	200	115°C	125°C
350	11 mW (15 dB)	180	119°C	125°C

Table 3 shows that the TPA311 can be used to its full 350-mW rating without any heat sinking in still air up to 46°C.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPA311D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		311	Samples
TPA311DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		311	Samples
TPA311DGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		AAB	Samples
TPA311DGNG4	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		AAB	Samples
TPA311DGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		AAB	Samples
TPA311DGNRG4	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		AAB	Samples
TPA311DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		311	Samples
TPA311DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		311	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

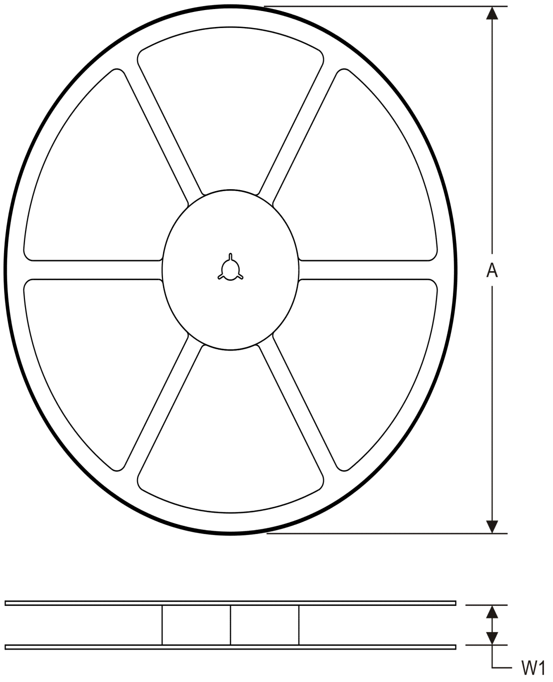
[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

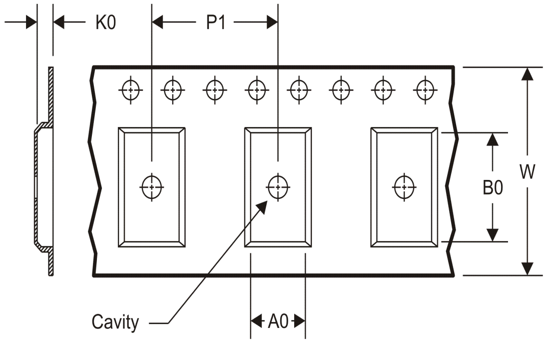
[4] Only one of markings shown within the brackets will appear on the physical device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



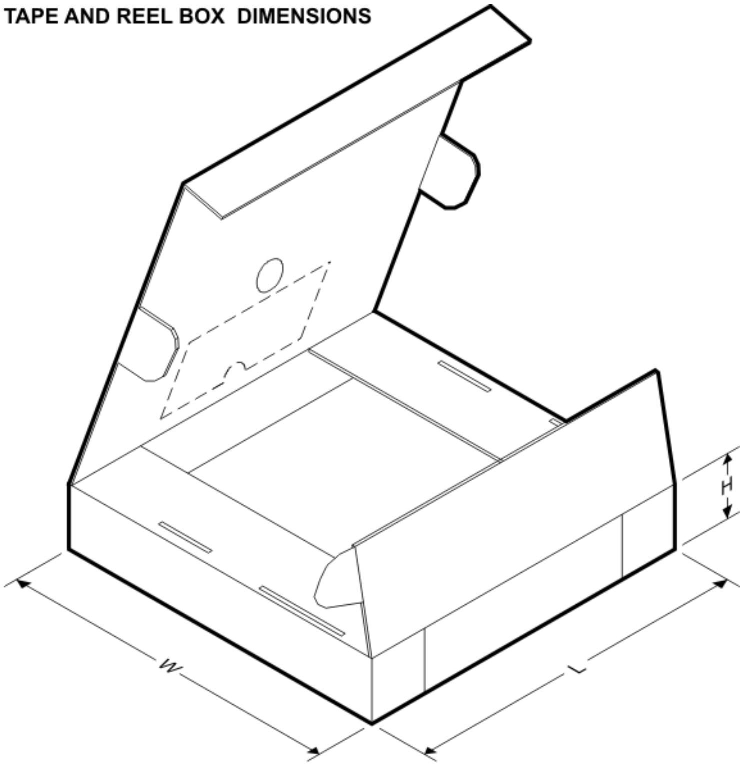
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA311DGNR	MSOP-PowerPAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPA311DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

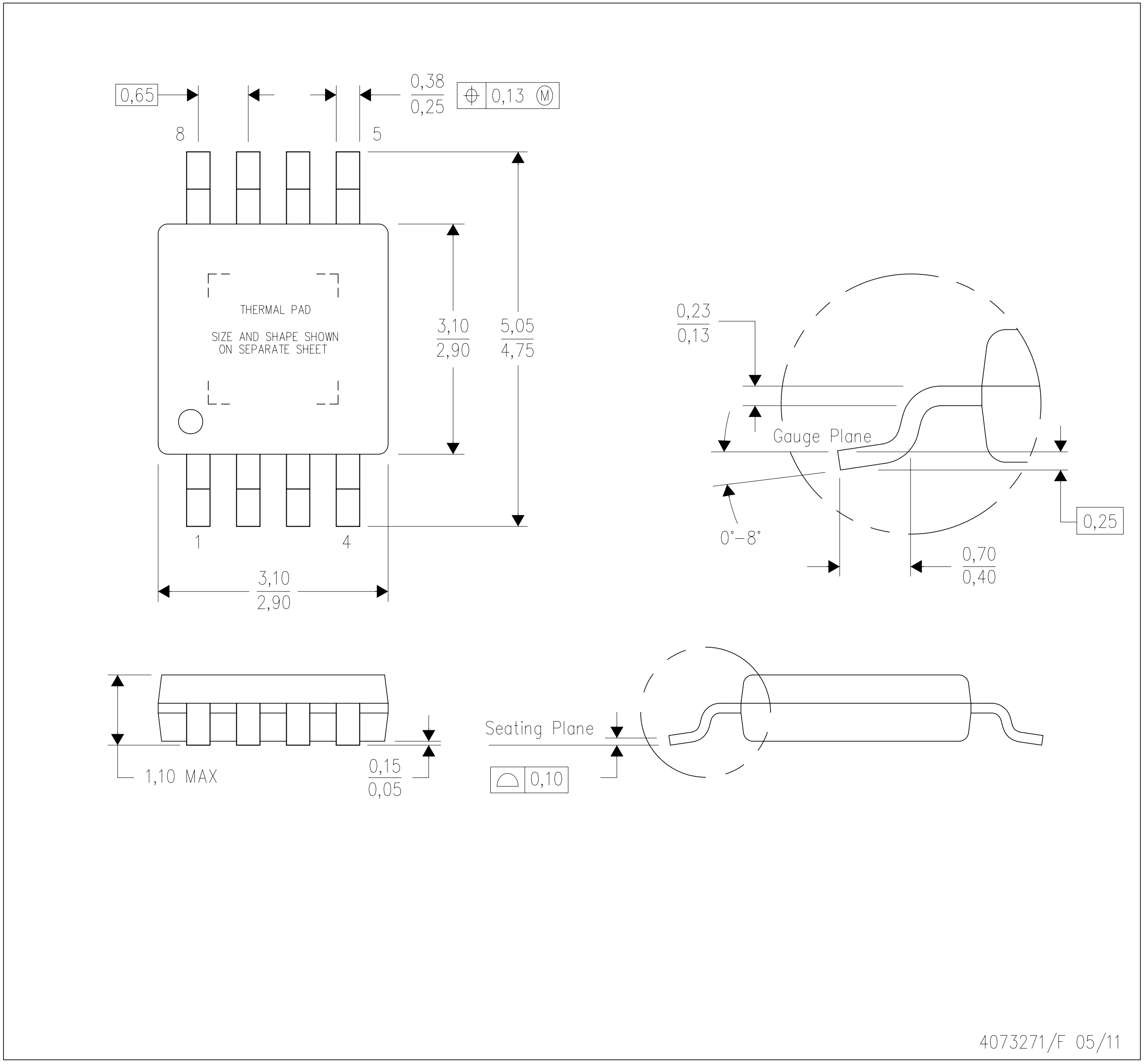
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA311DGNR	MSOP-PowerPAD	DGN	8	2500	358.0	335.0	35.0
TPA311DR	SOIC	D	8	2500	367.0	367.0	35.0

DGN (S-PDSO-G8) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MO-187 variation AA-T

PowerPAD is a trademark of Texas Instruments.

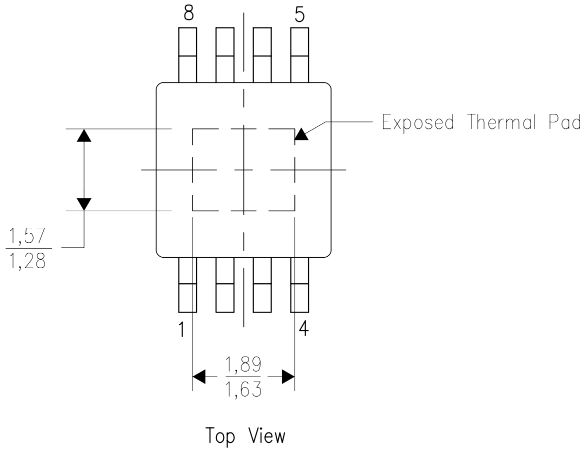
DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

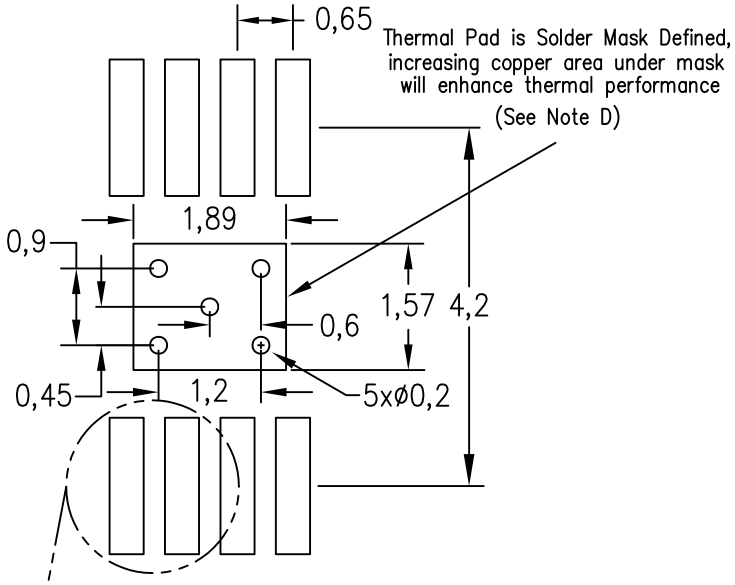
4206323–2/I 12/11

NOTE: All linear dimensions are in millimeters

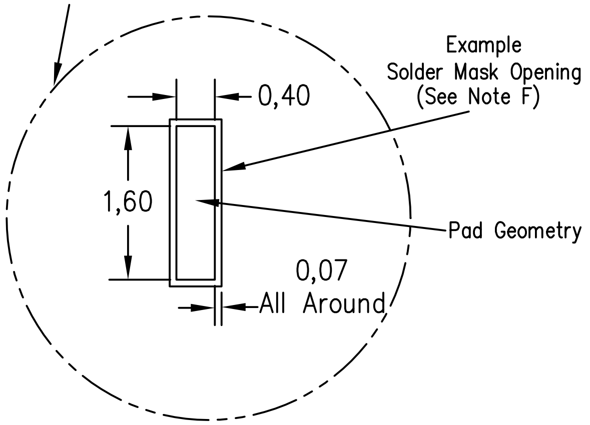
PowerPAD is a trademark of Texas Instruments

DGN (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

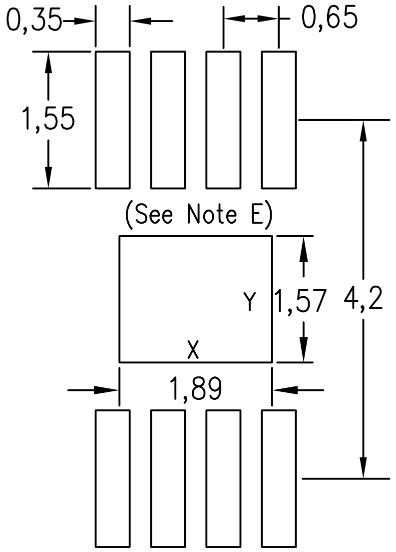
Example Board Layout
Via pattern and copper pad size
may vary depending on layout constraints



Example
Non Soldermask Defined Pad



Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).
Reference table below for other
solder stencil thicknesses

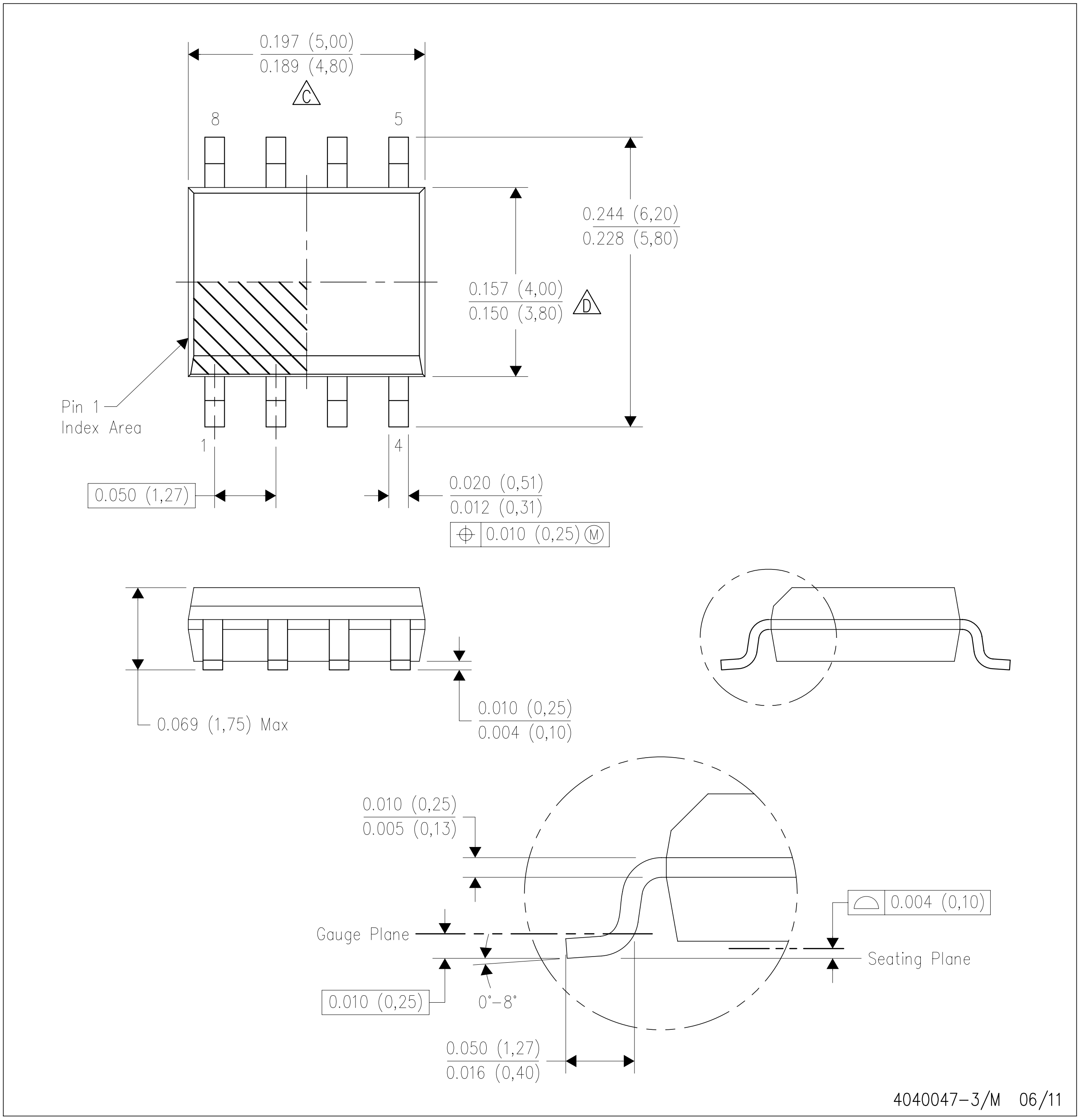


Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.0	1.7
0.127mm	1.89	1.57
0.152mm	1.75	1.45
0.178mm	1.65	1.35

4207737–2/F 02/13

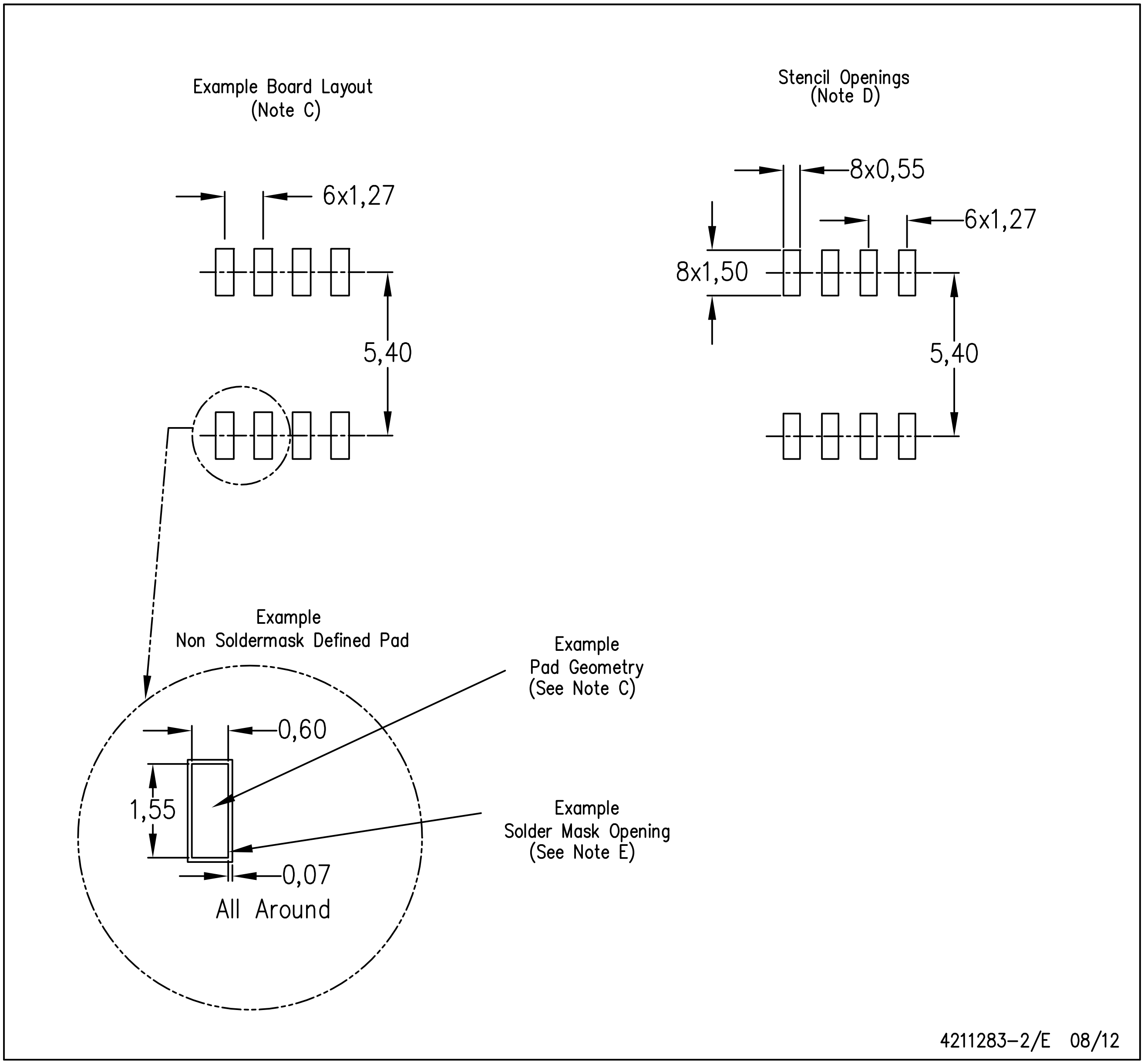
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
- F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265