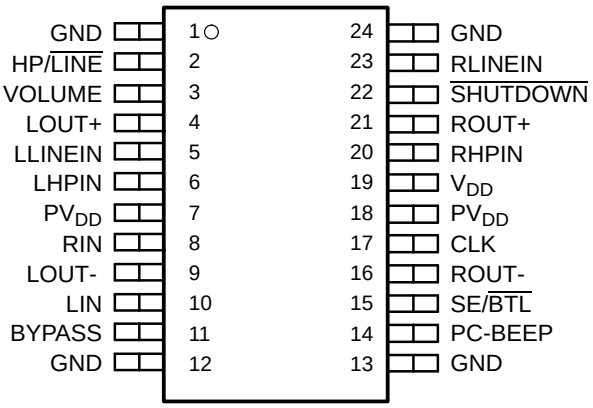
STEREO 2.8-W AUDIO POWER AMPLIFIER WITH DC VOLUME CONTROL AND MUX CONTROL

FEATURES

- **Compatible With PC 99 Desktop Line-Out Into 10-kΩ Load**
- **Compatible With PC 99 Portable Into 8-Ω Load**
- **Internal Gain Control, Which Eliminates External Gain-Setting Resistors**
- **DC Volume Control From 20 dB to -40 dB**
- **2.8-W/Ch Output Power Into a 3-Ω Load**
- **Input MUX Select Terminal**
- **PC-Beep Input**
- **Depop Circuitry**
- **Stereo Input MUX**
- **Fully Differential Input**
- **Low Supply Current and Shutdown Current**
- **Surface-Mount Power Packaging 24-Pin TSSOP PowerPAD™**

PWP PACKAGE
(TOP VIEW)



DESCRIPTION

The TPA0232 is a stereo audio power amplifier in a 24-pin TSSOP thermally enhanced package capable of delivering 2.8 W of continuous RMS power per channel into 3-Ω loads.

This device minimizes the number of external components needed, which simplifies the design and frees up board space for other features. When driving 1 W into 8-Ω speakers, the TPA0232 has less than 0.4% THD+N across its specified frequency range. Included within this device is integrated depop circuitry that virtually eliminates transients that cause noise in the speakers.

Amplifier gain is controlled by means of a dc voltage input on the VOLUME terminal. There are 31 discrete steps covering the range of 20 dB (maximum volume setting) to -40 dB (minimum volume setting) in 2-dB steps. When the VOLUME terminal exceeds 3.54 V, the device is muted. An internal input MUX allows two sets of stereo inputs to the amplifier. The HP/$\overline{\text{LINE}}$ terminal allows the user to select which MUX input is active regardless of whether the amplifier is in single-ended (SE) or bridge-tied load (BTL) mode. In notebook applications, where internal speakers are driven as BTL and the line outputs (often headphone drive) are required to be SE, the TPA0232 automatically switches into SE mode when the SE/$\overline{\text{BTL}}$ input is activated, and this effectively reduces the gain by 6 dB.

The TPA0232 consumes only 10 mA of supply current during normal operation. A miserly shutdown mode reduces the supply current to 150 µA.

The PowerPAD package (PWP) delivers a level of thermal performance that was previously achievable only in TO-220-type packages. Thermal impedances of approximately 35°C/W are readily realized in multilayer PCB applications. This allows the TPA0232 to operate at full power into 8-Ω loads at ambient temperatures of 85°C.

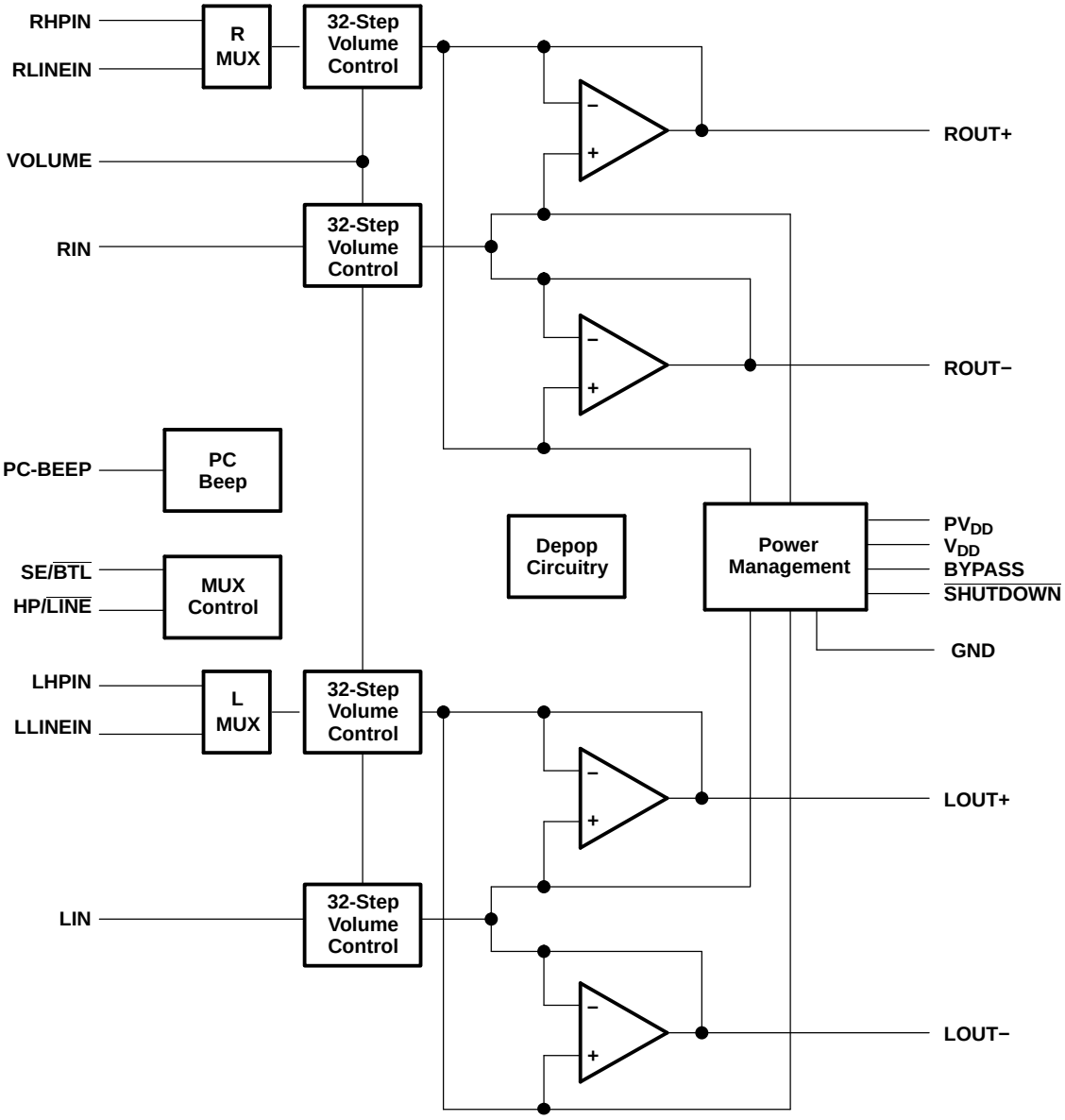
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	PACKAGED DEVICE
	TSSOP(1) (PWP)
-40°C to 85°C	TPA0232PWP

(1) The PWP package is available taped and reeled. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA0232PWPR).

FUNCTIONAL BLOCK DIAGRAM



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BYPASS	11		Tap to voltage divider for internal mid-supply bias generator
CLK	17	I	If a 47-nF capacitor is attached, the TPA0232 generates an internal clock. An external clock can override the internal clock input to this terminal.
GND	1, 12 13, 24	I	Ground connection for circuitry. Connected to thermal pad
LHPIN	6	I	Left channel headphone input, selected when SE/$\overline{\text{BTL}}$ is held high
LIN	10	I	Common left input for fully differential input. AC ground for single-ended inputs
LLINEIN	5	I	Left channel line negative input, selected when SE/$\overline{\text{BTL}}$ is held low
LOUT+	4	O	Left channel positive output in $\overline{\text{BTL}}$ mode and positive output in SE mode
LOUT-	9	O	Left channel negative output in $\overline{\text{BTL}}$ mode and high-impedance in SE mode
HP/$\overline{\text{LINE}}$	2	I	HP/$\overline{\text{LINE}}$ is the input MUX control input. When the HP/$\overline{\text{LINE}}$ terminal is held high, the headphone inputs (LHPIN or RHPIN [6, 20]) are active. When the HP/$\overline{\text{LINE}}$ terminal is held low, the line BTL inputs (LLINEIN or RLINEIN [5, 23]) are active.
PC-BEEP	14	I	The input for PC-Beep mode. PC-BEEP is enabled when a > 1.5-V (peak-to-peak) square wave is input to PC-BEEP.
PV_{DD}	7, 18	I	Power supply for output stage
RHPIN	20	I	Right channel headphone input, selected when SE/$\overline{\text{BTL}}$ is held high
RIN	8	I	Common right input for fully differential input. AC ground for single-ended inputs
RLINEIN	23	I	Right channel line input, selected when SE/$\overline{\text{BTL}}$ is held low
ROUT+	21	O	Right channel positive output in $\overline{\text{BTL}}$ mode and positive output in SE mode
ROUT-	16	O	Right channel negative output in $\overline{\text{BTL}}$ mode and high-impedance in SE mode
SE/$\overline{\text{BTL}}$	15	I	Hold SE/$\overline{\text{BTL}}$ low for BTL mode and hold high for SE mode
$\overline{\text{SHUTDOWN}}$	22	I	When held low, this terminal places the entire device, except PC-BEEP detect circuitry, in shutdown mode.
V_{DD}	19	I	Analog V_{DD} input supply. This terminal needs to be isolated from PV_{DD} to achieve highest performance.
VOLUME	3	I	VOLUME detects the dc level at the terminal and sets the gain for 31 discrete steps covering a range of 20 dB to -40 dB for dc levels of 0.15 V to 3.54 V. When the dc level is over 3.54 V, the device is muted.
Thermal Pad			Connect to ground. Must be soldered down in all applications to properly secure device on PC board.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

	UNIT
Supply voltage, V_{DD}	6 V
Input voltage, V_I	-0.3 V to V_{DD} 0.3 V
Continuous total power dissipation	Internally Limited (see Dissipation Rating Table)
Operating free-air temperature range, T_A	-40°C to 85°C
Operating junction temperature range, T_J	-40°C to 150°C
Storage temperature range, T_{stg}	-65°C to 85°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
PWP	2.7 W(1)	21.8 mW/°C	1.7 W	1.4 W

(1) See the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report* (literature number SLMA002), for more information on the PowerPAD package. The thermal data was measured on a PCB layout based on the information in the section entitled *Texas Instruments Recommended Board for PowerPAD* on page 33 of the before mentioned document.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
Supply voltage, V_{DD}		4.5	5.5	V
High-level input voltage, V_{IH}	SE/$\overline{\text{BTL}}$, HP/$\overline{\text{LINE}}$	$0.8 \times V_{DD}$		V
	$\overline{\text{SHUTDOWN}}$	2		
Low-level input voltage, V_{IL}	SE/$\overline{\text{BTL}}$, HP/$\overline{\text{LINE}}$		$0.6 \times V_{DD}$	V
	$\overline{\text{SHUTDOWN}}$		0.8	
Operating free-air temperature, T_A		-40	85	°C

ELECTRICAL CHARACTERISTICS

at specified free-air temperature, V_{DD} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\lvert V_{OO} \rvert$	Output offset voltage (measured differentially)	V_I = 0 V, A_V = 2 V/V			35	mV
PSRR	Power supply rejection ratio	V_{DD} = 4.9 V to 5.1 V		67		dB
$\lvert I_{IH} \rvert$	High-level input current ($\overline{\text{SHUTDOWN}}$, SE/$\overline{\text{BTL}}$, HP/$\overline{\text{LINE}}$, VOLUME)	V_{DD} = 5.5 V, $V_I = V_{DD}$			900	nA
$\lvert I_{IL} \rvert$	Low-level input current ($\overline{\text{SHUTDOWN}}$, SE/$\overline{\text{BTL}}$, HP/$\overline{\text{LINE}}$, VOLUME)	V_{DD} = 5.5 V, V_I = 0 V			900	nA
I_{DD}	Supply current	BTL mode, $\overline{\text{SHUTDOWN}}$ = 2 V, SE/$\overline{\text{BTL}}$ = HP/$\overline{\text{LINE}}$ = 0.6 V_{DD}		10	15	mA
		SE mode, $\overline{\text{SHUTDOWN}}$ = 2 V, SE/$\overline{\text{BTL}}$ = HP/$\overline{\text{LINE}}$ = 0.8 V_{DD}		5	7.5	
$I_{DD(SD)}$	Supply current, shutdown mode	$\overline{\text{SHUTDOWN}}$ = 0 V, SE/$\overline{\text{BTL}}$ = HP/$\overline{\text{LINE}}$ = 0 V_{DD}		150	300	µA

OPERATING CHARACTERISTICS

V_{DD} = 5 V, T_A = 25°C, R_L = 4Ω , Gain = 2 V/V, BTL mode (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_O	Output power	R_L = 3 Ω, f = 1 kHz	THD = 10%		2.8		W
			THD = 1%		2.3		
THD+N	Total harmonic distortion plus noise	P_O = 1 W, f = 20 Hz to 15 kHz			0.4%		
B_{OM}	Maximum output power bandwidth	THD = 5%			>15		kHz
	Supply ripple rejection ratio	f = 1 kHz, $C_{(BYP)}$ = 0.47 µF	BTL mode		65		dB
			SE mode		60		
V_n	Noise output voltage	$C_{(BYP)}$ = 0.47 µF, f = 20 Hz to 20 kHz	BTL mode		34		μV_{RMS}
			SE mode		44		

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
THD+N	Total harmonic distortion plus noise	vs Output power	1, 4, 6, 8, 10
		vs Voltage gain	2
		vs Frequency	3, 5, 7, 9, 11
		vs Output voltage	12
V_n	Output noise voltage	vs Frequency	13
	Supply ripple rejection ratio	vs Frequency	14, 15
	Crosstalk	vs Frequency	16, 17, 18
	Shutdown attenuation	vs Frequency	19
SNR	Signal-to-noise ratio	vs Frequency	20
	Closed loop response		21, 22
P_O	Output power	vs Load resistance	23, 24
P_D	Power dissipation	vs Output power	25, 26
		vs Ambient temperature	27
Z_I	Input impedance	vs Gain	28

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

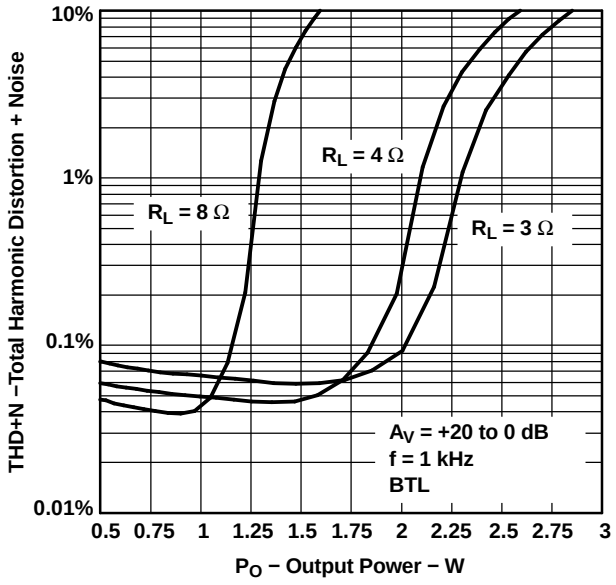


Figure 1.

TOTAL HARMONIC DISTORTION PLUS NOISE vs VOLTAGE GAIN

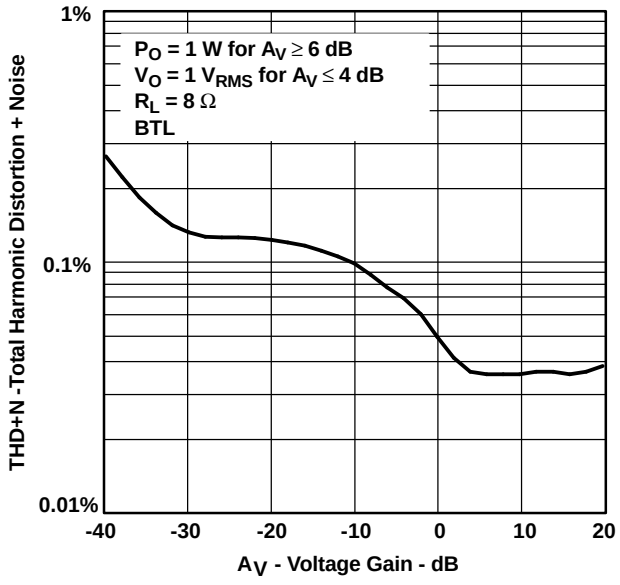


Figure 2.

TEXAS INSTRUMENTS
www.ti.com

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

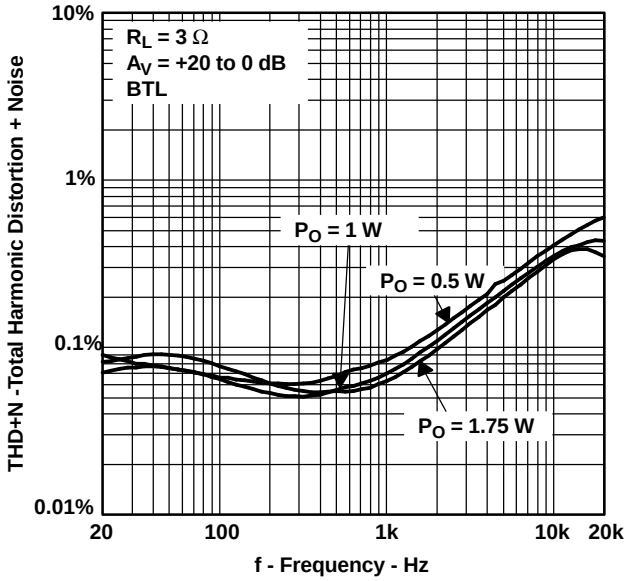


Figure 3.

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

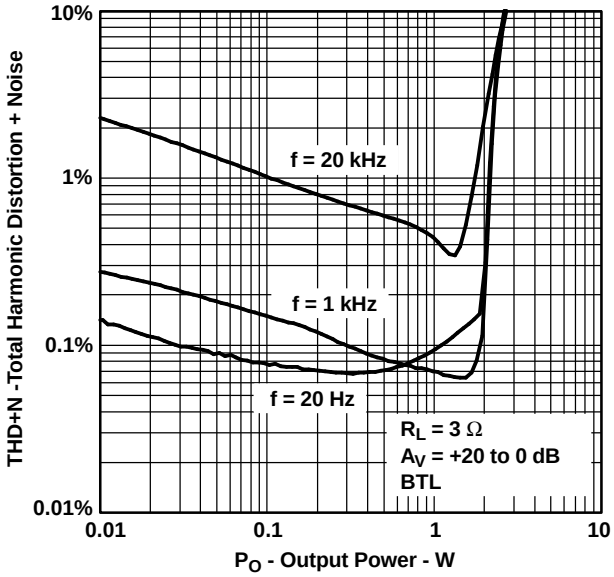


Figure 4.

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

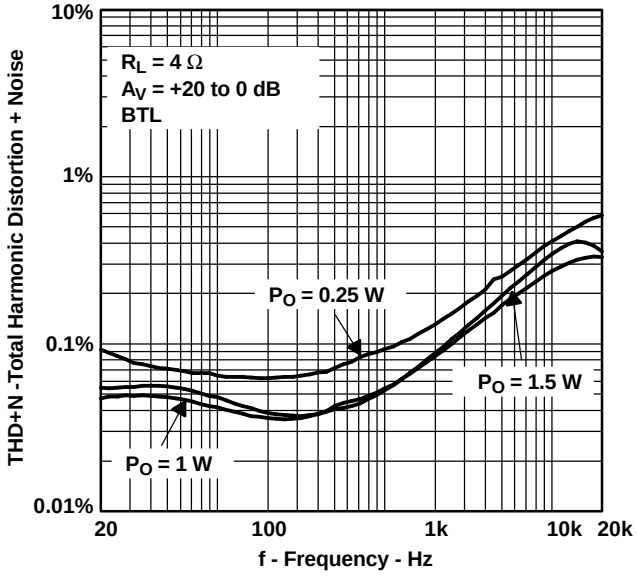


Figure 5.

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER

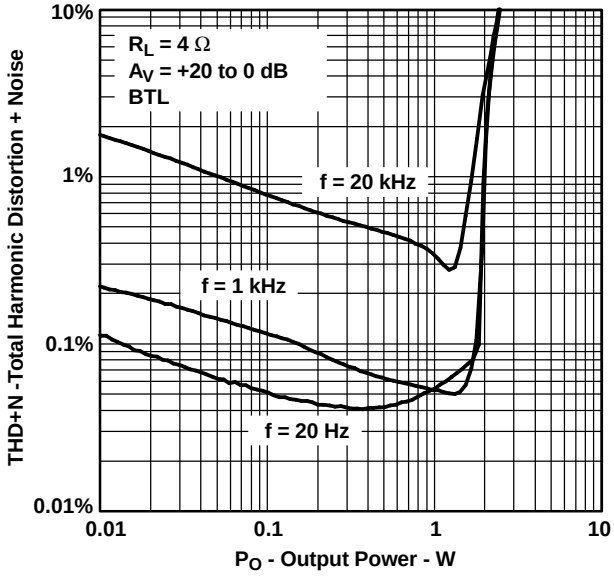


Figure 6.

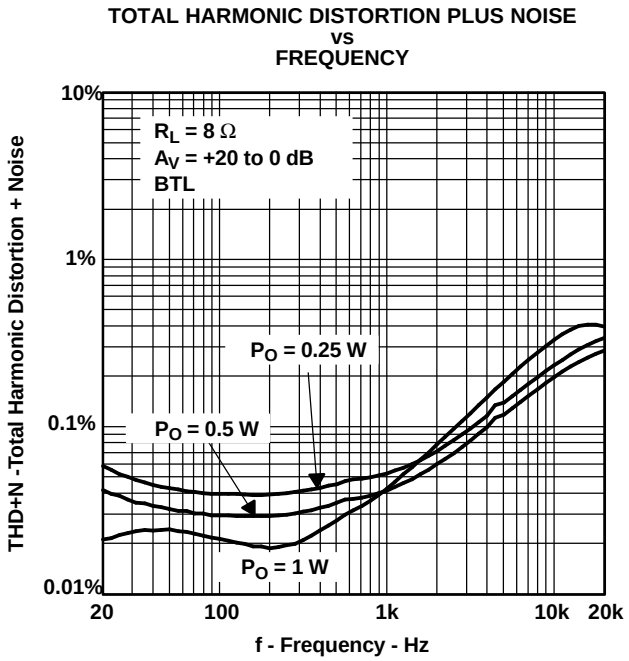


Figure 7.

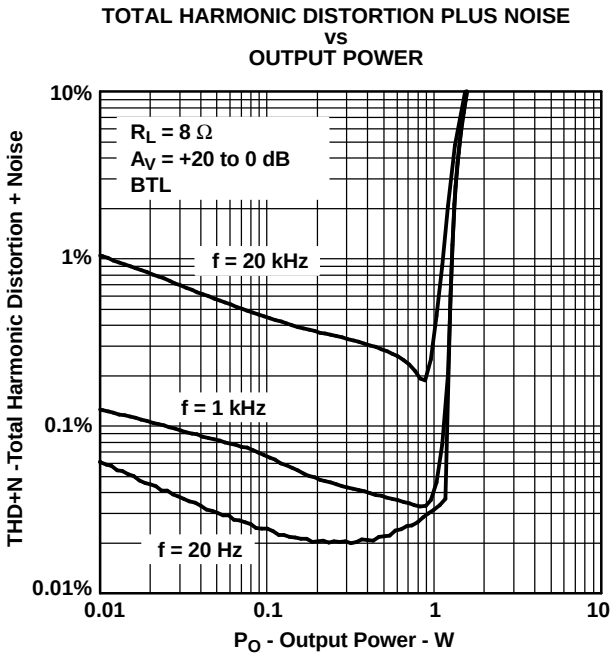


Figure 8.

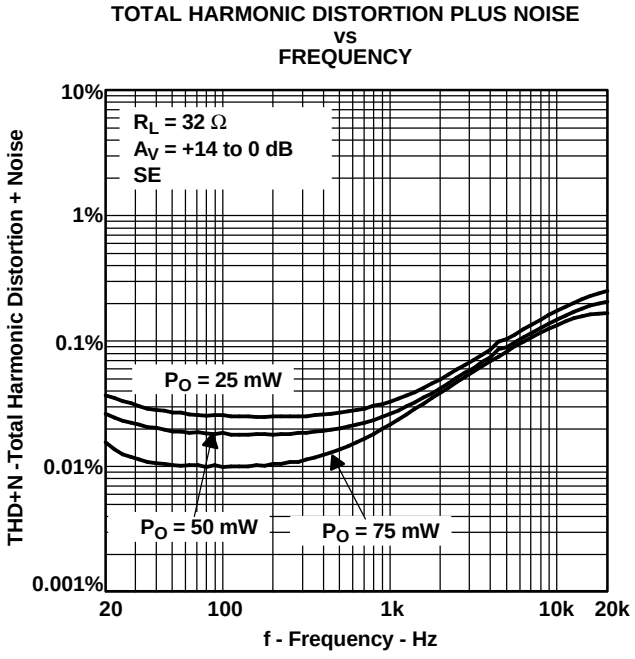


Figure 9.

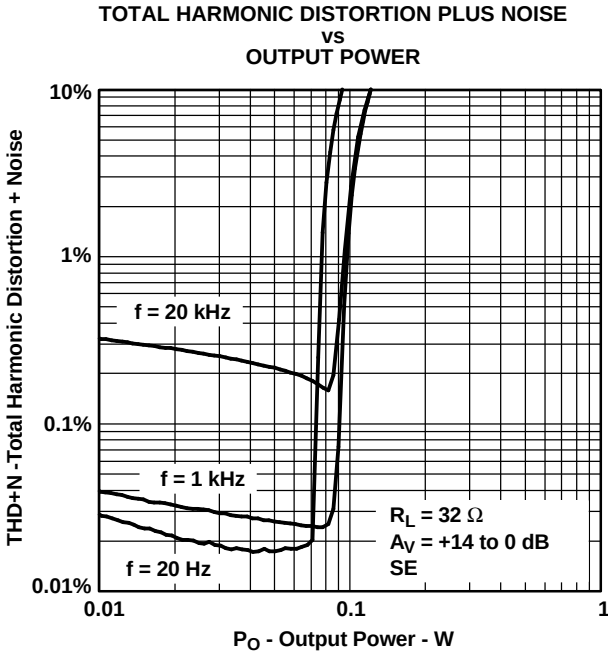


Figure 10.

TEXAS INSTRUMENTS
www.ti.com

TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

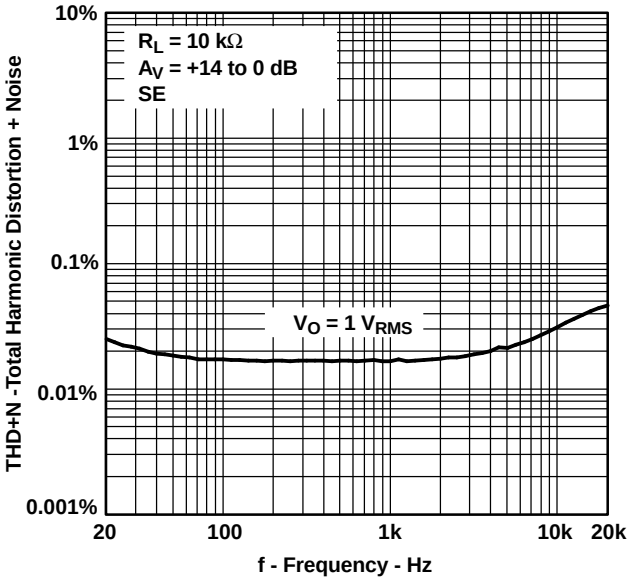


Figure 11.

TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT VOLTAGE

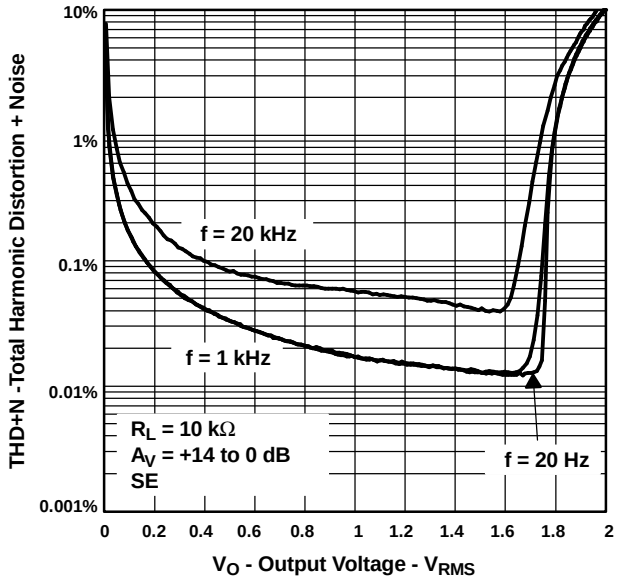


Figure 12.

OUTPUT NOISE VOLTAGE vs FREQUENCY

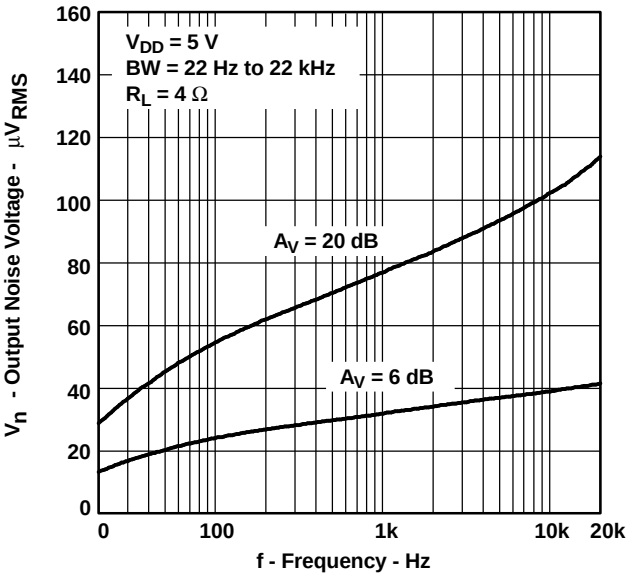


Figure 13.

SUPPLY RIPPLE REJECTION RATIO vs FREQUENCY

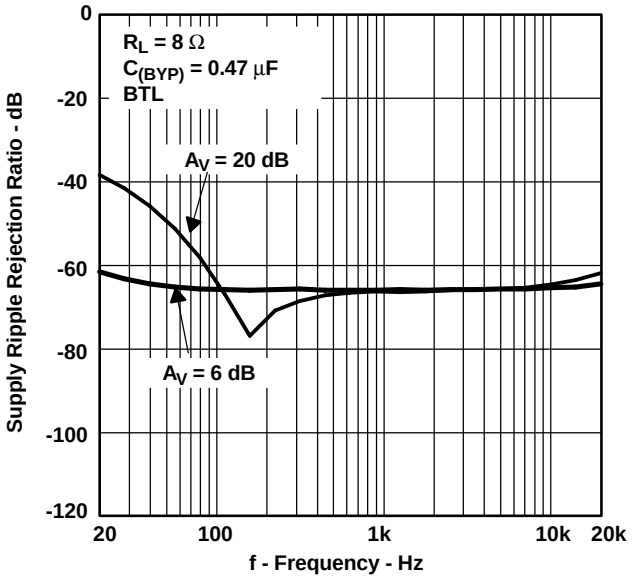


Figure 14.

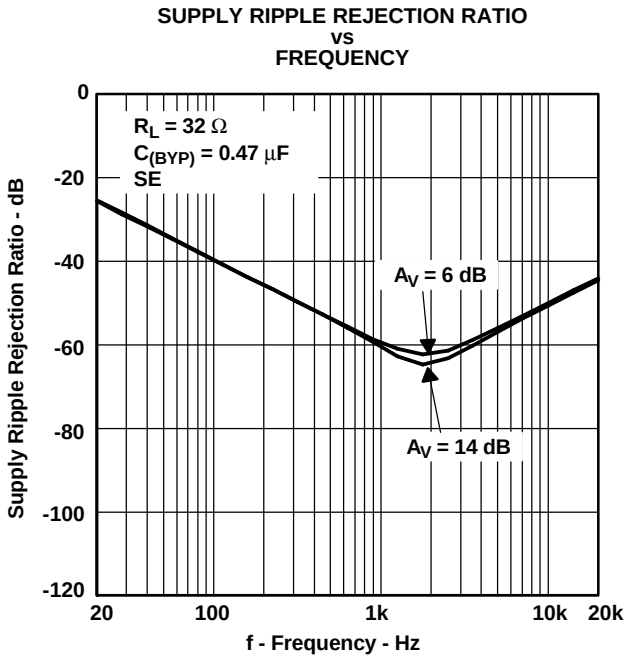


Figure 15.

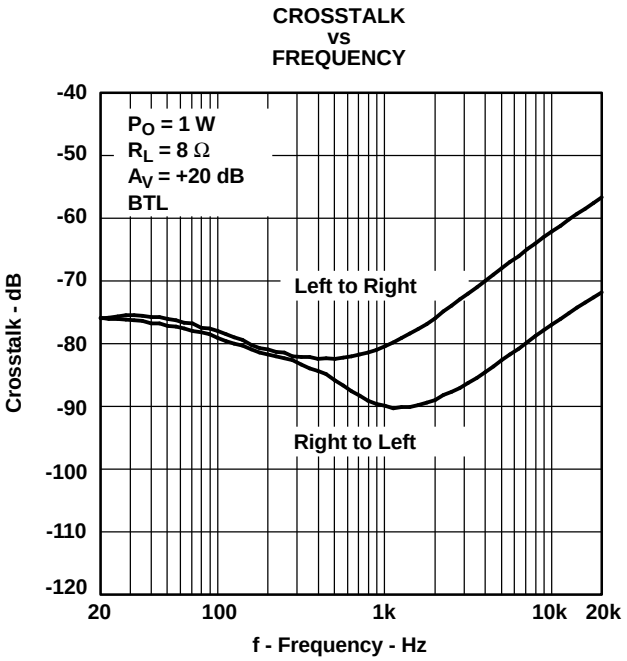


Figure 16.

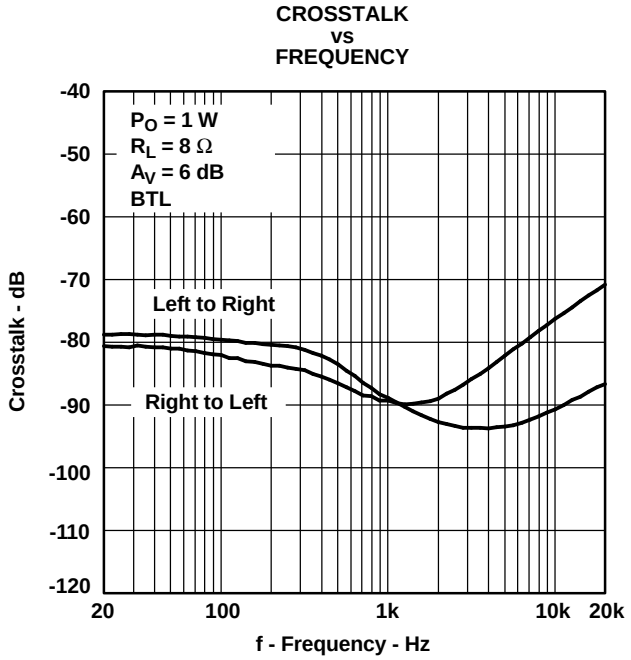


Figure 17.

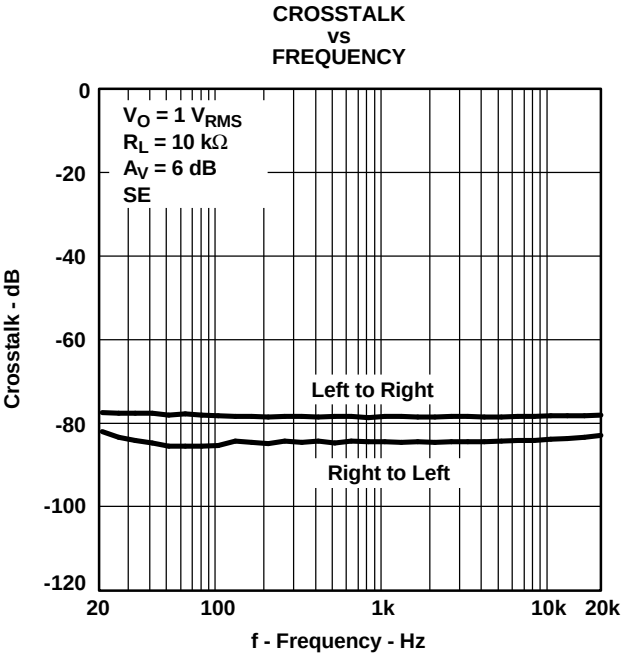


Figure 18.

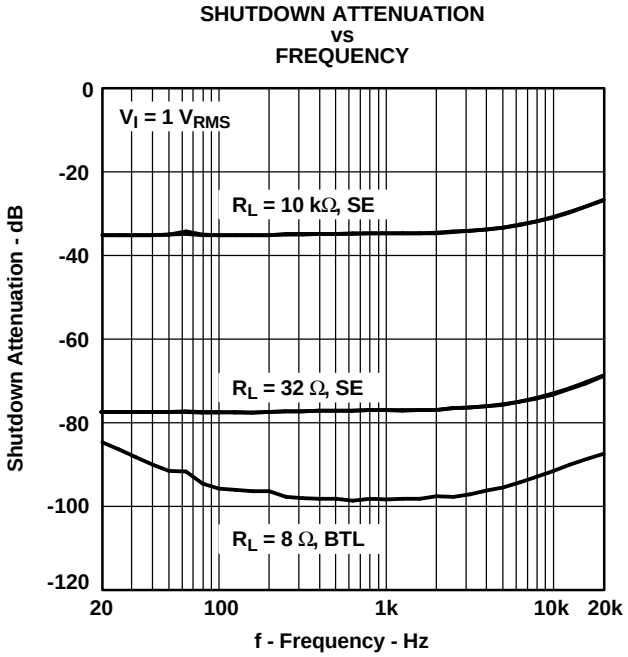


Figure 19.

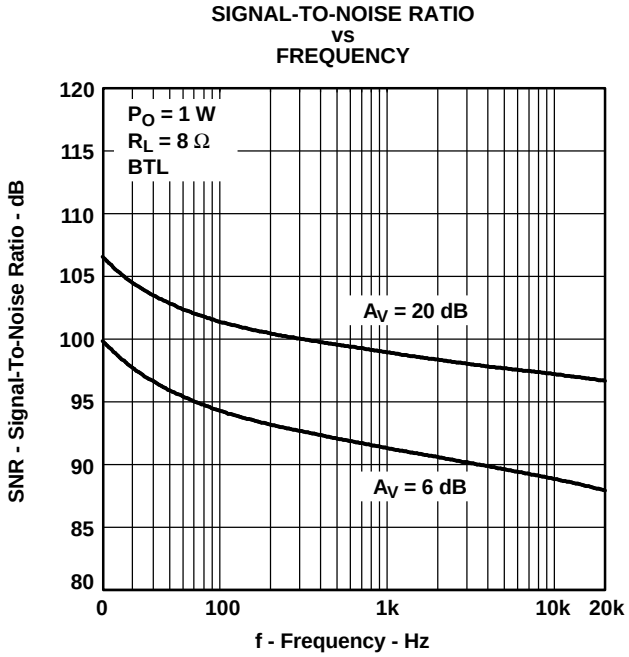


Figure 20.

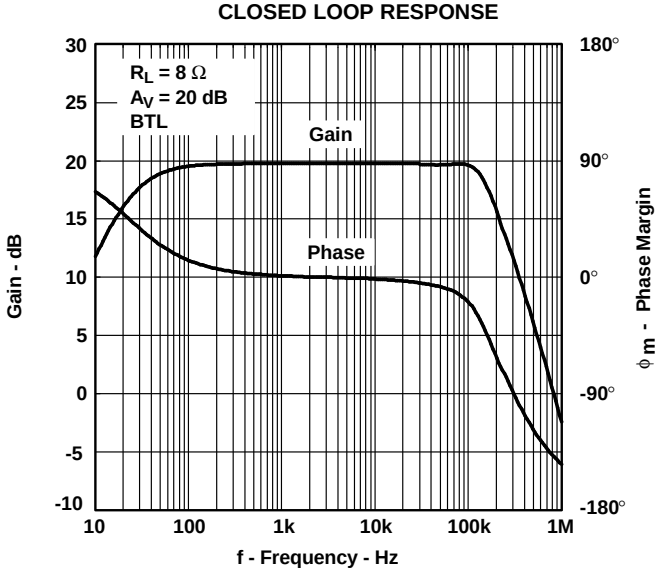


Figure 21.

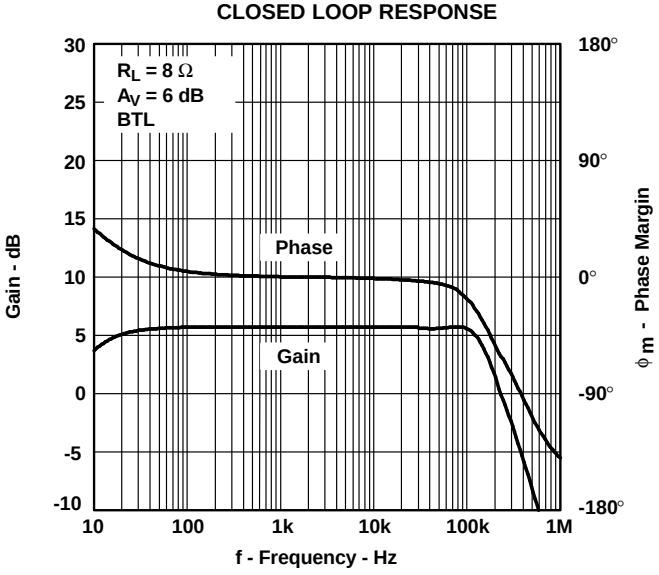


Figure 22.

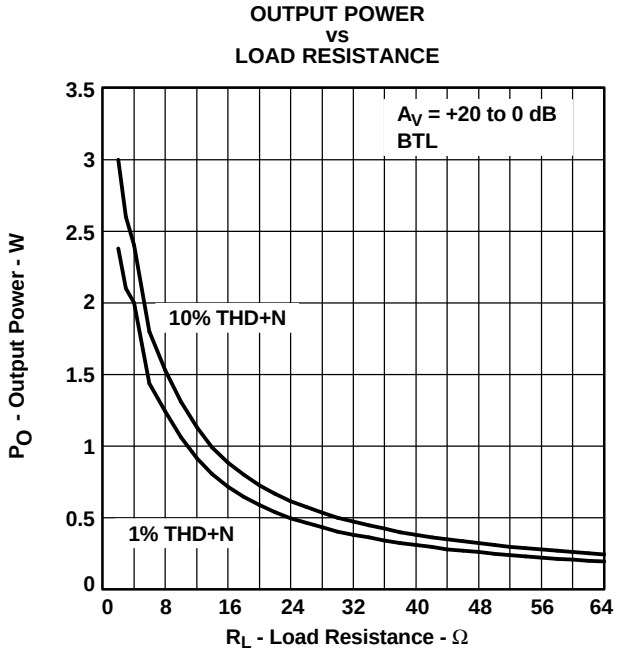


Figure 23.

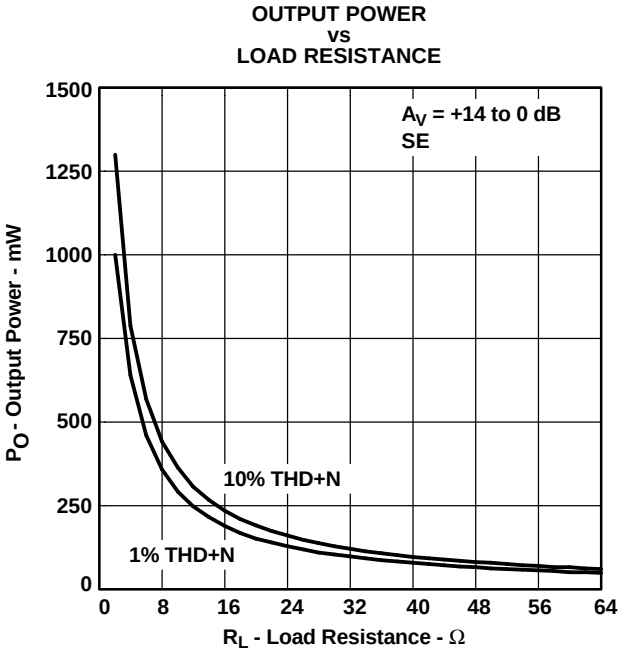


Figure 24.

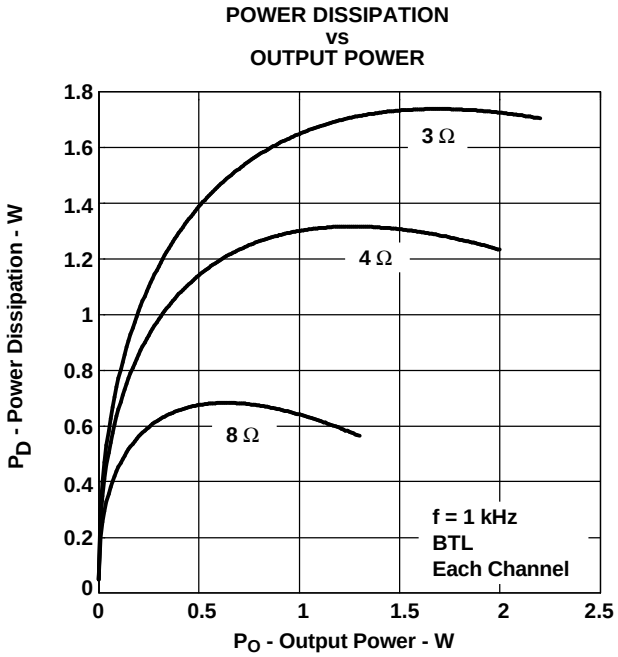


Figure 25.

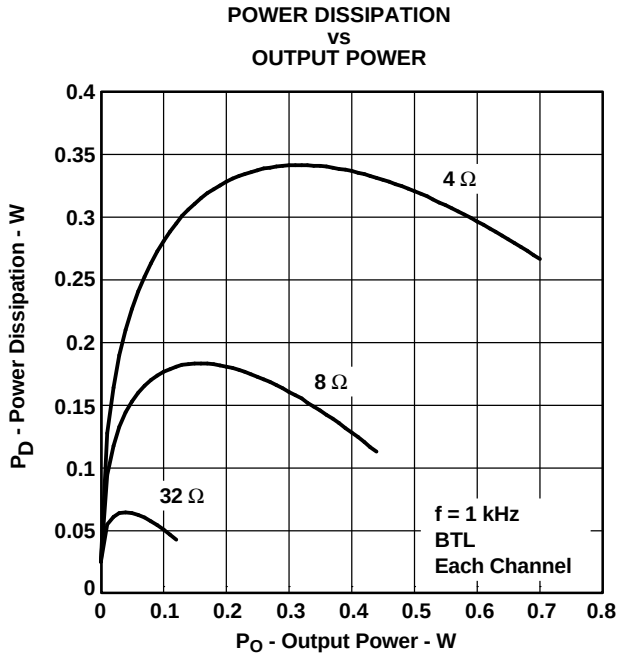


Figure 26.

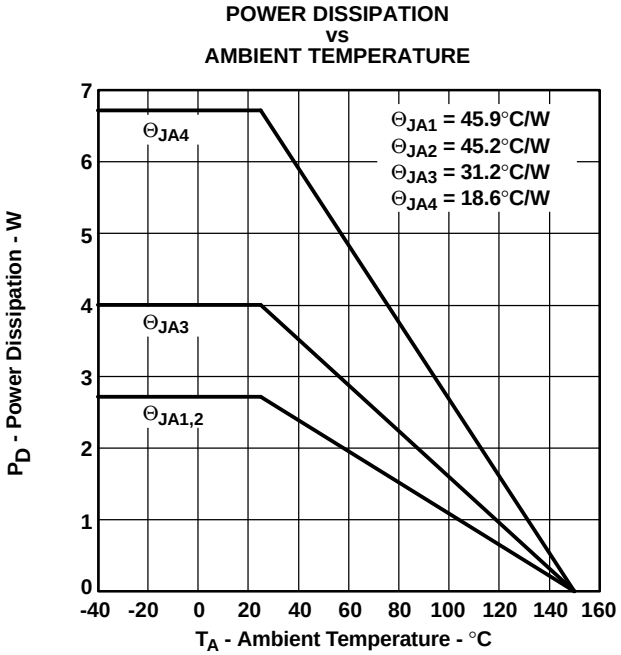


Figure 27.

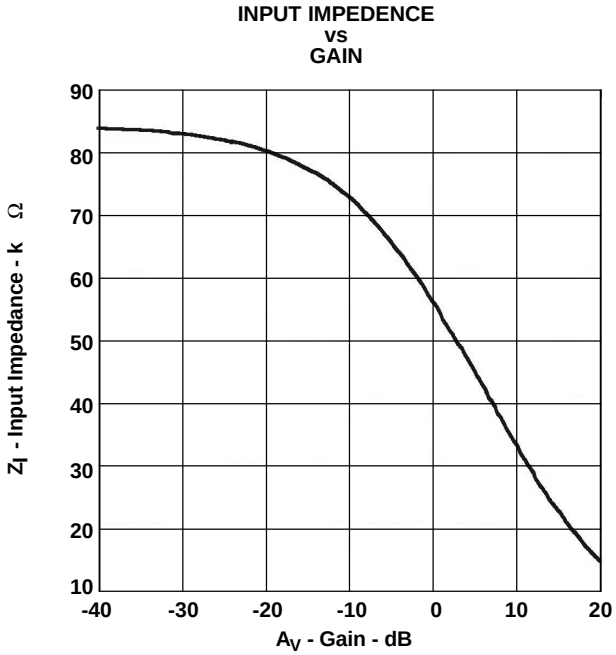


Figure 28.

Volume Control Characteristics

Table 1. Typical DC Volume Control(1)

VOLUME (Terminal 3)		TYPICAL GAIN of AMPLIFIER (dB)(2)
VOLTAGE INCREASING OR FIXED GAIN (V)	VOLTAGE DECREASING (V)	
0-0.27	0.16-0	20
0.28-0.37	0.28-0.17	18
0.38-0.48	0.39-0.29	16
0.49-0.58	0.50-0.40	14
0.59-0.69	0.61-0.51	12
0.70-0.80	0.72-0.62	10
0.81-0.91	0.84-0.73	8
0.92-1.02	0.95-0.85	6
1.03-1.13	1.06-0.96	4
1.14-1.24	1.17-1.07	2
1.25-1.35	1.29-1.18	0
1.36-1.46	1.40-1.30	-2
1.47-1.58	1.51-1.41	-4
1.59-1.68	1.62-1.52	-6
1.69-1.79	1.73-1.63	-8
1.80-1.90	1.84-1.74	-10
1.91-2.01	1.96-1.85	-12
2.02-2.12	2.06-1.97	-14
2.13-2.23	2.18-2.07	-16
2.24-2.34	2.29-2.19	-18
2.35-2.45	2.41-2.30	-20
2.46-2.56	2.52-2.42	-22
2.57-2.67	2.62-2.53	-24
2.68-2.78	2.74-2.63	-26
2.79-2.90	2.86-2.75	-28
2.91-3.01	2.97-2.87	-30
3.02-3.12	3.07-2.98	-32
3.13-3.23	3.19-3.08	-34
3.24-3.33	3.29-3.20	-36
3.34-3.44	3.40-3.30	-38
3.45-3.55	3.53-3.41	-40
3.56-5.00	5.00-3.54	-85

(1) Each step is tested at its midpoint and characterized within ±4dB of the specified gain value for V_{DD} = 5 V. For V_{DD} = 4.5 V to 5.5 V, multiply values by 90% and 110%, respectively.
(2) 95% of the characterized values lie within ±0.5dB of the specified gain value. Figure 29 shows the typical behavior of most devices.

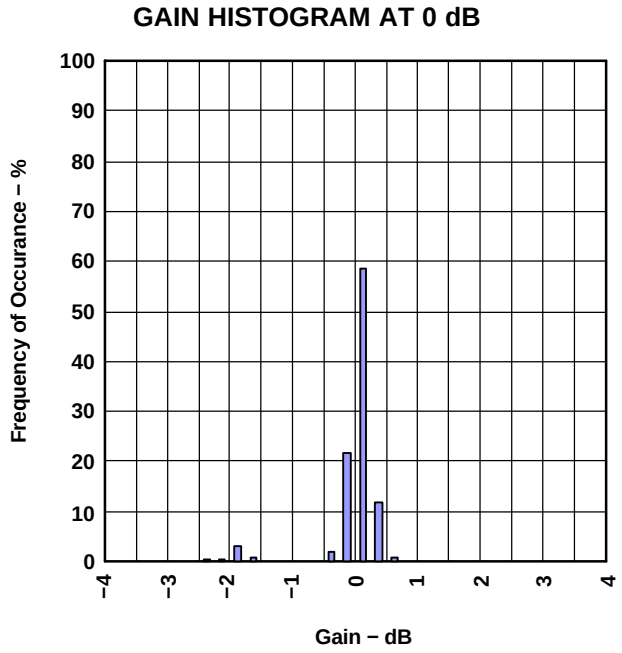


Figure 29. Typical Gain Variance

THERMAL INFORMATION

The thermally enhanced PWP package is based on the 24-pin TSSOP, but includes a thermal pad (see Figure 30) to provide an effective thermal contact between the IC and the PWB.

Traditionally, surface mount and power have been mutually exclusive terms. A variety of scaled-down TO-220-type packages have leads formed as gull wings to make them applicable for surface-mount applications. These packages, however, have only two shortcomings: they do not address the very low profile requirements (<2 mm) of many of today's advanced systems, and they do not offer a terminal-count high enough to accommodate increasing integration. On the other hand, traditional low-power surface-mount packages require power-dissipation derating that severely limits the usable range of many high-performance analog circuits.

The PowerPAD package (thermally enhanced TSSOP) combines fine-pitch, surface-mount technology with thermal performance comparable to much larger power packages.

The PowerPAD package is designed to optimize the heat transfer to the PWB. Because of the very small size and limited mass of a TSSOP package, thermal enhancement is achieved by improving the thermal conduction paths that remove heat from the component. The thermal pad is formed using a patented lead-frame design and manufacturing technique to provide a direct connection to the heat-generating IC. When this pad is soldered or otherwise thermally coupled to an external heat dissipator, high power dissipation in the ultrathin, fine-pitch, surface-mount package can be reliably achieved.

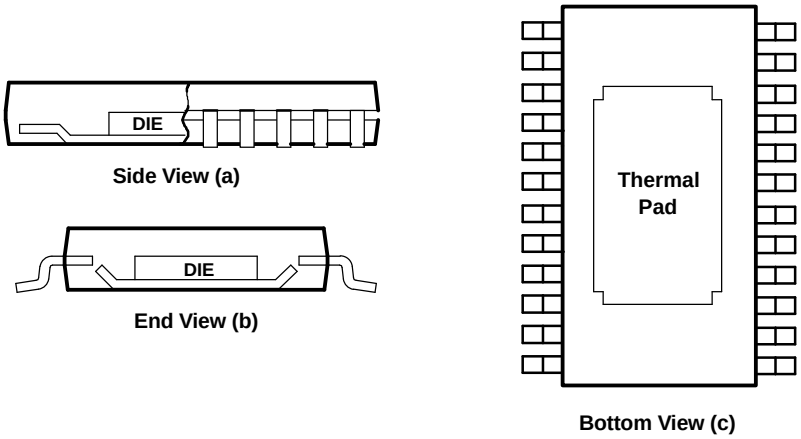
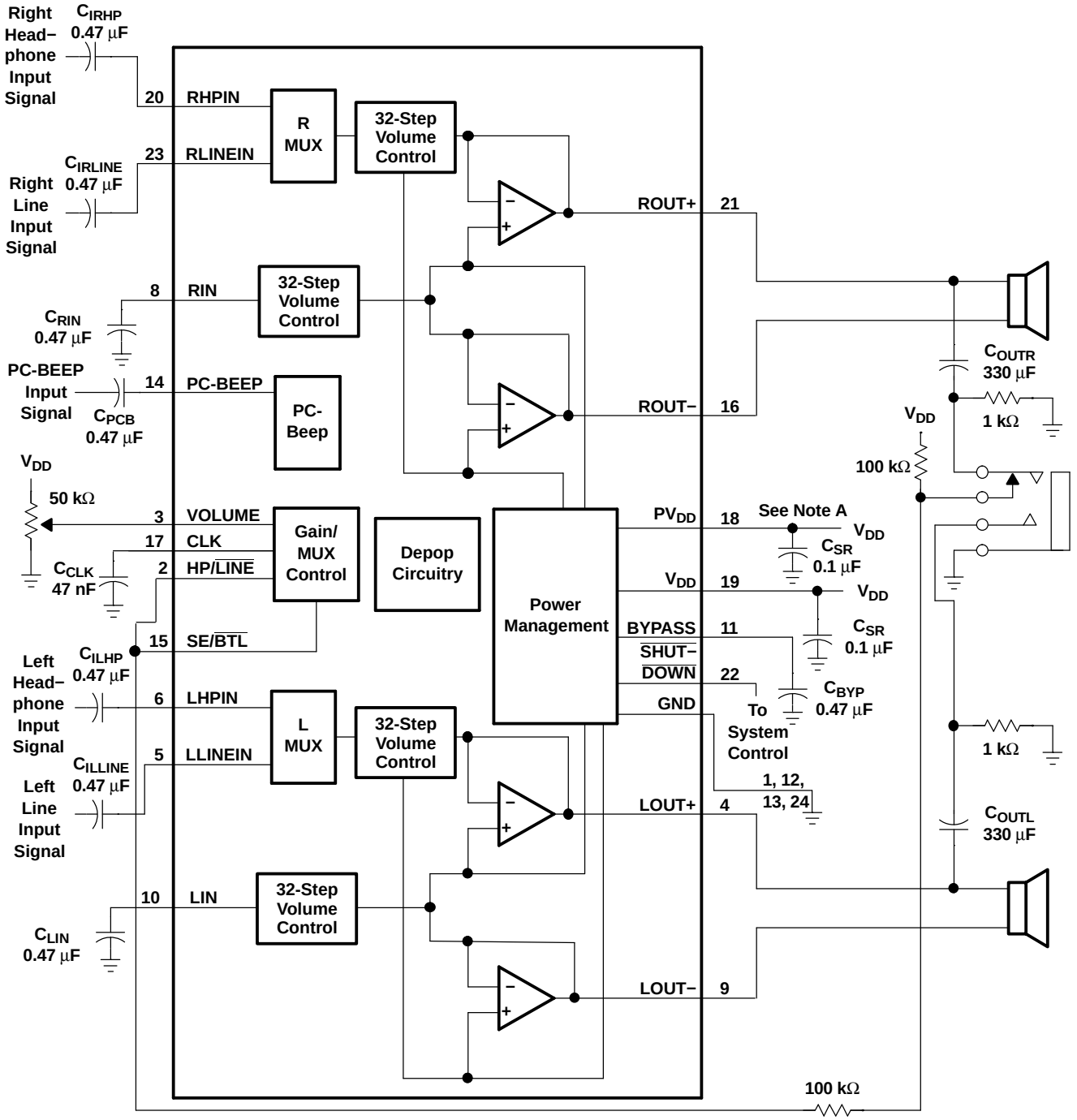


Figure 30. Views of Thermally Enhanced PWP Package

APPLICATION INFORMATION

COMPONENT SELECTION

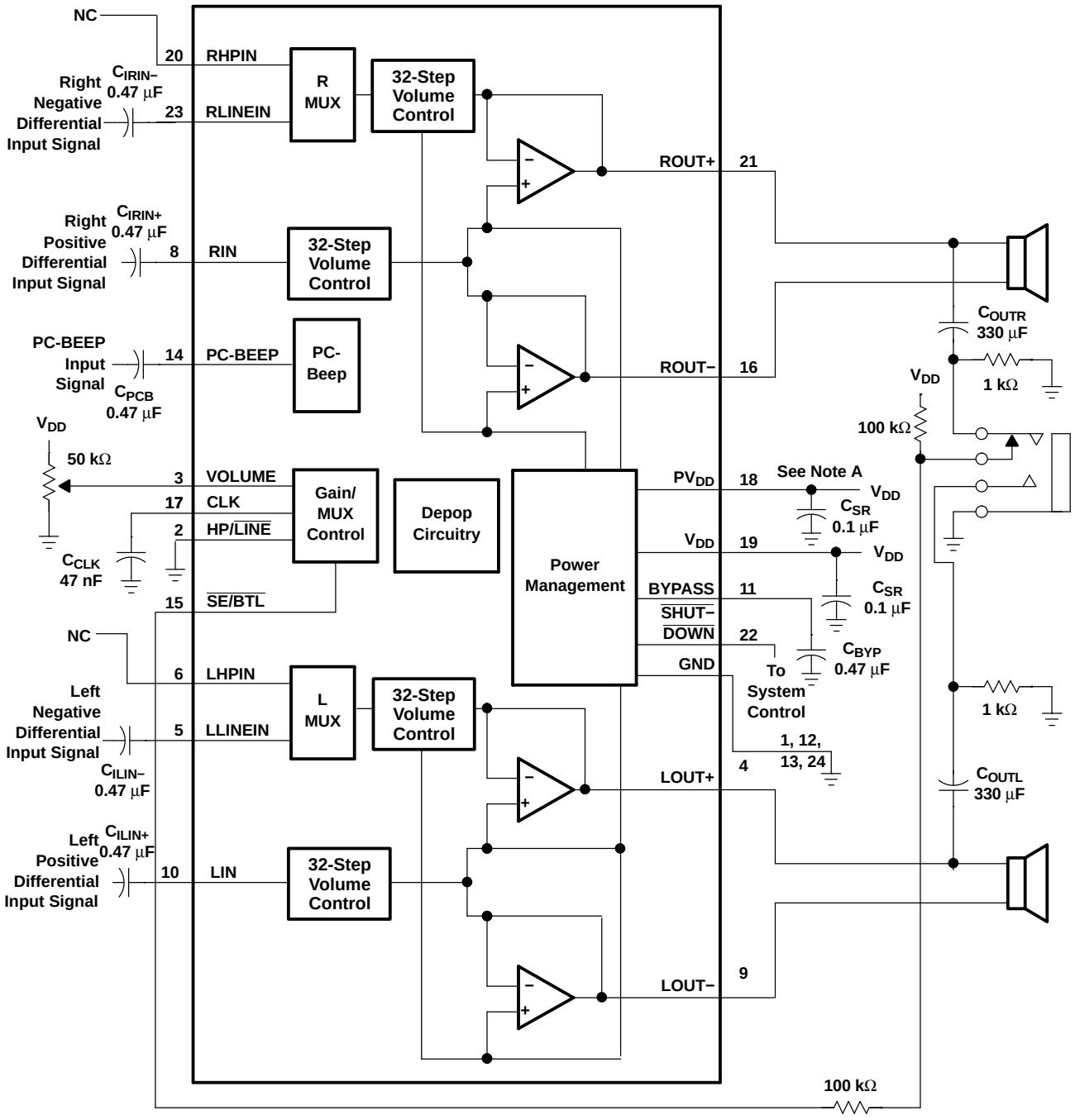
Figure 31 and Figure 32 are schematic diagrams of typical notebook computer application circuits.



A. A 0.1-µF ceramic capacitor should be placed as close as possible to the IC. For filtering lower-frequency noise signals, a larger electrolytic capacitor of 10 µF or greater should be placed near the audio power amplifier.

Figure 31. Typical TPA0232 Application Circuit Using Single-Ended Inputs and Input MUX

APPLICATION INFORMATION (continued)



A. A 0.1-µF ceramic capacitor should be placed as close as possible to the IC. For filtering lower-frequency noise signals, a larger electrolytic capacitor of 10 µF or greater should be placed near the audio power amplifier.

Figure 32. Typical TPA0232 Application Circuit Using Differential Inputs

APPLICATION INFORMATION (continued)

VOLUME CONTROL OPERATION

The VOLUME pin controls the volume of the TPA0232. It is controlled with a dc voltage, which should not ecceed V_{DD}. The gain voltages on the VOLUME pin are given in the Typical Characteristics section.

The trip point, where the gain actually changes, is different depending on whether the voltage on the VOLUME terminal is increasing or decreasing as a result of hysteresis about each trip point. The hysteresis ensures that the gain control is monotonic and does not oscillate from one gain step to another. A pictorial representation of the volume control can be found in Figure 33. The graph focuses on thress gain steps with the trip points defined in in the first and second columns of the Typical DC Volume Control table. The dotted lines represent the hysteresis about each gain step.

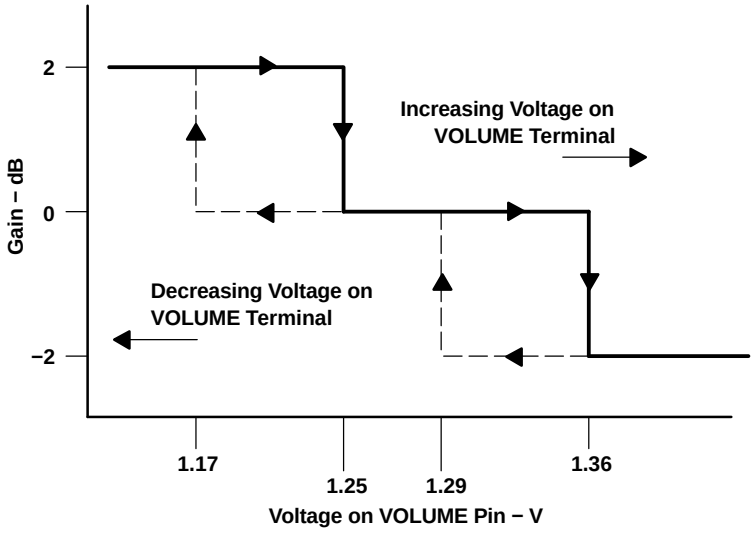


Figure 33. DC Volume Control Operation

INPUT RESISTANCE

The gain is set by varying the input resistance of the amplifier, which can range from its smallest value to over six times that value. As a result, if a single capacitor is used in the input high pass filter, the –3 dB or cut-off frequency also changes by over six times. Connecting an additional resistor from the input pin of the amplifier to ground, as shown in Figure 34, reduces the cutoff-frequency variation.

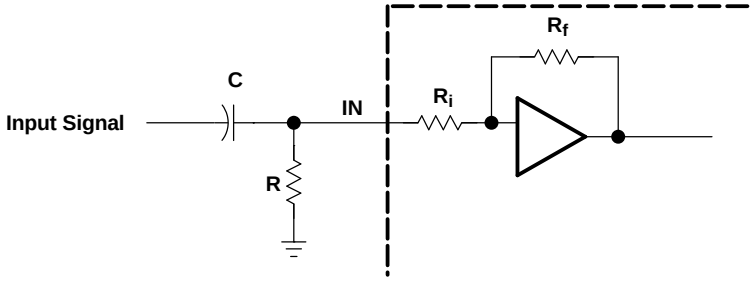


Figure 34. Resistor on Input for Cut-Off Frequency

The input resistance at each gain setting is given in the graph for Input Impedance vs Gain in the Typical Characteristics section.

The –3-dB frequency can be calculated using Equation 1.

APPLICATION INFORMATION (continued)

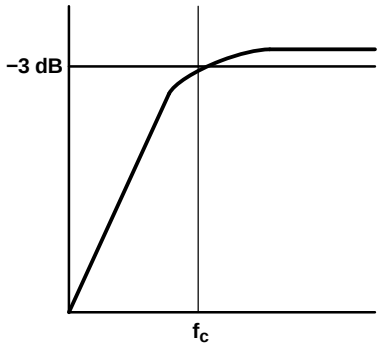
$$f_{-3\ dB} = \frac{1}{2\pi C\left(R \parallel R_i\right)} \quad (1)$$

To increase filter accuracy, increase the value of the capacitor and decrease the value of the resistor to ground. In addition, the order of the filter can be increased.

INPUT CAPACITOR, C_i

In a typical application, an input capacitor (C_i) is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_i and the input impedance of the amplifier (Z_i) form a high-pass filter with the corner frequency determined by Equation 2.

$$f_{c(highpass)} = \frac{1}{2\pi Z_{IN} C_i} \quad (2)$$



The value of C_i directly affects the bass (low frequency) performance of the circuit. Consider the example where Z_i is 55 kΩ and the specification calls for a flat bass response down to 30 Hz. Equation 2 is reconfigured as Equation 3.

$$C_i = \frac{1}{2\pi Z_i f_c} \quad (3)$$

In this example, C_i is 72 nF, so one would likely choose a value in the range of 0.1 µF to 1 µF. A further consideration for this capacitor is the leakage path from the input source through the input network (C_i) and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high-gain applications. For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, connect the positive lead of the capacitor to the amplifier input in most applications, as the dc level there is held at $V_{DD}/2$, typically higher than the source dc level. Note that it is important to confirm the capacitor polarity in the application.

POWER SUPPLY DECOUPLING, $C_{(S)}$

This high-performance CMOS audio amplifier requires adequate power-supply decoupling to minimize output total harmonic distortion (THD). Power-supply decoupling also prevents oscillations with long lead lengths between the amplifier and the speaker. Optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power-supply leads. To filter high-frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 µF, placed as close as possible to the device V_{DD} lead, works best. For filtering low-frequency noise signals, an aluminum electrolytic capacitor of 10 µF or greater placed near the audio power amplifier is recommended.

MIDRAIL BYPASS CAPACITOR, $C_{(BYP)}$

The midrail bypass capacitor, $C_{(BYP)}$, is the most critical capacitor and serves several important functions. During startup or recovery from shutdown mode, $C_{(BYP)}$ determines the rate at which the amplifier starts up. The second function is to reduce power-supply noise coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier, and appears as degraded PSRR and THD+N.

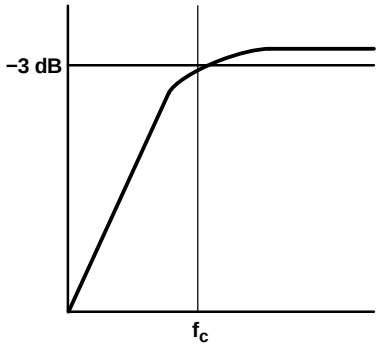
Bypass capacitor ($C_{(BYP)}$) values of 0.47-µF to 1-µF, and ceramic or tantalum low-ESR capacitors are recommended for best THD and noise performance.

APPLICATION INFORMATION (continued)

OUTPUT COUPLING CAPACITOR, $C_{(C)}$

In a typical single-supply SE configuration, an output coupling capacitor ($C_{(C)}$) is required to block the dc bias at the output of the amplifier to prevent dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by Equation 4.

$$f_{c(high)} = \frac{1}{2\pi R_L C_{(C)}} \quad (4)$$



The main disadvantage, from a performance standpoint, is that load impedances are typically small, driving the low-frequency corner higher, degrading the bass response. Large values of $C_{(C)}$ are required to pass low frequencies into the load. Consider the example where a $C_{(C)}$ of 330 µF is chosen and loads include 3 Ω, 4 Ω, 8 Ω, 32 Ω, 10 kΩ, and 47 kΩ. Table 2 summarizes the frequency response characteristics of each configuration.

Table 2. Common Load Impedances Vs Low Frequency Output Characteristics in SE Mode

R_L	$C_{(C)}$	LOWEST FREQUENCY
3 Ω	330 µF	161 Hz
4 Ω	330 µF	120 Hz
8 Ω	330 µF	60 Hz
32 Ω	330 µF	15 Hz
10,000 Ω	330 µF	0.05 Hz
47,000 Ω	330 µF	0.01 Hz

As Table 2 indicates, most of the bass response is attenuated into a 4-Ω load, an 8-Ω load is adequate, headphone response is good, and drive into line level inputs (a home stereo for example) is exceptional.

USING LOW-ESR CAPACITORS

Low-ESR capacitors are recommended throughout this applications section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

BRIDGED-TIED LOAD VS SINGLE-ENDED MODE

Figure 35 shows a Class-AB audio power amplifier (APA) in a BTL configuration. The TPA0232 amplifier consists of two Class-AB amplifiers driving both ends of the load. There are several potential benefits to this differential drive configuration, but, initially consider power to the load. The differential drive to the speaker means that as one side is slewing up, the other side is slewing down, and vice versa. This in effect doubles the voltage swing on the load as compared to a ground referenced load. Substituting $2 \times V_{O(PP)}$ into the power equation, where voltage is squared, yields 4× the output power from the same supply rail and load impedance (see Equation 5).

$$V_{(rms)} = \frac{V_{O(PP)}}{2\sqrt{2}}$$

$$\text{Power} = \frac{V_{(rms)}^2}{R_L} \quad (5)$$

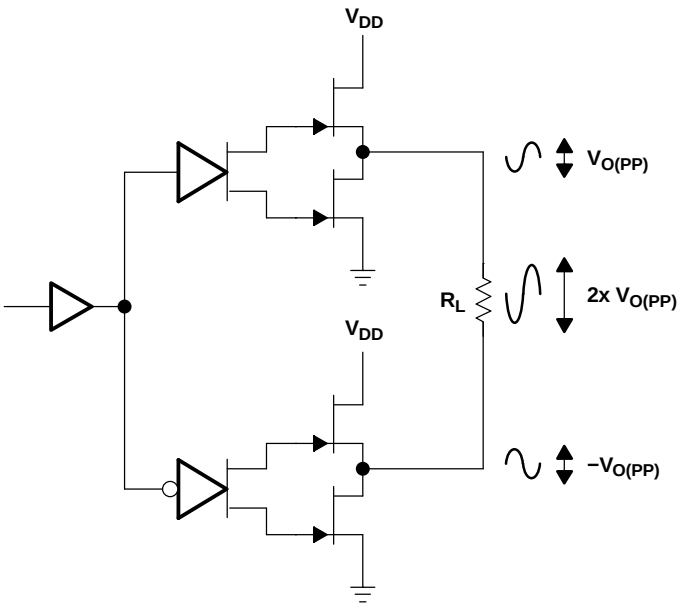


Figure 35. Bridge-Tied Load Configuration

In a typical computer sound channel operating at 5 V, bridging raises the power into an 8-Ω speaker from a singled-ended (SE, ground reference) limit of 250 mW to 1 W. In sound power, this is a 6-dB improvement — loudness that can be heard. In addition to increased power there are frequency-response concerns. Consider the single-supply SE configuration shown in Figure 36. A coupling capacitor is required to block the dc offset voltage from reaching the load. These capacitors can be quite large (approximately 33 µF to 1000 µF), so they tend to be expensive, heavy, occupy valuable PCB area, and have the additional drawback of limiting the low-frequency performance of the system. This frequency-limiting effect is due to the high-pass filter network created with the speaker impedance and the coupling capacitance, and is calculated with Equation 6.

$$f_{(c)} = \frac{1}{2\pi R_L C_{(C)}} \quad (6)$$

For example, a 68-µF capacitor with an 8-Ω speaker would attenuate low frequencies below 293 Hz. The BTL configuration cancels the dc offsets, eliminating the need for blocking capacitors. Low-frequency performance is then limited only by the input network and speaker response. Cost and PCB space are also minimized by eliminating the bulky coupling capacitor.

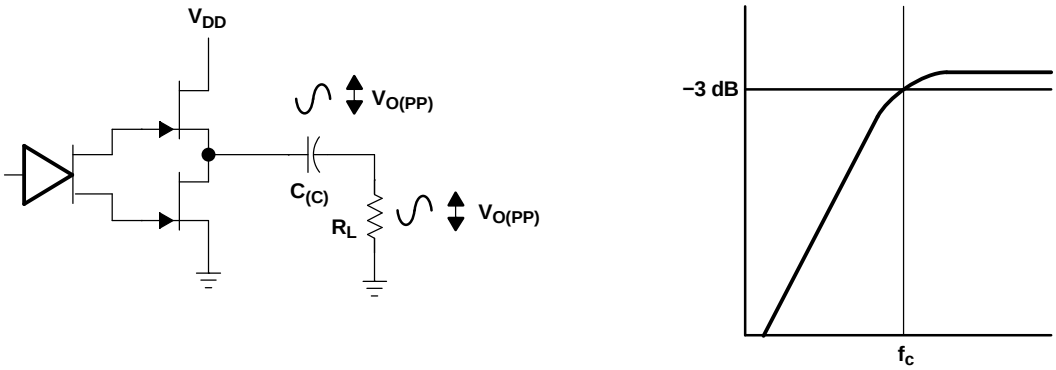


Figure 36. Single-Ended Configuration and Frequency Response

Increasing power to the load does carry a penalty of increased internal power dissipation. The increased dissipation is understandable, since the BTL configuration produces 4× the output power of the SE configuration. Internal dissipation versus output power is discussed further in the *Crest Factor and Thermal Considerations* section.

Single-Ended Operation

In SE mode (see Figure 36), the load is driven from the primary amplifier output for each channel (LOUT+ and ROUT+).

The amplifier switches to single-ended operation when the SE/$\overline{\text{BTL}}$ terminal is held high. This puts the negative outputs in a high-impedance state, and reduces the amplifier's gain by 6 dB.

For example, a 68-µF capacitor with an 8-Ω speaker would attenuate low frequencies below 293 Hz. The BTL configuration cancels the dc offsets, which eliminates the need for the blocking capacitors. Low-frequency performance is then limited only by the input network and speaker response. Cost and PCB space are also minimized by eliminating the bulky coupling capacitor.

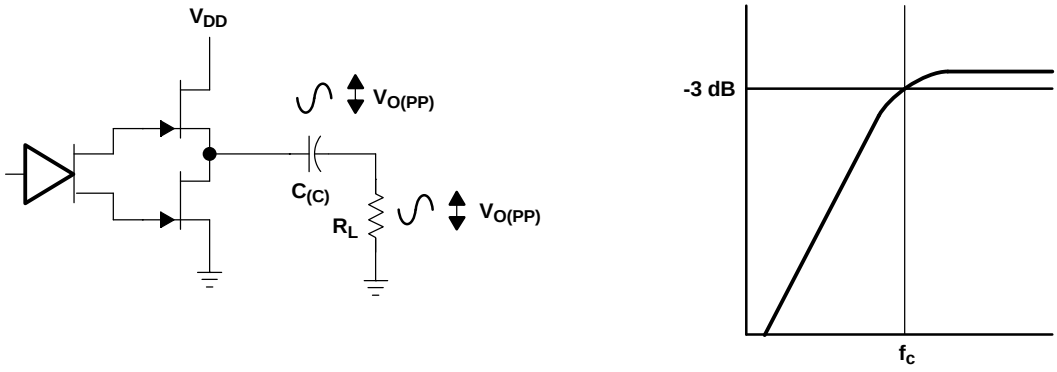


Figure 37. Single-Ended Configuration and Frequency Response

Increasing power to the load does carry a penalty of increased internal power dissipation. The increased dissipation is understandable considering that the BTL configuration produces 4× the output power of the SE configuration. Internal dissipation versus output power is discussed further in the *crest factor and thermal considerations* section.

BTL AMPLIFIER EFFICIENCY

Class-AB amplifiers are inefficient, primarily because of voltage drop across the output-stage transistors. The two components of the internal voltage drop are the headroom or dc voltage drop that varies inversely to output power, and the sine wave nature of the output. The total voltage drop can be calculated by subtracting the RMS value of the output voltage from V_{DD}. The internal voltage drop multiplied by the RMS value of the supply current (I_{DD}rms) determines the internal power dissipation of the amplifier.

An easy-to-use equation to calculate efficiency begins as the ratio of power from the power supply to the power delivered to the load. To accurately calculate the RMS and average values of power in the load and in the amplifier, the current and voltage waveforms must be understood (see Figure 38).

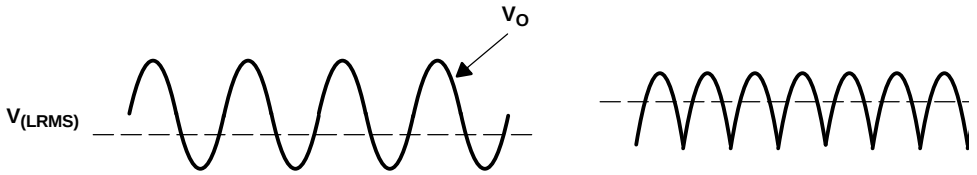


Figure 38. Voltage and Current Waveforms for BTL Amplifiers

Although the voltages and currents for SE and BTL are sinusoidal in the load, currents from the supply are very different between SE and BTL configurations. In an SE application, the current waveform is a half-wave rectified shape, whereas in BTL it is a full-wave rectified waveform. Therefore, RMS conversion factors are different. Keep in mind that for most of the waveform both the push and pull transistors are not on at the same time, which supports the fact that each amplifier in the BTL device only draws current from the supply for half the waveform. Equation 7 and Equation 8 are the basis for calculating amplifier efficiency.

$$\text{Efficiency of a BTL amplifier} = \frac{P_L}{P_{SUP}}$$

Where:

$$P_L = \frac{V_L rms^2}{R_L}, \text{ and } V_{LRMS} = \frac{V_P}{\sqrt{2}}, \text{ therefore, } P_L = \frac{V_P{}^2}{2R_L}$$

$$\text{and} \quad P_{SUP} = V_{DD}\, I_{DD}avg \qquad \text{and} \qquad I_{DD}avg = \frac{1}{\pi}\int_0^{\pi} \frac{V_P}{R_L} \sin(t)\, dt = -\frac{1}{\pi} \times \frac{V_P}{R_L} [\cos(t)]_0^{\pi} = \frac{2V_P}{\pi R_L}$$

Therefore,

$$P_{SUP} = \frac{2\, V_{DD}\, V_P}{\pi\, R_L}$$

substituting P_L and P_{SUP} into equation 7,

$$\text{Efficiency of a BTL amplifier} = \frac{\frac{V_P{}^2}{2\, R_L}}{\frac{2\, V_{DD}\, V_P}{\pi\, R_L}} = \frac{\pi\, V_P}{4\, V_{DD}}$$

Where:

$$V_P = \sqrt{2\, P_L\, R_L} \tag{7}$$

Therefore,

$$\eta_{BTL} = \frac{\pi \sqrt{2\, P_L\, R_L}}{4\, V_{DD}}$$

P_L = Power delivered to load
P_{SUP} = Power drawn from power supply
V_{LRMS} = RMS voltage on BTL load
R_L = Load resistance
V_P = Peak voltage on BTL load
$I_{DD}avg$ = Average current drawn from the power supply
V_{DD} = Power supply voltage
η_{BTL} = Efficiency of a BTL amplifier

(8)

Table 3 employs Equation 8 to calculate efficiencies for four different output-power levels. Note that the efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in a nearly flat internal power dissipation over the normal operating range. Note that the internal dissipation at full output power is less than in the half-power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a stereo 1-W audio system with 8-Ω loads and a 5-V supply, the maximum draw on the power supply is almost 3.25 W.

Table 3. Efficiency vs Output Power in 5-V, 8-Ω BTL Systems

OUTPUT POWER (W)	EFFICIENCY (%)	PEAK VOLTAGE (V)	INTERNAL DISSIPATION (W)
0.25	31.4	2.00	0.55
0.50	44.4	2.83	0.62
1.00	62.8	4.00	0.59
1.25	70.2	4.47(1)	0.53

(1) High peak voltages cause the THD to increase.

A final point to remember about Class-AB amplifiers (either SE or BTL) is how to manipulate the terms in the efficiency equation to utmost advantage when possible. Note that in Equation 8, V_{DD} is in the denominator. This indicates that as V_{DD} goes down, efficiency goes up.

CREST FACTOR AND THERMAL CONSIDERATIONS

Class-AB power amplifiers dissipate a significant amount of heat in the package under normal operating conditions. A typical music CD requires 12 dB to 15 dB of dynamic range, or headroom, above the average power output, to pass the loudest portions of the signal without distortion. In other words, music typically has a crest factor between 12 dB and 15 dB. When determining the optimal ambient operating temperature, the internal dissipated power at the average output power level must be used. From the data sheet, one can see that when the device is operating from a 5-V supply into a 3-Ω speaker that 4-W peaks are available. Use Equation 9 to convert watts to dB.

$$P_{dB} = 10 \text{Log} \frac{P_W}{P_{ref}} = 10 \text{Log} \frac{4 \text{ W}}{1 \text{ W}} = 6 \text{ dB} \quad (9)$$

Subtracting the headroom restriction to obtain the average listening level without distortion yields:

6 dB - 15 dB = -9 dB (15-dB crest factor)
6 dB - 12 dB = -6 dB (12-dB crest factor)
6 dB - 9 dB = -3 dB (9-dB crest factor)
6 dB - 6 dB = 0 dB (6-dB crest factor)
6 dB - 3 dB = 3 dB (3-dB crest factor)

Converting dB back into watts:

$P_W = 10^{PdB/10} \times P_{ref}$
= 63 mW (18-dB crest factor)
= 125 mW (15-dB crest factor)
= 250 mW (9-dB crest factor)
= 500 mW (6-dB crest factor)
= 1000 mW (3-dB crest factor)
= 2000 mW (0-dB crest factor)

This is valuable information to consider when estimating the heat-dissipation requirements for the amplifier system. Comparing the worst case, 2 W of continuous power output with a 3-dB crest factor, against 12-dB and 15-dB applications, drastically affects maximum ambient temperature ratings for the system. Using the power dissipation curves for a 5-V, 3-Ω system, the internal dissipation and maximum ambient temperatures are shown in the table below.

Table 4. TPA0232 Power Rating, 5-V, 3-Ω Stereo

PEAK OUTPUT POWER (W)	AVERAGE OUTPUT POWER	POWER DISSIPATION (W/CHANNEL)	MAXIMUM AMBIENT TEMPERATURE
4	2 W (3 dB)	1.7	-3°C
4	1000 mW (6 dB)	1.6	6°C
4	500 mW (9 dB)	1.4	24°C
4	250 mW (12 dB)	1.1	51°C
4	125 mW (15 dB)	0.8	78°C
4	63 mW (18 dB)	0.6	85°C(1)

(1) Package limited to 85°C ambient.

Table 5. TPA0232 Power Rating, 5-V, 8-Ω Stereo

PEAK OUTPUT POWER (W)	AVERAGE OUTPUT POWER	POWER DISSIPATION (W/Channel)	MAXIMUM AMBIENT TEMPERATURE(1)
2.5	1250 mW (3-dB crest factor)	0.55	85°C
2.5	1000 mW (4-dB crest factor)	0.62	85°C
2.5	500 mW (7-dB crest factor)	0.59	85°C
2.5	250 mW (10-dB crest factor)	0.53	85°C

(1) Package limited to 85°C ambient.

The maximum dissipated power (P_{Dmax}) is reached at a much lower output power level for a 3-Ω load than for an 8-Ω load. As a result, the formula in Equation 10for calculating P_{Dmax} may be used for a 3-Ω application:

$$P_{Dmax} = \frac{2V_{DD}^2}{\pi^2 R_L} \tag{10}$$

However, in the case of an 8-Ω load, the P_{Dmax} occurs at a point well above the normal operating power level. The amplifier may therefore be operated at a higher ambient temperature than required by the P_{Dmax} formula for an 8-Ω load, but do not exceed the maximum ambient temperature of 85°.

The maximum ambient temperature depends on the heatsinking ability of the PCB system. The derating factor for the PWP package is shown in the dissipation rating table. Converting this to θ_{JA}:

$$\theta_{JA} = \frac{1}{\text{Derating Factor}} = \frac{1}{0.022} = 45°C/W \tag{11}$$

To calculate maximum ambient temperatures, first consider that the numbers from the dissipation graphs are per-channel, so the dissipated heat is doubled for two-channel operation. Given θ_{JA}, the maximum allowable junction temperature, and the total internal dissipation, the maximum ambient temperature can be calculated using Equation 12. The maximum recommended junction temperature for the device is 150°C. The internal dissipation figures are taken from the Power Dissipation vs Output Power graphs.

$$\begin{aligned} T_A\,\text{Max} &= T_J\,\text{Max} - \theta_{JA} P_D \\ &= 150 - 45(0.6 \times 2) = 96°C \text{ (15-dB crest factor)} \end{aligned} \tag{12}$$

NOTE:

Internal dissipation of 0.6 W is estimated for a 2-W system with 15-dB crest factor per channel.
Due to package limitiations, the actual T_{AMAX} is 85°C.

The power rating tables show that for some applications, no airflow is required to keep junction temperatures in the specified range. The internal thermal protection turns the device off at junction temperatures higher than 150°C to prevent damage to the IC. The power rating tables in this section were calculated for maximum listening volume without distortion. When the output level is reduced the numbers in the table change significantly. Also, using 8-Ω speakers dramatically increases the thermal performance by increasing amplifier efficiency.

SE/$\overline{\text{BTL}}$ OPERATION

The ability of the TPA0232 to easily switch between BTL and SE modes is one of its most important cost-saving features. This feature eliminates the requirement for an additional headphone amplifier in applications where internal stereo speakers are driven in BTL mode but external headphone or speakers must be accommodated. Two separate internal amplifiers drive OUT+ and OUT–. The SE/$\overline{\text{BTL}}$ input controls the operation of the follower amplifier that drives LOUT– and ROUT–. When SE/$\overline{\text{BTL}}$ is held low, the amplifier is on and the device is in the BTL mode. When SE/$\overline{\text{BTL}}$ is held high, the OUT– amplifiers are in a high output-impedance state, which configures the device outputs as SE drivers from LOUT+ and ROUT+. I_{DD} is reduced by approximately one-half in SE mode. Control of the SE/$\overline{\text{BTL}}$ input can be from a logic-level CMOS source or, more typically, from a resistor-divider network as shown in Figure 39.

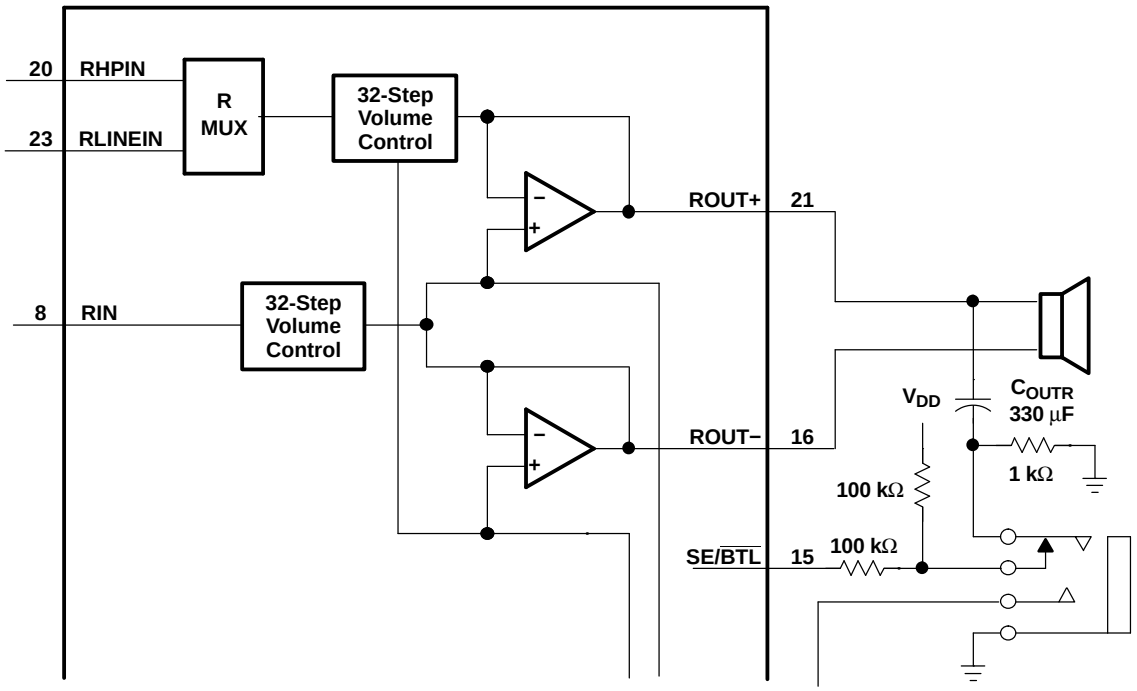


Figure 39. TPA0232 Resistor Divider Network Circuit

Using a readily-available 1/8-in. (3,5 mm) stereo headphone jack, the control switch is closed when no plug is inserted. When closed, the 100-kΩ/1-kΩ divider pulls the SE/$\overline{\text{BTL}}$ input low. When a plug is inserted, the 1-kΩ resistor is disconnected and the SE/$\overline{\text{BTL}}$ input is pulled high. When the input goes high, the OUT– amplifier is shut down, muting the speaker (virtually open-circuits the speaker). The OUT+ amplifier then drives through the output capacitor (C_O) into the headphone jack.

PC-BEEP OPERATION

The PC-BEEP input allows a system beep to be sent directly from a computer through the amplifier to the speakers with few external components. The input is activated automatically. When the PC-BEEP input is active, both LINEIN and HPIN inputs are deselected, and both the left and right channels are driven in BTL mode with the signal from PC-BEEP. The gain from the PC-BEEP input to the speakers is fixed at 0.3 V/V and is independent of the volume setting. When the PC-BEEP input is deselected, the amplifier returns to the previous operating mode and volume setting. Furthermore, if the amplifier is in shutdown mode, activating PC-BEEP takes the device out of shutdown, outputs the PC-BEEP signal, then returns the amplifier to shutdown mode.

The preferred input signal is a square wave or pulse train. To be accurately detected, the signal must have a minimum of 1.5-V_{pp} amplitude, rise and fall times of less than 0.1 µs and a minimum of eight rising edges. When the signal is no longer detected, the amplifier returns to its previous operating mode and volume setting.

To ac-couple the PC-BEEP input, choose a coupling-capacitor value to satisfy Equation 13.

$$C_{PCB} \geq \frac{1}{2\pi f_{PCB}(100\ k\Omega)} \quad (13)$$

The PC-BEEP input can also be dc-coupled to avoid using this coupling capacitor. The pin normally rests at midrail when no signal is present.

SHUTDOWN MODES

The TPA0232 shutdown mode minimizes supply current (I_{DD}) during periods of nonuse to conserve battery power. The $\overline{\text{SHUTDOWN}}$ input terminal must be held high during normal operation when the amplifier is in use. Pulling $\overline{\text{SHUTDOWN}}$ low mutes the outputs and puts the amplifier into a low-current state, with I_{DD} = 150 µA. $\overline{\text{SHUTDOWN}}$ is never left unconnected because amplifier operation would be unpredictable.

Table 6. HP/$\overline{\text{LINE}}$, SE/$\overline{\text{BTL}}$, and Shutdown Functions

INPUTS(1)			AMPLIFIER STATE	
HP/$\overline{\text{LINE}}$	SE/$\overline{\text{BTL}}$	$\overline{\text{SHUTDOWN}}$	INPUT	OUTPUT
X(2)	X(2)	Low	X(2)	Mute
Low	Low	High	Line	BTL
Low	High	High	Line	SE
High	Low	High	HP	BTL
High	High	High	HP	SE

(1) Do not leave inputs unconnected.
(2) X = do not care

INPUT MUX OPERATION

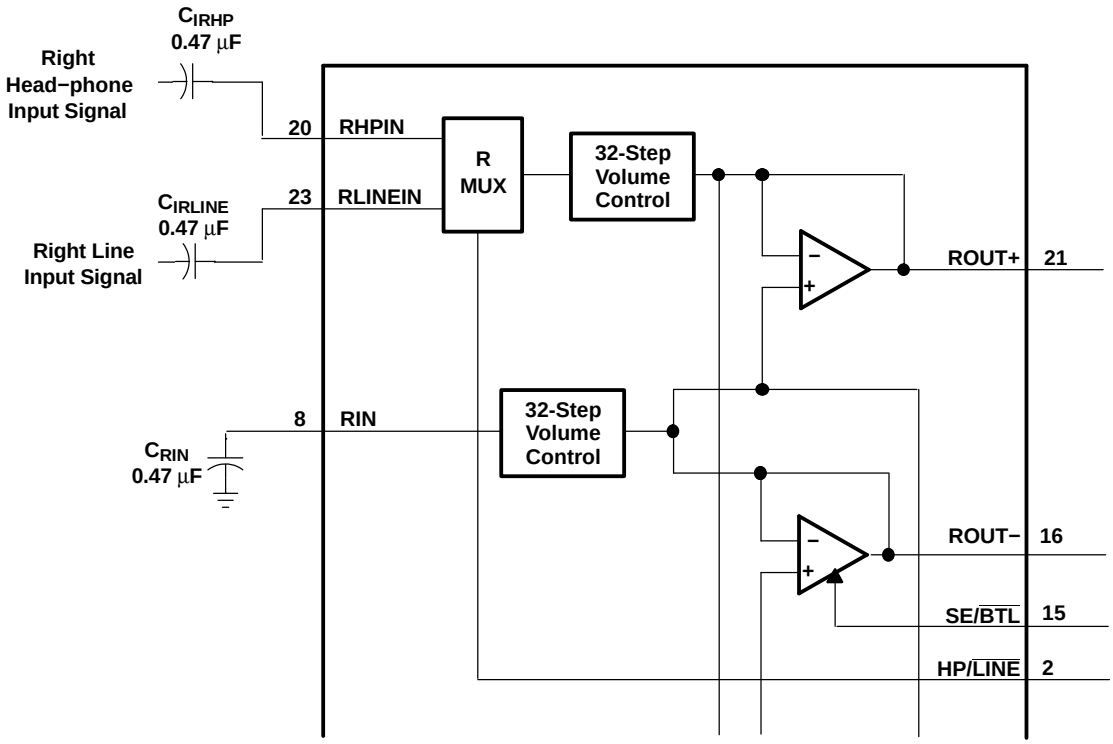


Figure 40. TPA0232 Example Input MUX Circuit

The TPA0232 offers the capability for the designer to use separate headphone inputs (RHPIN, LHPIN) and line inputs (RLINEIN, LLINEIN). The inputs can be different if the input signal is single-ended. If using a differential input signal, the inputs must be the same because the inputs share a common RIN, LIN. Although the typical application in Figure 31 shows the input mux control signal HP/LINE tied to SE/BTL, that configuration is not required. The input mux can be used to select between two inputs that are used in both SE and BTL modes.

If using the TPA0232 with a single-ended input, the RIN and LIN terminals must be tied through a capacitor to ground, as shown in Figure 40. RIN and LIN must not be tied to bypass or an offset occurs on the output causing the device to pop when turning on and off.

Input coupling capacitors can be eliminated when using differential inputs, but are used to obtain maximum output power. If the input capacitors are eliminated, the dc offset must match the voltage on BYPASS or the output power is limited.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPA0232PWP	ACTIVE	HTSSOP	PWP	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPA0232	Samples
TPA0232PWPG4	ACTIVE	HTSSOP	PWP	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPA0232	Samples
TPA0232PWPR	ACTIVE	HTSSOP	PWP	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPA0232	Samples
TPA0232PWPRG4	ACTIVE	HTSSOP	PWP	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPA0232	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

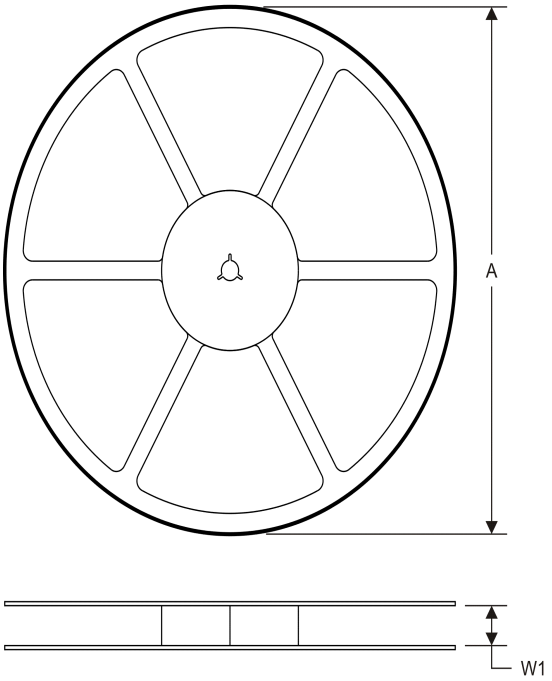
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

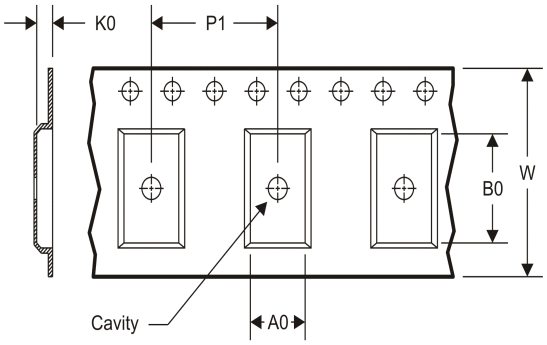
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



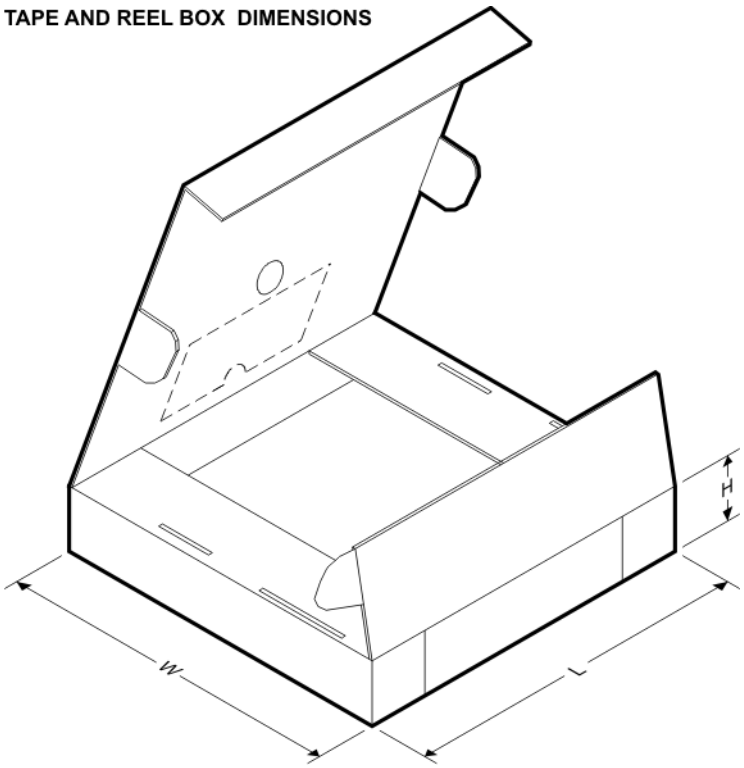
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA0232PWPR	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

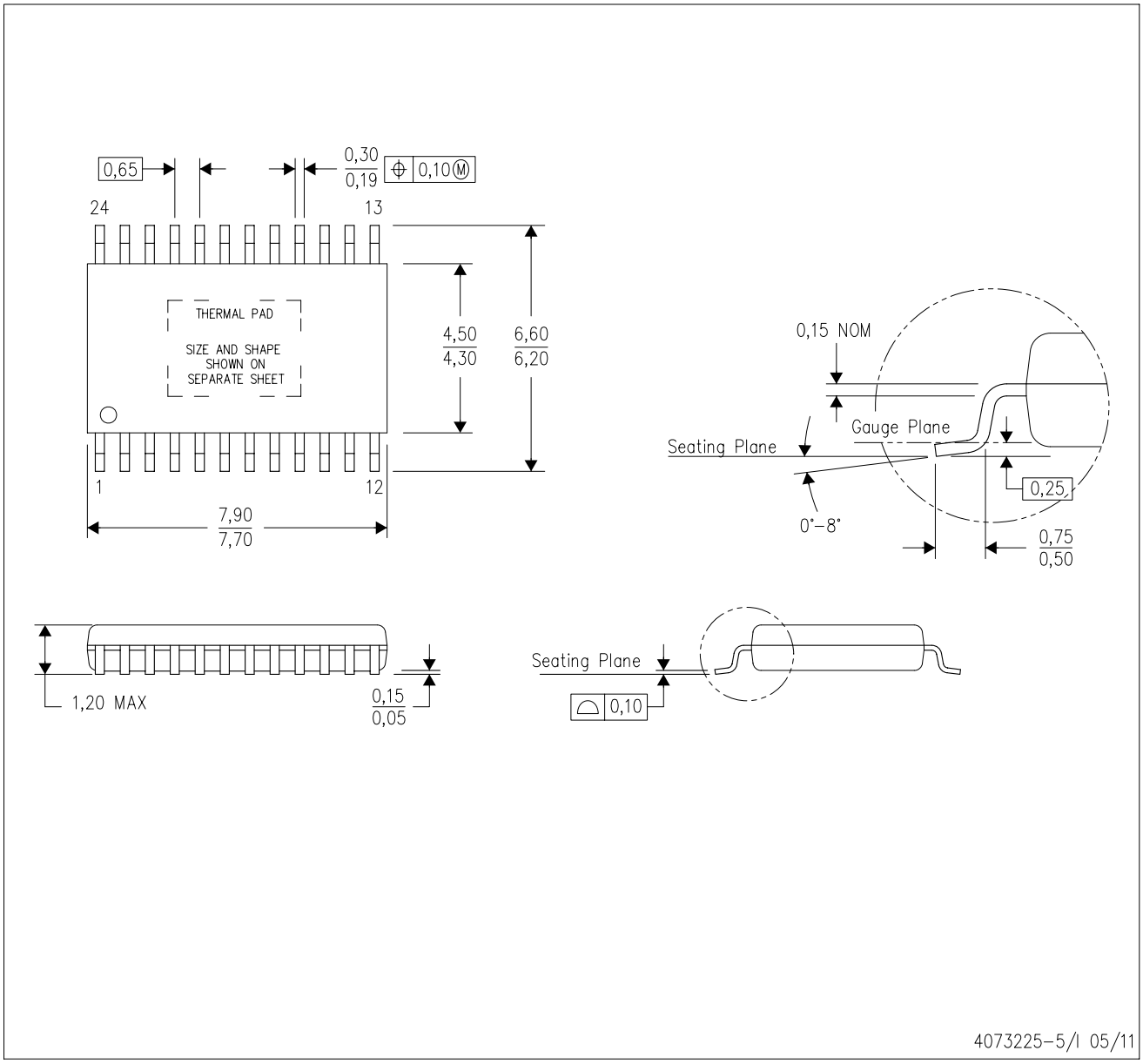
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA0232PWPR	HTSSOP	PWP	24	2000	367.0	367.0	38.0

PWP (R–PDSO–G24) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

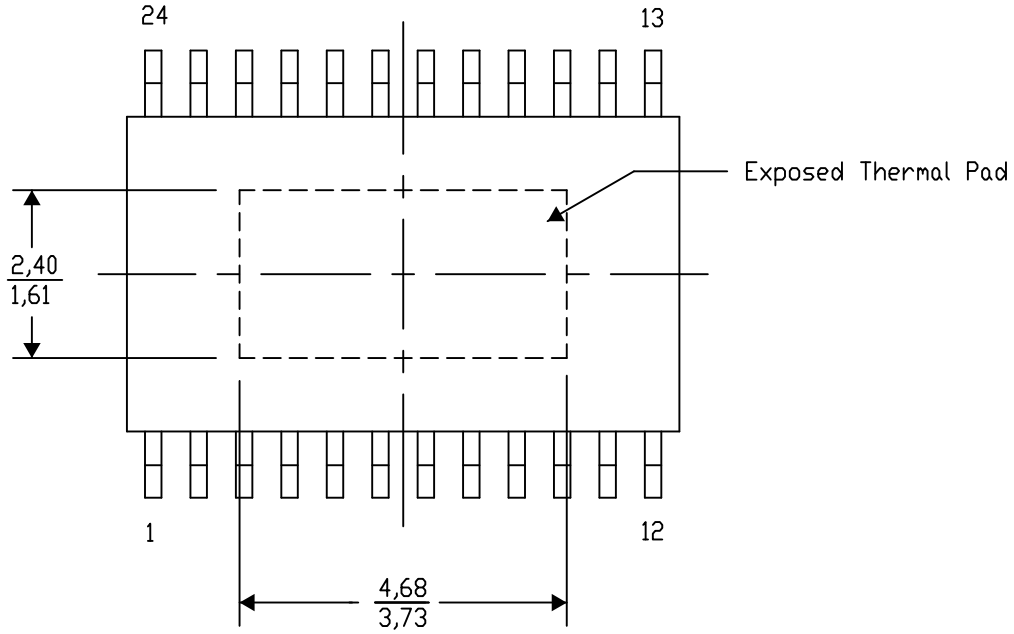
PWP (R–PDSO–G24) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

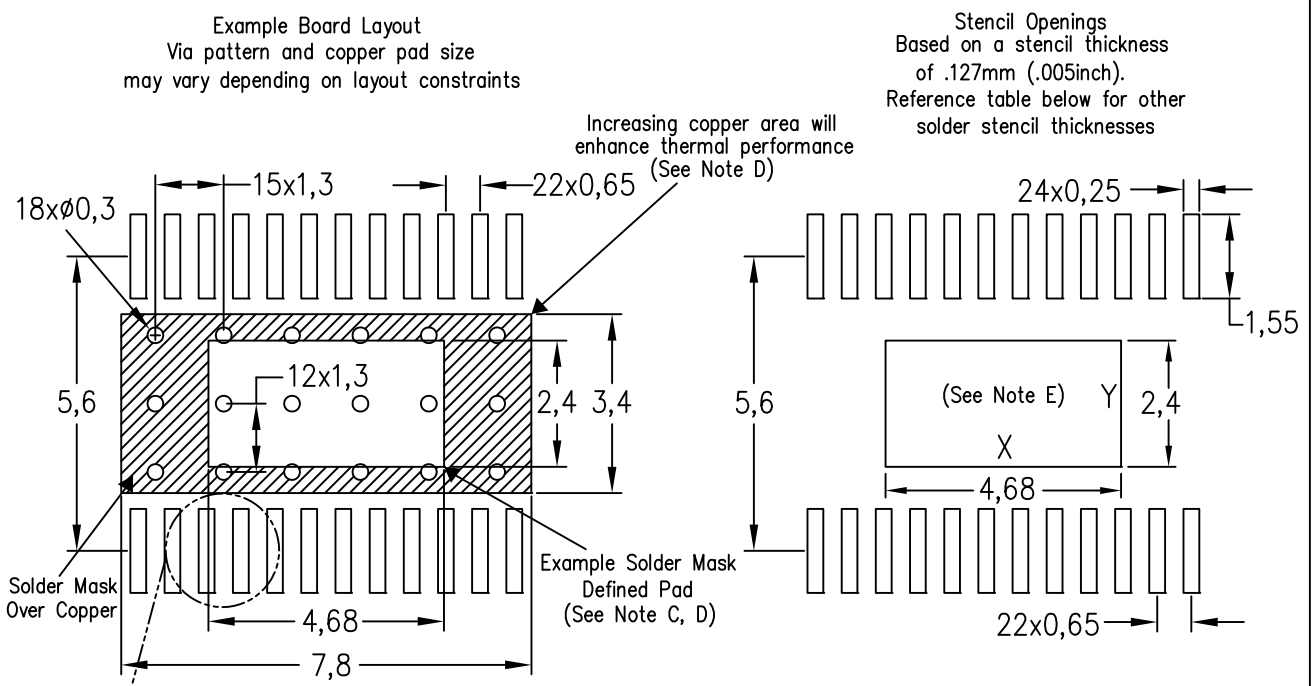
Exposed Thermal Pad Dimensions

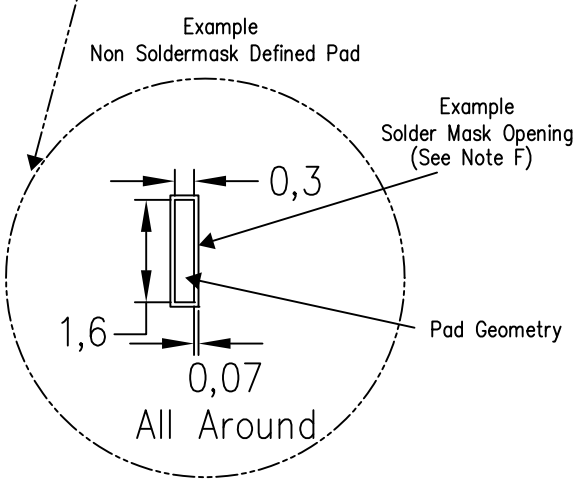
4206332–27/AG 08/13

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G24) PowerPAD™ PLASTIC SMALL OUTLINE





Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	5.0	2.6
0.127mm	4.68	2.4
0.152mm	4.3	2.2
0.178mm	4.2	2.1

4207609–14/T 08/13

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

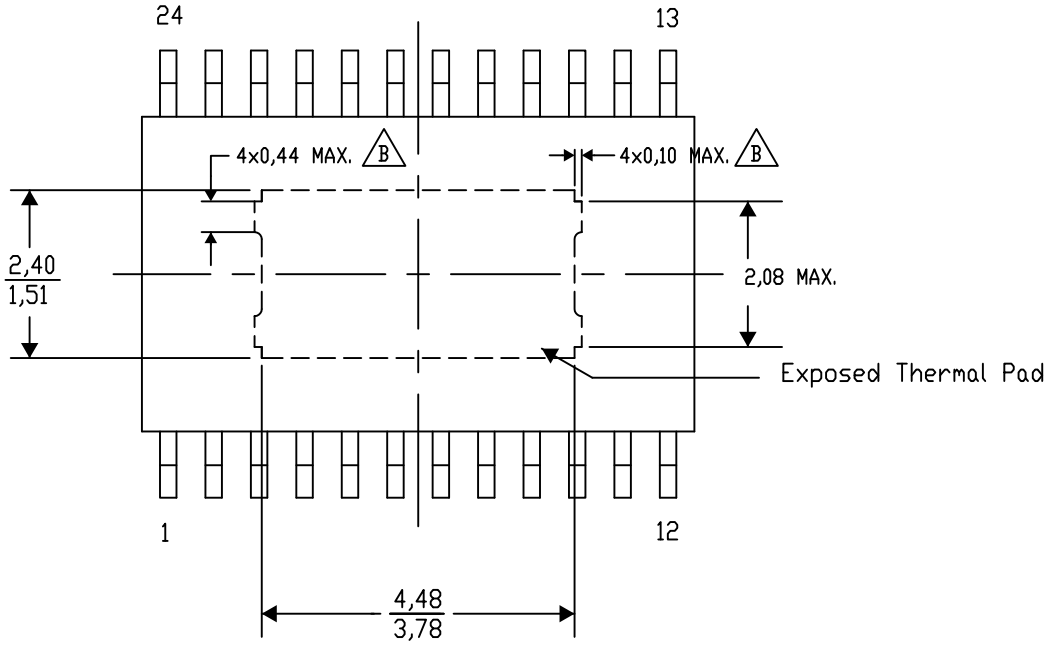
PWP (R–PDSO–G24) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206332–42/AG 08/13

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265