



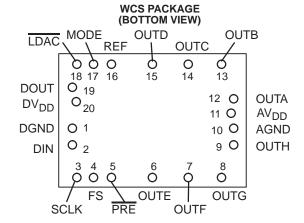
2.7 V TO 5.5 V, 12- AND 10-BIT OCTAL DAC IN WAFER CHIP SCALE PACKAGE

FEATURES

- Eight Voltage Output DACs in One Package
 - TLV5610IYE ... 12-Bit
 - TLV5608IYE ... 10-Bit
- Programmable Settling Time vs Power Consumption
 - 1 μs in Fast Mode
 - $3 \mu s$ in Slow Mode
- Compatible With TMS320[™] DSP Family and SPI Serial Ports
- Monotonic Over Temperature
- Low Power Consumption:
 - 18 mW in Slow Mode at 3 V
 - 48 mW in Fast Mode at 3 V
- Power Down Mode
- Buffered, High Impedance Reference Inputs
- Data Output for Daisy Chainin

APPLICATIONS

- Digital Servo Control Loops
- Digital Offset and Gain Adjustment
- Industrial Process Control
- Machine and Motion Control Devices
- Mass Storage Devices



DESCRIPTION

The TLV5610IYE and TLV5608IYE are pin compatible eight channel 12-/10-bit voltage output DACs each with a flexible serial interface. The serial interface allows glueless interface to TMS320 and SPI, QSPI, and Microwire serial ports. It is programmed with a 16-bit serial string containing 4 control and 12 data bits.

Additional features are a power-down mode, an LDAC input for simultaneous update of all eight DAC outputs, and a data output which can be used to cascade multiple devices.

The resistor string output voltage is buffered by a rail-to-rail output amplifier with a programmable settling time to allow the designer to optimize speed vs power dissipation. The buffered, high-impedance reference input can be connected to the supply voltage.

The TLV5610IYE and TLV5608IYE implemented with a CMOS process and are available in a 20-terminal WCS package. The TLV5610IYE and TLV5608IYE are characterized for operation from -40°C to 85°C in a wire-bonded small outline (SOIC) package.

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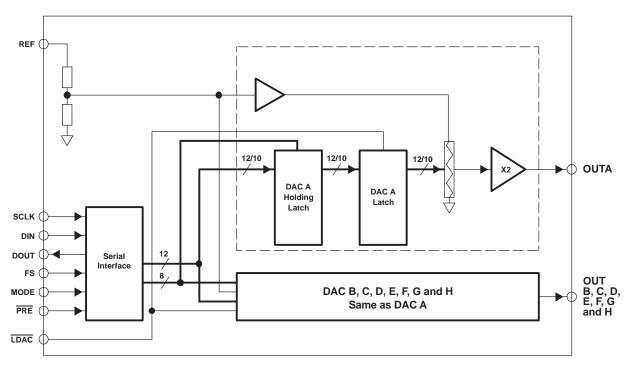
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

AVAILABLE OPTIONS

T _A	PACKAGE
TA	WCS(1) (YE)
−40°C to 85°C	TLV5610IYE
-40°C 10 65°C	TLV5608IYE

⁽¹⁾ Wafer chip scale package. See Figure 13.

FUNCTIONAL BLOCK DIAGRAM



Terminal Functions

TERMIN	AL		DECODINE
NAME	NO.	1/0	DESCRIPTION
AGND	10	Р	Analog ground
AV_{DD}	11	Р	Analog power supply
DGND	1	Р	Digital ground
DIN	2	1	Digital serial data input
DOUT	19	0	Digital serial data output
DV_{DD}	20	Р	Digital power supply
FS	4	I	Frame sync input
LDAC	18	1	Load DAC. The DAC outputs are only updated, if this signal is low. It is an asynchronous input.
MODE	17	I	DSP/ μ C mode pin. High = μ C mode, NC = DSP mode.
PRE	5	I	Preset input
REF	16	I	Voltage reference input
SCLK	3	I	Serial clock input
OUTA-OUTH	12–15, 6–9	0	DAC outputs A, B, C, D, E, F, G and H



TLV5608IYE

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

	UNIT
Supply voltage, (AV _{DD} , DV _{DD} to GND)	7 V
Reference input voltage range	- 0.3 V to AV _{DD} + 0.3
Digital input voltage rang	- 0.3 V to DV _{DD} + 0.3
Operating free-air temperature range, TA	−40°C to 85°C

⁽¹⁾ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIM	TYP	MAX	UNIT
0 1 1 1 1 1 1	5-V operation	4.5	5	5.5	V
Supply voltage, AV _{DD} , AV _{DD}	3-V operation	2.7	3	3.3	V
High level digital input, V _{IH}	DV _{DD} = 2.7 V to 5.5 V	2			V
Low level digital input, V _{IL}	DV _{DD} = 2.7 V to 5.5 V			0.8	V
5.4	AV _{DD} = 5 V	GNE	4.096	AV_{DD}	.,
Reference voltage, V _{ref}	AV _{DD} = 3 V	GNE	2.048	AV_{DD}	V
Load resistance, R _L		2			kΩ
Load capacitance, C _L				100	pF
Clock frequency, f _{CLK}				30	MHz
Operating free-air temperature, T _A		-40)	85	°C

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range unless otherwise noted(1)

POWER	R-SUPPLY								
	PARAMETER		TEST CONDIT	IONS		MIN	TYP	MAX	UNIT
	D	No load,	V _{re}	f = 4.096 V,	Fast		16	21	A
IDD	Power supply current	All inputs = DV _{DD}	or GND	•	Slow		6	8	mA
	Power-down supply current						0.1		μΑ
POR	Power on threshold						2		V
PSRR	Power supply rejection ratio	Full scale, See No	ote 1				-60		dB
STATIC	DAC SPECIFICATIONS								
	5	TLV5610IYE					12		
	Resolution	TLV5608IYE					10		Bits
		TLV5610IYE			0 to 4095		±2	±6	
INL	Integral nonlinearity	TLV5608IYE	$V_{ref} = 2 V, 4 V$	Code 2	0 to 1023		±0.5	±2	LSB
D. II	DW	TLV5610IYE	., ., .,		0 to 4095		±0.5	±1	1.00
DNL	Differential nonlinearity	TLV5608IYE	$V_{ref} = 2 V, 4 V$	Code 2	0 to 1023		±0.1	±1	LSB

DNII	Differential neutineaute.	TLV5610IYE		Code 40 to 4095	±0.5	±1	LCD
DNL	Differential nonlinearity	TLV5608IYE	V _{ref} = 2 V, 4 V	Code 20 to 1023	±0.1	±1	LSB
EZS	Zero scale error (offset error at ze	ro scale)				±30	mV
E _{ZS} TC	Zero scale error temperature coeff	ficient			30		μV/°C
EG	Gain error					±0.6	%Full Scale V
E _G TC	Gain error temperature coefficient				10		ppm/°C
(1) Power	supply rejection ratio at full scale is	measured by varying	AV _{DD} and is given	by:			

 $[\]mathsf{PSRR} = 20 \; \mathsf{log} \; [(\mathsf{E}_{G}(\mathsf{AV}_{DD}\mathsf{max}) - \mathsf{E}_{G}(\mathsf{AV}_{DD}\mathsf{min})) / \mathsf{V}_{DD}\mathsf{max}]$

TLV5610IYE



ELECTRICAL CHARACTERISTICS (CONTINUED)

over operating free-air temperature range unless otherwise noted(1)

OUTP	UT SPECIFICATIONS					_
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VO	Voltage output range	$R_L = 10 \text{ k}\Omega$	0		AV _{DD} -0.4	V
	Output load regulation accuracy	$R_L = 2 \text{ k}\Omega \text{ vs } 10 \text{ k}\Omega$			±0.3	%Full Scale V

REFE	RENCE INPUT						
	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
٧ı	Input voltage range			0		AV_{DD}	V
R _I	Input resistance						kΩ
Ci	Input capacitance				5		pF
	Defences Sensit bear de Olik	V 0.4V - 0.040 V/s - larget scale - 0.000	Fast		2.2		MHz
	Reference input bandwidth	$V_{ref} = 0.4 V_{pp} + 2.048 Vdc$, Input code = 0x800	Slow		1.9		MHz
	Reference feedthrough	V _{ref} = 2 V _{pp} at 1 kHz + 2.048 Vdc (see Note 1)			-84		dB

⁽¹⁾ Reference feedthrough is measured at the DAC output with an input code = 0x000.

DIGITA	L INPUTS						
	PARAMETE	R	TEST CONDITIONS	MIN	TYP	MAX	UNIT
lн	High-level digital input current		$V_I = DV_{DD}$			1	μΑ
IIL	Low-level digital input current		V _I = 0 V	-1			μΑ
Ci	Input capacitance				8		рF

DIGITAL	LOUTPUTS						
	PARAMETE	:R	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Vон	High-level digital output voltage	$R_L = 10 \text{ k}\Omega$		2.6			V
VOL	Low-level digital output voltage	R _L = 10 kΩ				0.4	V
	Output voltage rise time	$R_L = 10 \text{ k}\Omega, C_L = 20 \text{ pF}, Include}$	s propogation delay		7	20	ns

ANALOG OUTPUT DYNAMIC PERFORMANCE									
	PARAMETER	TI	EST CONDITIONS		MIN	TYP	MAX	UNIT	
t _S (FS) Output settling time, full scale		D 4010	0 400 F.O. N. 4	Fast		1	3		
	$R_L = 10 \text{ k}\Omega$, $C_L = 100 \text{ pF}$, See Note 1	Slow		3	7	μs			
				Fast		0.5	1		
ts(CC)	Output settling time, code to code	$R_L = 10 \text{ k}\Omega$	$C_L = 100 \text{ pF}$, See Note 2	Slow		1	2	μs	
0.0	Cl .	D 4010	0 400 F.O. N. A.	Fast	4	10			
SR	Slew rate	R_L = 10 kΩ, C_L = 100 pF, See Note 3	Slow	1	3		V/μs		
	Glitch energy	See Note 4				4		nV-s	
	Channel crosstalk	10 kHz sine, 4 Vpp				-90		dB	

⁽¹⁾Settling time is the time for the output signal to remain within ±0.5 LSB of the final measured value for a digital input code change of 0x80 to 0xFFF and 0xFFF to 0x080 respectively. Assured by design; not tested.

⁽²⁾Settling time is the time for the output signal to remain within ±0.5 LSB of the final measured value for a digital input code change of one count. The max time applies to code changes near zero scale or full scale. Assured by design; not tested.

⁽³⁾Slew rate determines the time it takes for a change of the DAC output from 10% to 90% full scale voltage.

⁽⁴⁾Code transition: TLV5610IYE - 0x7FF to 0x800, TLV5608IYE - 0x7FC to 0x800.



TLV5608IYE

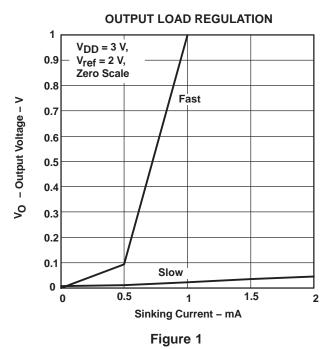
TLV5610IYE

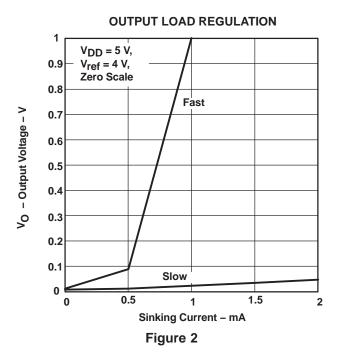
DIGITAL INPUT TIMING REQUIREMENTS

	PARAMETER	MIN	TYP	MAX	UNIT
t _{su(FS-CK)}	Setup time, FS low before first negative SCLK edge	8			ns
tsu(C16-FS)	Setup time, 16^{th} negative edge after FS low on which bit D0 is sampled before rising edge of FS. μ C mode only	10			ns
twL(LDAC)	LDAC duration low	10			ns
t _{wH}	SCLK pulse duration high	16			ns
t_{WL}	SCLK pulse duration low	16			
t _{su(D)}	Setup time, data ready before SCLK falling edge	8			ns
t _{h(D)}	Hold time, data held valid after SCLK falling edge	5			ns
twH(FS)	FS duration high	10			ns
twL(FS)	FS duration low	10			ns
t _S	Settling time	See AC specs			

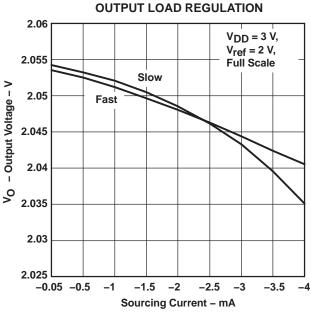


TYPICAL CHARACTERISTICS









OUTPUT LOAD REGULATION 4.12

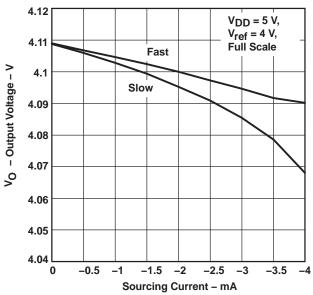
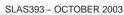


Figure 3 Figure 4

TLV5610IYE







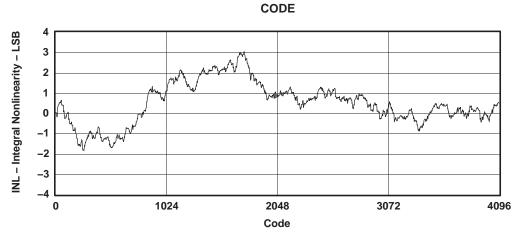


Figure 5

TLV5610IYE DIFFERENTIAL NONLINEARITY

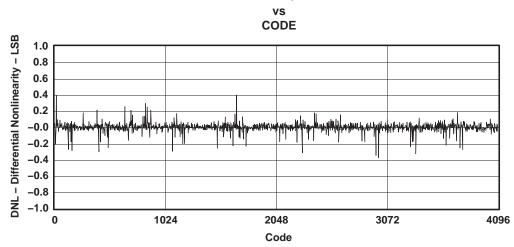


Figure 6



TLV5608IYE INTEGRAL NONLINEARITY

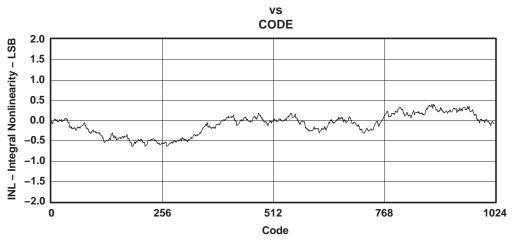


Figure 7

TLV5608IYE DIFFERENTIAL NONLINEARITY

vs CODE

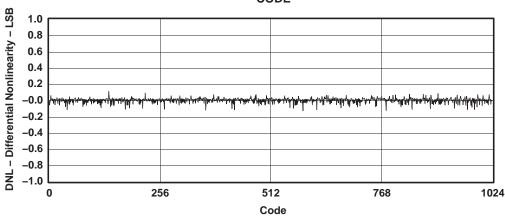


Figure 8

TLV5608IYE



PARAMETER MEASUREMENT INFORMATION

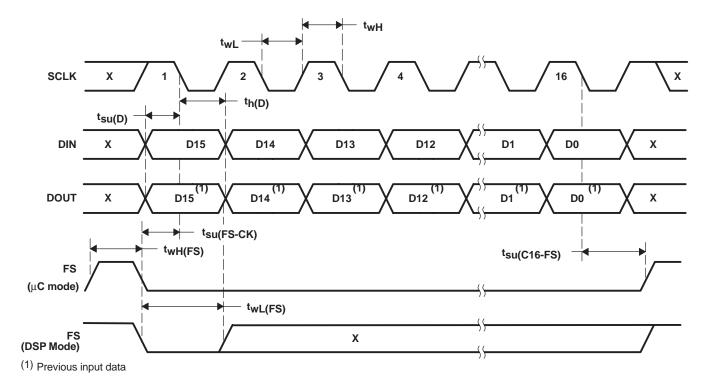


Figure 9. Serial Interface Timing

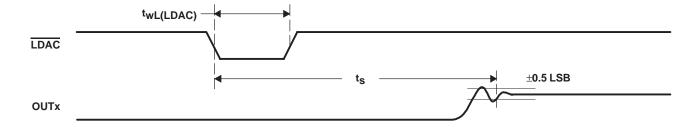


Figure 10. Output Timing



APPLICATION INFORMATION

GENERAL FUNCTION

The TLV5610IYE and TLV5608IYE are 8-channel, 12-bit, single supply DACs, based on a resistor string architecture. They consist of a serial interface, a speed and power-down control logic, a reference input buffer, a resistor string, and a rail-to-rail output buffer.

The output voltage (full scale determined by external reference) for each channel is given by:

REF
$$\frac{\text{CODE}}{0 \times 1000}$$
[V]

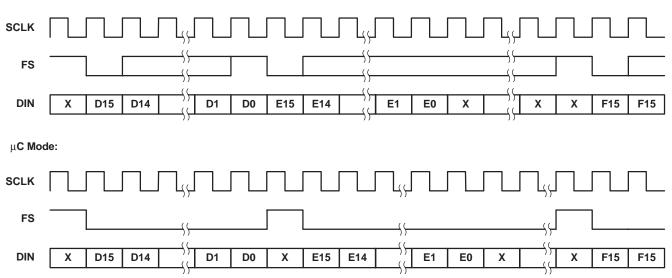
where REF is the reference voltage and CODE is the digital input value. The input range is 0x000 to 0xFFF for the TLV5610IYE and, 0x000 to 0xFFC for the TLV5608IYE. A power on reset initially puts the internal latches to a defined state (all bits zero).

SERIAL INTERFACE

A falling edge of FS starts shifting the data on DIN starting with the MSB to the internal register on the falling edges of SCLK. After 16 bits have been transferred, the content of the shift register is moved to one of the DAC holding registers depending on the address bits within the data word. A logic 0 on the $\overline{\text{LDAC}}$ pin is required to transfer the content of the DAC holding register to the DAC latch and to update the DAC outputs. $\overline{\text{LDAC}}$ is an asynchronous input. It can be held low if a simultaneous update of all eight channels is not needed.

For daisy-chaining, DOUT provides the data sampled on DIN with a delay of 16 clock cycles.





Difference between DSP mode (MODE = N.C. or 0) and μC (MODE = 1) mode:

- In μC mode FS needs to be held low until all 16 data bits have been transferred. If FS is driven high before the 16th falling clock edge the data transfer is cancelled. The DAC is updated after a rising edge on FS.
- In DSP mode FS only needs to stay low for 20 ns and can go high before the 16th falling clock edge.





SERIAL CLOCK FREQUENCY AND UPDATE RATE

The maximum serial clock frequency is given by:

$$f_{sclkmax} = \frac{1}{t_{whmin} + t_{wlmin}} = 30 \text{ MHz}$$

The maximum update rate is:

$$f_{updatemax} = \frac{1}{16 (t_{whmin} + t_{wlmin})} = 1.95 \text{ MHz}$$

Note, that the maximum update rate is just a theoretical value for the serial interface, as the settling time of the DAC has to be considered also.

DATA FORMAT

The 16 bit data word consists of two parts:

• Address bits (D15...D12)

• Data bits (D11...D0)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
A3	A2	A1	A0	Data											

Ax: Address bits. See table.

REGISTER MAP

А3	A2	A1	A0	FUNCTION		
0	0	0	0	DAC A		
0	0	0	1	DAC B		
0	0	1	0	DAC C		
0	0	1	1	DAC D		
0	1	0	0	DAC E		
0	1	0	1	DAC F		
0	1	1	0	DAC G		
0	1	1	1	DAC H		
1	0	0	0	CTRL0		
1	0	0	1	CTRL1		
1	0	1	0	Preset		
1	0	1	1	Reserved		
1	1	0	0	DAC A and B		
1	1	0	1	DAC C and D		
1	1	1	0	DAC E and F		
1	1	1	1	DAC G and H		



DAC A-H AND TWO-CHANNEL REGISTERS

Writing to DAC A-H sets the output voltage of channel A-H. It is possible to automatically generate the complement of one channel by writing to one of the four two-channel registers (DAC A and \overline{B} etc.).

The TLV5610IYE decodes all 12 data bits. The TLV5608IYE decodes D11 to D2 (D1 and D0 are ignored).

PRESET

The outputs of all DAC channels can be driven to a predefined value stored in the preset register by driving the PRE input low. The PRE input is asynchronous to the clock.

CTRL0

	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ſ	Χ	Х	Х	Х	Х	Х	Х	PD	DO	Х	Х	IM

PD : Full device power down 0 = normal 1 = power down DO : Digital output enable 0 = disable 1 = enable

IM : Input mode 0 = straight binary 1 = twos complement

X : Reserved

If DOUT is enabled, the data input on DIN is output on DOUT with a 16 cycle delay. That makes it possible to daisy-chain multiple DACs on one serial bus.

CTRL1

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	PGH	PEF	PCD	P _{AB}	S _{GH}	SEF	S _{CD}	S _{AB}

 P_{XY} : Power Down DAC_{XY} 0 = normal 1 = power down

 S_{XY} : Speed DAC_{XY} 0 = slow 1 = fast

XY: DAC pair AB, CD, EF or GH

In power-down mode, the amplifiers of the selected DAC pair within the device are disabled and the total power consumption of the device is significantly reduced. Power-down mode of a specific DAC pair can be selected by setting the PXY bit within the data word to 1.

There are two settling time modes: fast and slow. Fast mode of a DAC pair is selected by setting S_{XY} to 1 and slow mode is selected by setting S_{XY} to 0.



USING TLV5610IYE AND TLV5608IYE, WAFER CHIP SCALE PACKAGE (WCS)

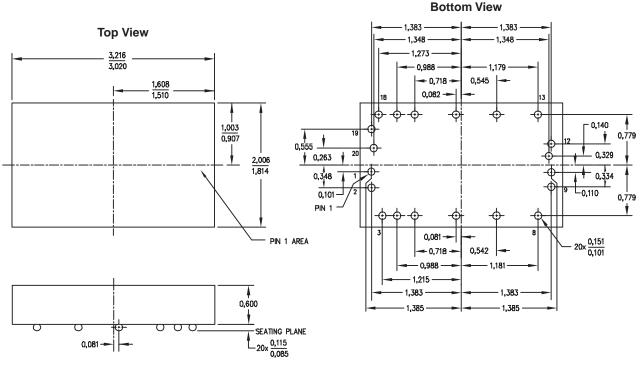
- TLV5610 and TLV5608 qualifications were done using a wire-bonded small outline (SOIC) package and includes: steady state life, thermal shock, ESD, latch-up, biased HAST, autoclave, and characterization. These qualified devices are orderable as TLV5610IDW and TLV5608IDW.
- The wafer chip-scale package (WCS), TLV5610IYE and TLV5608IYE, uses the same DIE as TLV5610IDW and TLV5608IDW respectively, but are not qualified. WCS qualification, including board level reliability (BLR), is the responsibility of the customer.
- It is recommended that underfill be used for increased reliability. BLR is application dependent, but may include test such as: temperature cycling, drop test, key push, bend, vibration, and package shear.

The following WCSP information provides the user of the TLV5610IYE and TLV5608IYE with some general guidelines for board assembly.

- Melting point of eutectic solder is 183°C.
- Recommended peak reflow temperatures are in the 220°C to 230°C range.
- The use of underfill is required. The use of underfill greatly reduces the risk of thermal mismatch fails.

Underfill is an epoxy/adhesive that may be added during the board assembly process to improve board level/system level reliability. The process is to dispense the epoxy under the dice after die attach reflow. The epoxy adheres to the body of the device and to the printed-circuit board. It reduces stress placed upon the solder joints due to the thermal coefficient of expansion (TCE) mismatch between the board and the component. Underfill material is highly filled with silica or other fillers to increase an epoxy's modulus, reduce creep sensitivity, and decrease the material's TCE.

The recommendation for peak flow temperatures of 220°C to 230°C is based on general empirical results that indicate that this temperature range is needed to facilitate good wetting of the solder bump to the substrate or circuit board pad. Lower peak temperatures may cause nonwets (cold solder joints).



NOTES:A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

Figure 11. TLV5610IYE and TLV5608IYE Wafer Chip Scale Package



PACKAGE OPTION ADDENDUM

28-Aug-2010

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
TLV5608IYER	OBSOLETE	DIESALE	YE	20		TBD	Call TI	Call TI	Samples Not Available
TLV5610IYE	ACTIVE	DIESALE	YE	20	150	TBD	Call TI	N / A for Pkg Type	Request Free Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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