

## AUTOMOTIVE LOW-DROPOUT VOLTAGE REGULATORS

Check for Samples: [TL750Mxx-Q1](#), [TL751Mxx-Q1](#)

### FEATURES

- **Qualified for Automotive Applications**
- **Low Dropout Voltage, Less Than 0.6 V at 750 mA**
- **Low Quiescent Current**
- **TTL- and CMOS-Compatible Enable on TL751M Series**
- **Load-Dump Protection**
- **Overvoltage Protection**
- **Internal Thermal Overload Protection**
- **Internal Overcurrent-Limiting Circuitry**

### DESCRIPTION

The TL750M and TL751M series are low-dropout positive voltage regulators specifically designed for automotive applications. The TL750M and TL751M series incorporate onboard overvoltage and current-limiting protection circuitry to protect the devices and the regulated system. Both series are fully protected against load-dump and reverse-battery conditions. Load-dump protection is up to a maximum of 60 V at the input of the device. Low quiescent current, even during full-load conditions, makes the TL750M and TL751M series ideal for use in applications that are permanently connected to the vehicle battery.

The TL750M and TL751M series offers 5-V, 8-V, and 12-V options. The TL751M series has the addition of an enable (ENABLE) input. The ENABLE input gives complete control over power up, allowing sequential power up or shutdown. When ENABLE is high, the regulator output is placed in the high-impedance state. The ENABLE input is TTL and CMOS compatible.

The TL750Mxx and TL751Mxx are characterized for operation over the virtual junction temperature range –40°C to 125°C.

### AVAILABLE OPTIONS<sup>(1)</sup>

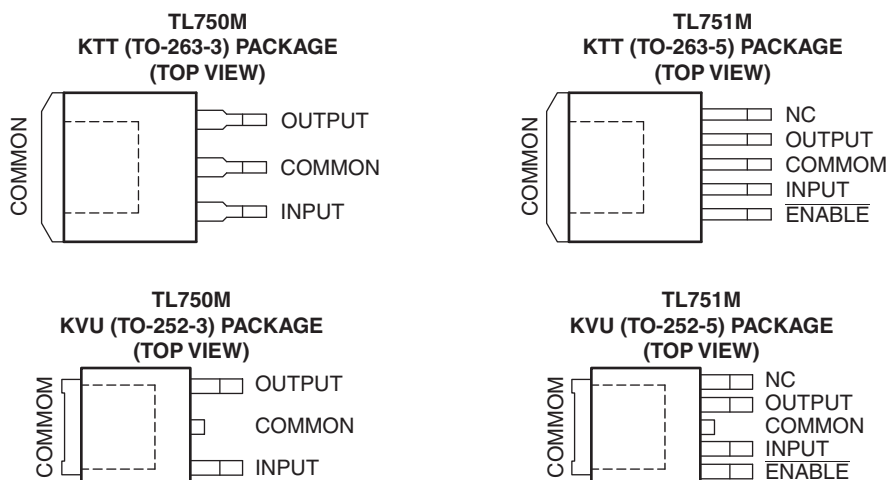
T <sub>J</sub>	V <sub>O</sub> NOM (V)	PACKAGE <sup>(2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	5 V	TO-263-3 – KTT	Reel of 500	TL750M05QKTTRQ1	TL750M05Q1
		TO-252-3 – KVV	Reel of 2500	TL750M05QKVURQ1	750M05Q
	8 V	TO-263-3 – KTT	Reel of 500	TL750M08QKTTRQ1	TL750M08Q1
		TO-252-3 – KVV	Reel of 2500	TL750M08QKVURQ1	750M08Q
	12 V	TO-263-3 – KTT	Reel of 500	TL750M12QKTTRQ1	TL750M12Q1
		TO-252-3 – KVV	Reel of 2500	TL750M12QKVURQ1	750M12Q
	5 V	TO-263-5 – KTT	Reel of 500	TL751M05QKTTRQ1	TL751M05Q1
		TO-252-5 – KVV	Reel of 2500	TL751M05QKVURQ1	751M05Q
	8 V	TO-263-5 – KTT	Reel of 500	TL751M08QKTTRQ1	TL751M08Q1
		TO-252-5 – KVV	Reel of 2500	TL751M08QKVURQ1	751M08Q
	12 V	TO-263-5 – KTT	Reel of 500	TL751M12QKTTRQ1	TL751M12Q1
		TO-252-5 – KVV	Reel of 2500	TL751M12QKVURQ1	751M12Q

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

(2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

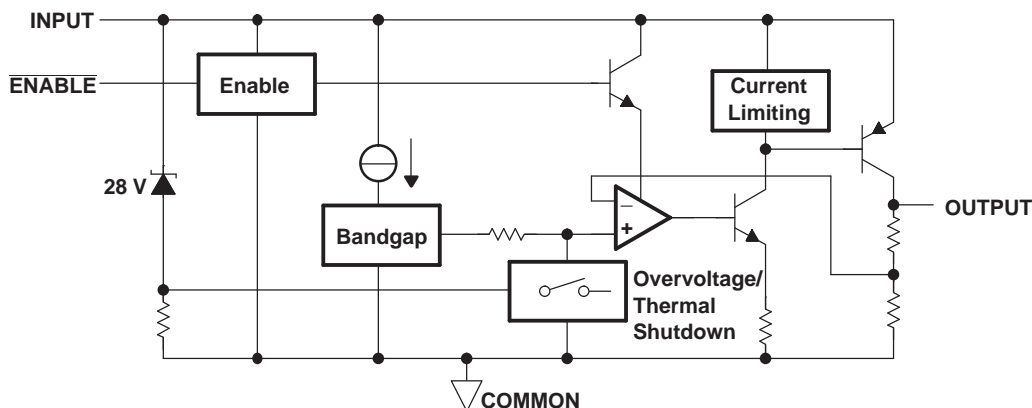


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



NOTE: The COMMON terminal is in electrical contact with the mounting base.  
NC – No internal connection

## TL751Mxx FUNCTIONAL BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

Continuous input voltage		26 V	
Transient input voltage (see <a href="#">Figure 4</a> )		60 V	
Continuous reverse input voltage		–15 V	
Transient reverse input voltage		t = 100 ms –50 V	
$\theta_{JA}$	Package thermal impedance <sup>(2) (3)</sup>	KTT package (3 pin)	26.9°C/W
		KTT package (5 pin)	26.5°C/W
		KVU package	38.6°C/W
T <sub>J</sub>	Virtual junction temperature range		–40°C to 150°C
T <sub>stg</sub>	Storage temperature range		–65°C to 150°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Maximum power dissipation is a function of  $T_J(\text{max})$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(\text{max}) - T_A)/\theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can impact reliability. Due to variation in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.
- (3) The package thermal impedance is calculated in accordance with JESD 51.

## THERMAL INFORMATION

THERMAL METRIC <sup>(1)</sup>		TL750M05	UNITS
		KTT	
		3 PINS	
$\theta_{JA}$	Junction-to-ambient thermal resistance <sup>(2)</sup>	27.5	°C/W
$\theta_{JCTop}$	Junction-to-case (top) thermal resistance <sup>(3)</sup>	43.2	
$\theta_{JB}$	Junction-to-board thermal resistance <sup>(4)</sup>	17.3	
$\Psi_{JT}$	Junction-to-top characterization parameter <sup>(5)</sup>	2.8	
$\Psi_{JB}$	Junction-to-board characterization parameter <sup>(6)</sup>	9.3	
$\theta_{JCbott}$	Junction-to-case (bottom) thermal resistance <sup>(7)</sup>	0.3	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (5) The junction-to-top characterization parameter,  $\Psi_{JT}$ , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining  $\theta_{JA}$ , using a procedure described in JESD51-2a (sections 6 and 7).
- (6) The junction-to-board characterization parameter,  $\Psi_{JB}$ , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining  $\theta_{JA}$ , using a procedure described in JESD51-2a (sections 6 and 7).
- (7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

## RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
$V_I$	Input voltage	TL75xM05	6	26
		TL75xM08	9	26
		TL75xM12	13	26
$V_{IH}$	High-level $\overline{\text{ENABLE}}$ input voltage	TL751Mxx	2	15
$V_{IL}$	Low-level $\overline{\text{ENABLE}}$ input voltage	TL751Mxx	0	0.8
$I_O$	Output current	TL75xMxx	750	mA
$T_J$	Operating virtual junction temperature	TL75xMxx	–40	125

## TL751Mxx ELECTRICAL CHARACTERISTICS

$V_I = 14\text{ V}$ ,  $I_O = 300\text{ mA}$ ,  $T_J = 25^\circ\text{C}$

PARAMETER	TL751Mxx	UNIT
	TYP	
Response time, $\overline{\text{ENABLE}}$ to output (start-up)	50	$\mu\text{s}$

## TL750M05/TL751M05 ELECTRICAL CHARACTERISTICS

$V_I = 14\text{ V}$ ,  $I_O = 300\text{ mA}$ ,  $\overline{\text{ENABLE}}$  at 0 V for TL751M05,  $T_J = -40^\circ\text{C}$  to  $125^\circ\text{C}$  (unless otherwise noted)<sup>(1)</sup>

PARAMETER	TEST CONDITIONS	TL750M05 TL751M05			UNIT
		MIN	TYP	MAX	
Output voltage	$V_I = 6\text{ V}$ to $26\text{ V}$	4.85	5	5.15	V
Line regulation	$V_I = 9\text{ V}$ to $16\text{ V}$ , $I_O = 250\text{ mA}$		10	25	mV
	$V_I = 6\text{ V}$ to $26\text{ V}$ , $I_O = 250\text{ mA}$		12	50	
Power-supply ripple rejection	$V_I = 8\text{ V}$ to $18\text{ V}$ , $f = 120\text{ Hz}$		55		dB
Load regulation	$I_O = 5\text{ mA}$ to $750\text{ mA}$		20	50	mV
Dropout voltage <sup>(2)</sup>	$I_O = 500\text{ mA}$ , $T_J = 25^\circ\text{C}$			0.5	V
	$I_O = 750\text{ mA}$ , $T_J = 25^\circ\text{C}$			0.65	
Current consumption $I_q = I_I - I_O$	$I_O = 750\text{ mA}$		60	75	mA
	$I_O = 10\text{ mA}$			5	
Shutdown current (TL751M05 only)	$\overline{\text{ENABLE}}$ $V_{IH} \geq 2\text{ V}$			200	$\mu\text{A}$

(1) Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1- $\mu\text{F}$  capacitor across the input and a 10- $\mu\text{F}$  tantalum capacitor on the output, with equivalent series resistance within the guidelines shown in [Figure 4](#).

(2) Measured when the output voltage,  $V_O$ , has dropped 100 mV from the nominal value obtained at  $V_I = 14\text{ V}$ .

## TL750M08/TL751M08 ELECTRICAL CHARACTERISTICS

$V_I = 14\text{ V}$ ,  $I_O = 300\text{ mA}$ ,  $\overline{\text{ENABLE}}$  at 0 V for TL751M08,  $T_J = -40^\circ\text{C}$  to  $125^\circ\text{C}$  (unless otherwise noted)<sup>(1)</sup>

PARAMETER	TEST CONDITIONS	TL750M08 TL751M08			UNIT
		MIN	TYP	MAX	
Output voltage	$V_I = 6\text{ V}$ to $26\text{ V}$	7.76	8	8.24	V
Line regulation	$V_I = 10\text{ V}$ to $17\text{ V}$ , $I_O = 250\text{ mA}$		12	40	mV
	$V_I = 9\text{ V}$ to $26\text{ V}$ , $I_O = 250\text{ mA}$		15	68	
Power-supply ripple rejection	$V_I = 11\text{ V}$ to $21\text{ V}$ , $f = 120\text{ Hz}$		55		dB
Load regulation	$I_O = 5\text{ mA}$ to $750\text{ mA}$		24	80	mV
Dropout voltage <sup>(2)</sup>	$I_O = 500\text{ mA}$ , $T_J = 25^\circ\text{C}$			0.5	V
	$I_O = 750\text{ mA}$ , $T_J = 25^\circ\text{C}$			0.65	
Current consumption $I_q = I_I - I_O$	$I_O = 750\text{ mA}$ , $T_J = 25^\circ\text{C}$		60	75	mA
	$I_O = 10\text{ mA}$			5	
Shutdown current (TL751M08 only)	$\overline{\text{ENABLE}}$ $V_{IH} \geq 2\text{ V}$			200	$\mu\text{A}$

(1) Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1- $\mu\text{F}$  capacitor across the input and a 10- $\mu\text{F}$  tantalum capacitor on the output, with equivalent series resistance within the guidelines shown in [Figure 4](#).

(2) Measured when the output voltage,  $V_O$ , has dropped 100 mV from the nominal value obtained at  $V_I = 14\text{ V}$ .

**TL750M12/TL751M12 ELECTRICAL CHARACTERISTICS**
 $V_I = 14\text{ V}$ ,  $I_O = 300\text{ mA}$ ,  $\overline{\text{ENABLE}}$  at 0 V for TL751M12,  $T_J = -40^\circ\text{C}$  to  $125^\circ\text{C}$  (unless otherwise noted)<sup>(1)</sup>

PARAMETER	TEST CONDITIONS	TL750M12 TL751M12			UNIT
		MIN	TYP	MAX	
Output voltage	$V_I = 13\text{ V to }26\text{ V}$	11.76	12	12.24	V
Line regulation	$V_I = 14\text{ V to }19\text{ V}$ , $I_O = 250\text{ mA}$		15	43	mV
	$V_I = 13\text{ V to }26\text{ V}$ , $I_O = 250\text{ mA}$		20	78	
Power-supply ripple rejection	$V_I = 13\text{ V to }23\text{ V}$ , $f = 120\text{ Hz}$	50	55		dB
Load regulation	$I_O = 5\text{ mA to }750\text{ mA}$		30	120	mV
Dropout voltage <sup>(2)</sup>	$I_O = 500\text{ mA}$ , $T_J = 25^\circ\text{C}$			0.5	V
	$I_O = 750\text{ mA}$ , $T_J = 25^\circ\text{C}$			0.6	
Current consumption $I_q = I_I - I_O$	$I_O = 750\text{ mA}$ , $T_J = 25^\circ\text{C}$		60	75	mA
	$I_O = 10\text{ mA}$			5	
Shutdown current (TL751M12 only)	$\overline{\text{ENABLE}}$ $V_{IH} \geq 2\text{ V}$			200	$\mu\text{A}$

- (1) Pulse-testing techniques maintain the junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1- $\mu\text{F}$  capacitor across the input and a 10- $\mu\text{F}$  tantalum capacitor on the output, with equivalent series resistance within the guidelines shown in [Figure 4](#).
- (2) Measured when the output voltage,  $V_O$ , has dropped 100 mV from the nominal value obtained at  $V_I = 14\text{ V}$ .

## PARAMETER MEASUREMENT INFORMATION

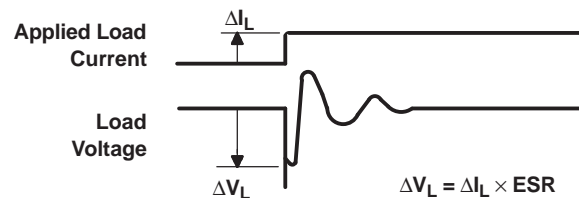
The TL750Mxx and TL751Mxx are low-dropout regulators. The output capacitor value and the parasitic equivalent series resistance (ESR) affect the bandwidth and stability of the control loop for these devices. For this reason, the capacitor and ESR must be carefully selected for a given operating temperature and load range. [Figure 2](#) and [Figure 3](#) can be used to establish the appropriate capacitance value and ESR for the best regulator transient response.

[Figure 2](#) shows the recommended range of ESR for a given load with a 10- $\mu\text{F}$  capacitor on the output. [Figure 2](#) also shows a maximum ESR limit of 2  $\Omega$  and a load-dependent minimum ESR limit.

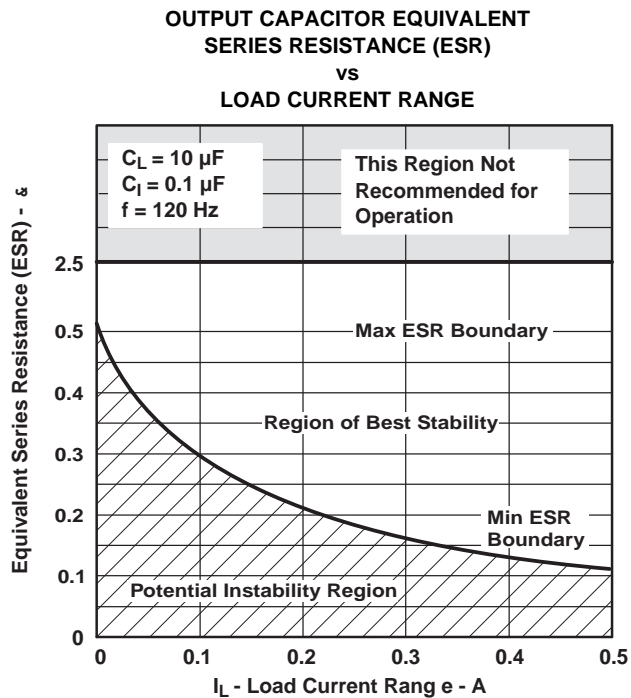
For applications with varying loads, the lightest load condition should be chosen because it is the worst case. [Figure 3](#) shows the relationship of the reciprocal of ESR to the square root of the capacitance, with a minimum capacitance limit of 10  $\mu\text{F}$  and a maximum ESR limit of 2  $\Omega$ . This figure establishes the amount that the minimum ESR limit shown in [Figure 2](#) can be adjusted for different capacitor values. For example, where the minimum load needed is 200 mA, [Figure 2](#) suggests an ESR range of 0.8  $\Omega$  to 2  $\Omega$  for 10  $\mu\text{F}$ . [Figure 3](#) shows that changing the capacitor from 10  $\mu\text{F}$  to 400  $\mu\text{F}$  can change the ESR minimum by greater than 3/0.5 (or 6). Therefore, the new minimum ESR value is 0.8/6 (or 0.13  $\Omega$ ). This allows an ESR range of 0.13  $\Omega$  to 2  $\Omega$ , achieving an expanded ESR range by using a larger capacitor at the output. For better stability in low-current applications, a small resistance placed in series with the capacitor (see [Table 1](#)) is recommended, so that ESRs better approximate those shown in [Figure 2](#) and [Figure 3](#).

**Table 1. Compensation for Increased Stability at Low Currents**

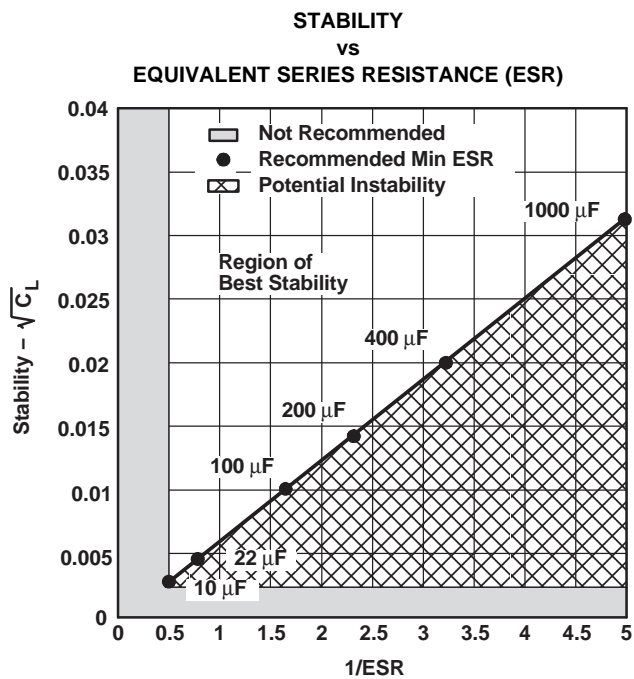
MANUFACTURER	CAPACITANCE	ESR TYP	PART NUMBER	ADDITIONAL RESISTANCE
AVX	15 $\mu\text{F}$	0.9 $\Omega$	TAJB156M010S	1 $\Omega$
KEMET	33 $\mu\text{F}$	0.6 $\Omega$	T491D336M010AS	0.5 $\Omega$



**Figure 1.**



**Figure 2.**

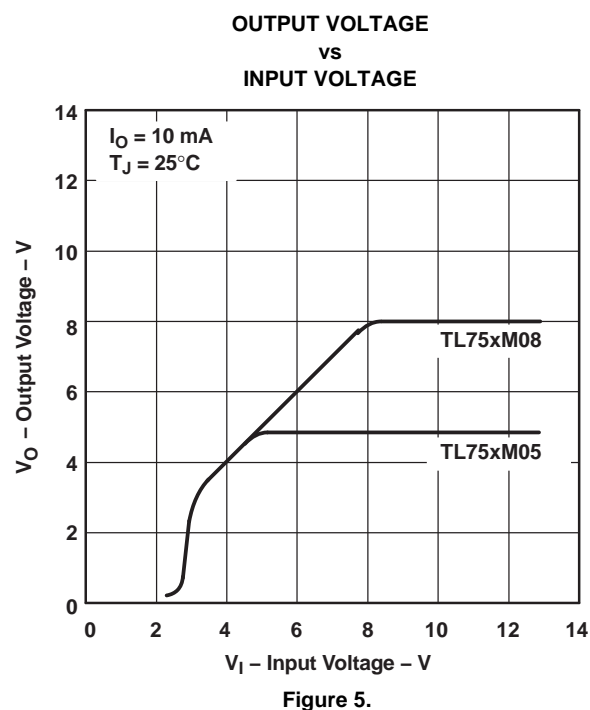
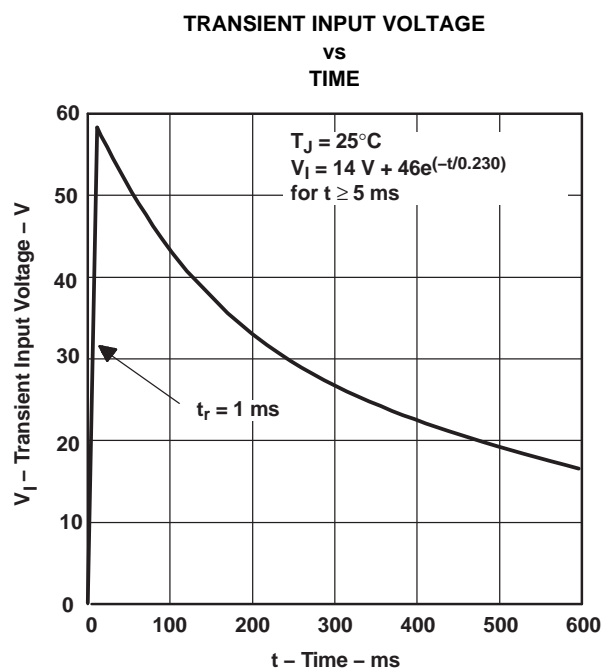


**Figure 3.**

## TYPICAL CHARACTERISTICS

Table 2. Table of Graphs

			FIGURE
Transient input voltage	vs Time		4
Output voltage	vs Input voltage		5
Input current	vs Input voltage	I <sub>O</sub> = 10 mA	6
		I <sub>O</sub> = 100 mA	7
Dropout voltage	vs Output current		8
Quiescent current	vs Output current		9
Load transient response			10
Line transient response			11





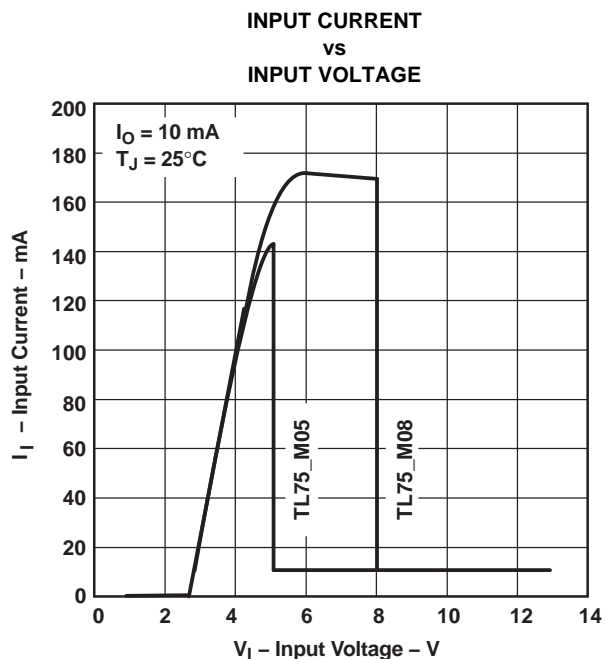


Figure 6.

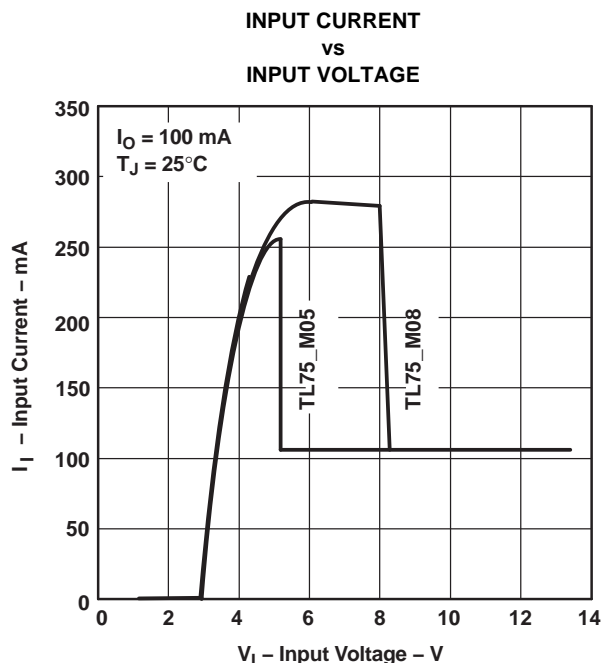


Figure 7.

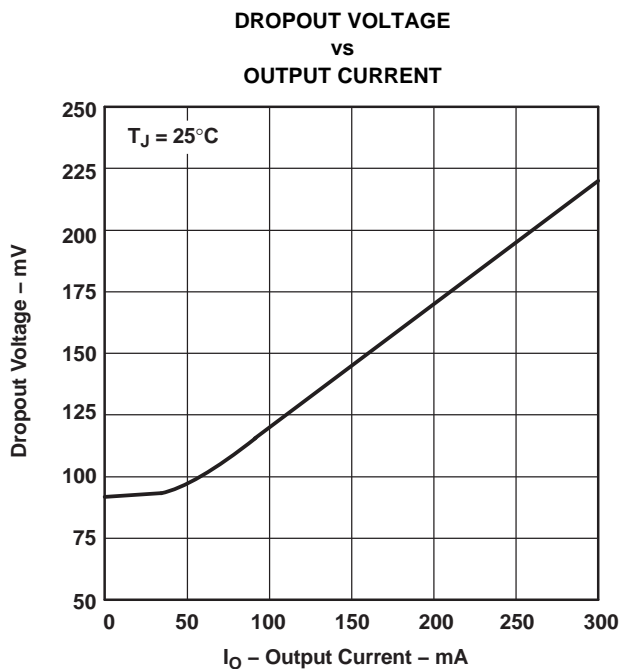


Figure 8.

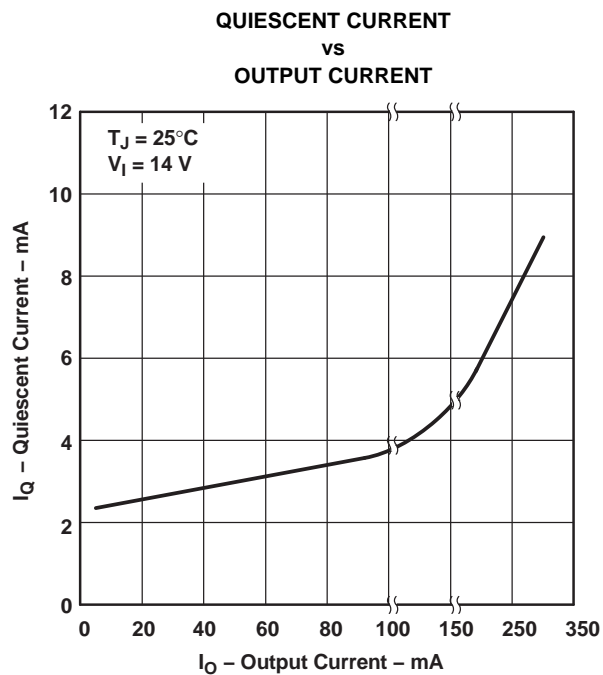


Figure 9.

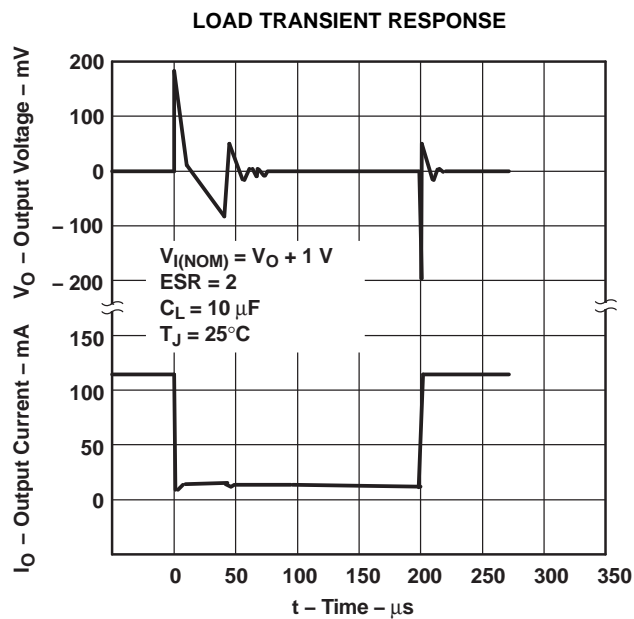


Figure 10.

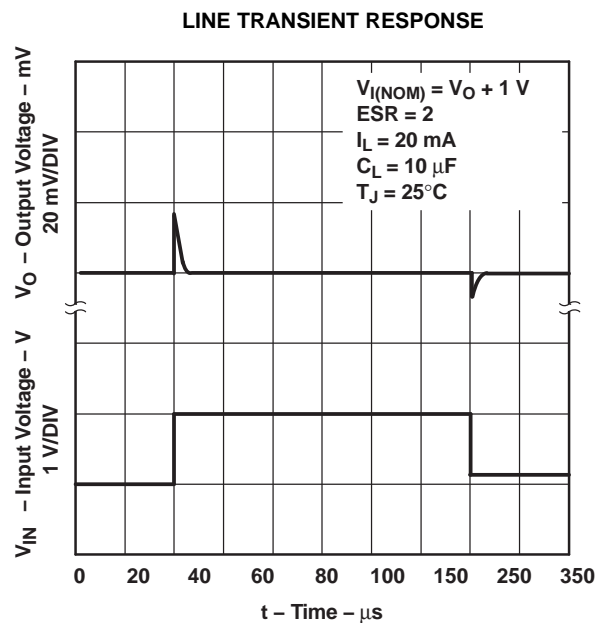


Figure 11.

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL750M05QKTTRQ1	ACTIVE	DDPAK/ TO-263	KTT	3	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	-40 to 125	TL750M05Q1	<a href="#">Samples</a>
TL750M05QKVURQ1	ACTIVE	TO-252	KVU	3	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	750M05Q	<a href="#">Samples</a>
TL750M08QKVURQ1	ACTIVE	TO-252	KVU	3	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	750M08Q	<a href="#">Samples</a>
TL750M12QKTTRQ1	ACTIVE	DDPAK/ TO-263	KTT	3	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	-40 to 125	TL750M12Q1	<a href="#">Samples</a>
TL750M12QKVURQ1	ACTIVE	TO-252	KVU	3	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	750M12Q	<a href="#">Samples</a>
TL751M05QKTTRQ1	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	-40 to 125	TL751M05Q1	<a href="#">Samples</a>
TL751M05QKVURQ1	ACTIVE	TO-252	KVU	5	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	751M05Q	<a href="#">Samples</a>
TL751M08QKTTRQ1	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	-40 to 125	TL751M08Q1	<a href="#">Samples</a>
TL751M08QKVURQ1	ACTIVE	TO-252	KVU	5	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	751M08Q	<a href="#">Samples</a>
TL751M12QKTTRQ1	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR	-40 to 125	TL751M12Q1	<a href="#">Samples</a>
TL751M12QKVURQ1	ACTIVE	TO-252	KVU	5	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	751M12Q	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TL750M05-Q1, TL750M08-Q1, TL750M12-Q1, TL751M05-Q1 :**

- Catalog: [TL750M05](#), [TL750M08](#), [TL750M12](#), [TL751M05](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL750M05QKVURQ1	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TL750M08QKVURQ1	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TL750M12QKTTRQ1	DDPAK/ TO-263	KTU	3	500	330.0	24.4	10.6	15.8	4.9	16.0	24.0	Q2
TL750M12QKVURQ1	TO-252	KVU	3	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TL751M05QKVURQ1	TO-252	KVU	5	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TL751M08QKTTRQ1	DDPAK/ TO-263	KTU	5	500	330.0	24.4	10.6	15.8	4.9	16.0	24.0	Q2
TL751M08QKVURQ1	TO-252	KVU	5	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2
TL751M12QKTTRQ1	DDPAK/ TO-263	KTU	5	500	330.0	24.4	10.6	15.8	4.9	16.0	24.0	Q2
TL751M12QKVURQ1	TO-252	KVU	5	2500	330.0	16.4	6.9	10.5	2.7	8.0	16.0	Q2

## TAPE AND REEL BOX DIMENSIONS

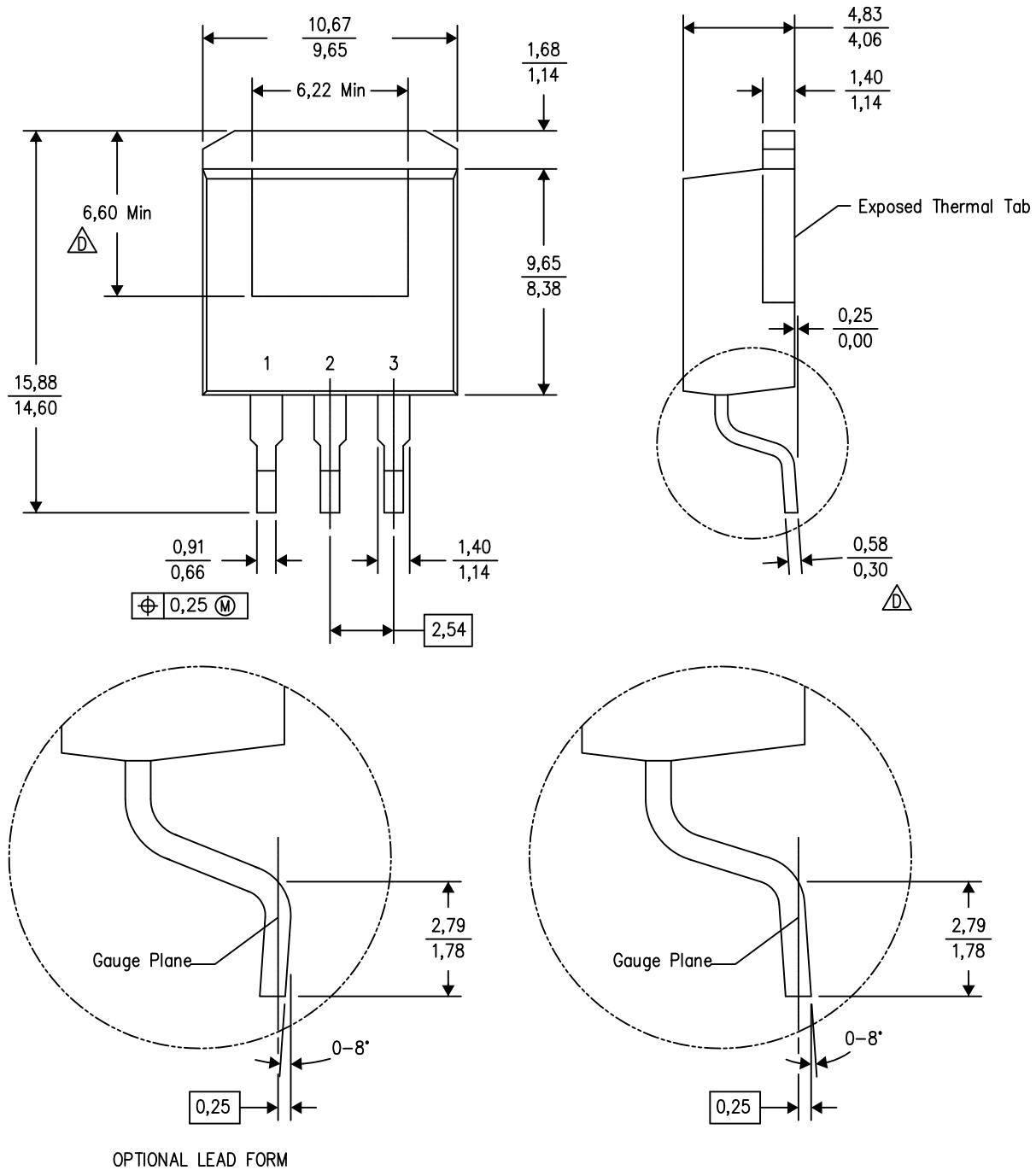


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL750M05QKVURQ1	TO-252	KVU	3	2500	340.0	340.0	38.0
TL750M08QKVURQ1	TO-252	KVU	3	2500	340.0	340.0	38.0
TL750M12QKTTRQ1	DDPAK/TO-263	KTT	3	500	340.0	340.0	38.0
TL750M12QKVURQ1	TO-252	KVU	3	2500	340.0	340.0	38.0
TL751M05QKVURQ1	TO-252	KVU	5	2500	340.0	340.0	38.0
TL751M08QKTTRQ1	DDPAK/TO-263	KTT	5	500	340.0	340.0	38.0
TL751M08QKVURQ1	TO-252	KVU	5	2500	340.0	340.0	38.0
TL751M12QKTTRQ1	DDPAK/TO-263	KTT	5	500	340.0	340.0	38.0
TL751M12QKVURQ1	TO-252	KVU	5	2500	340.0	340.0	38.0

KTT (R-PSFM-G3)

PLASTIC FLANGE-MOUNT PACKAGE

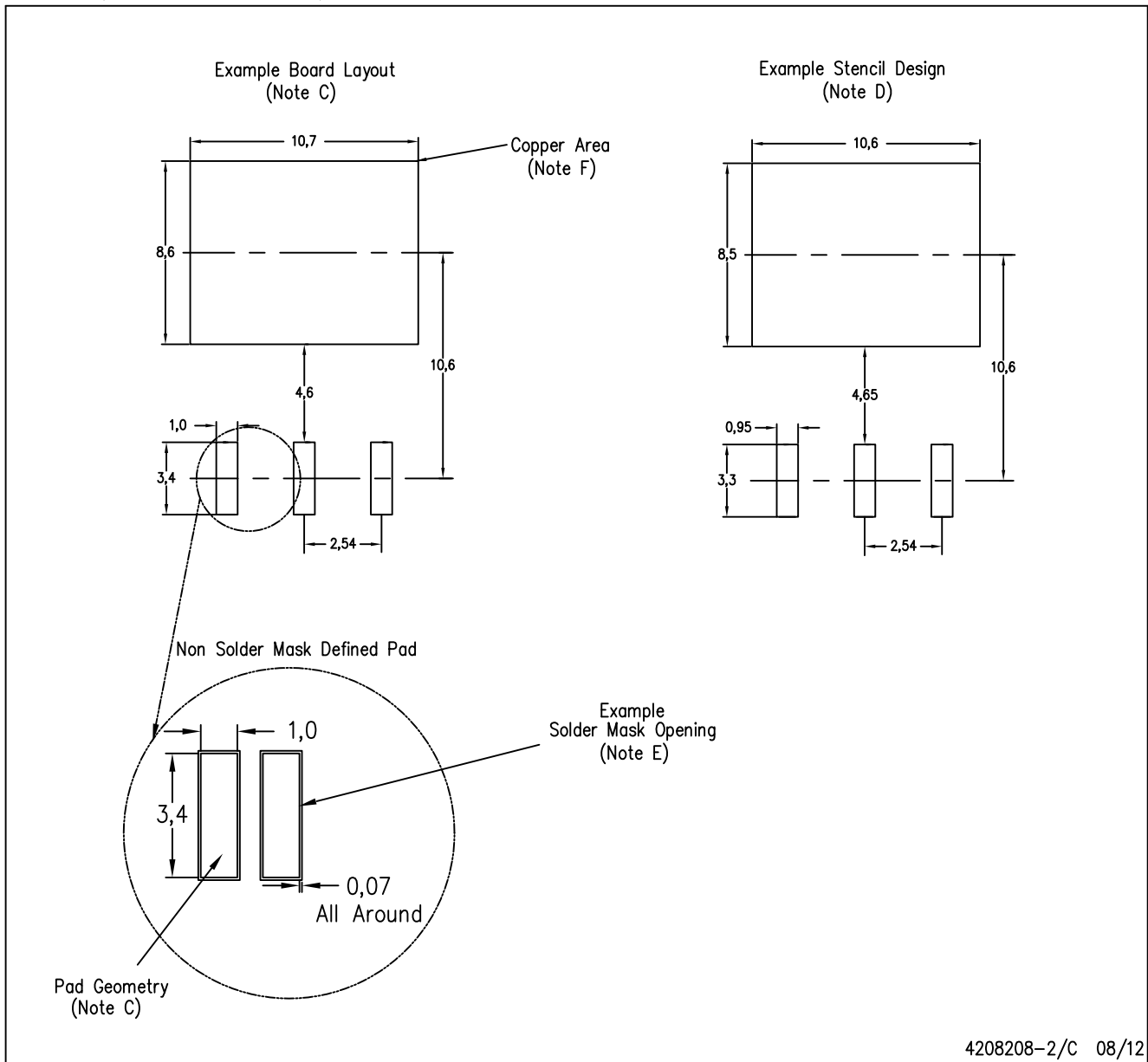


4200577-3/G 01/13

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
  - $\Delta$  Falls within JEDEC TO-263 variation AA, except minimum lead thickness and minimum exposed pad length.

KTT (R-PSFM-G3)

PLASTIC FLANGE-MOUNT PACKAGE

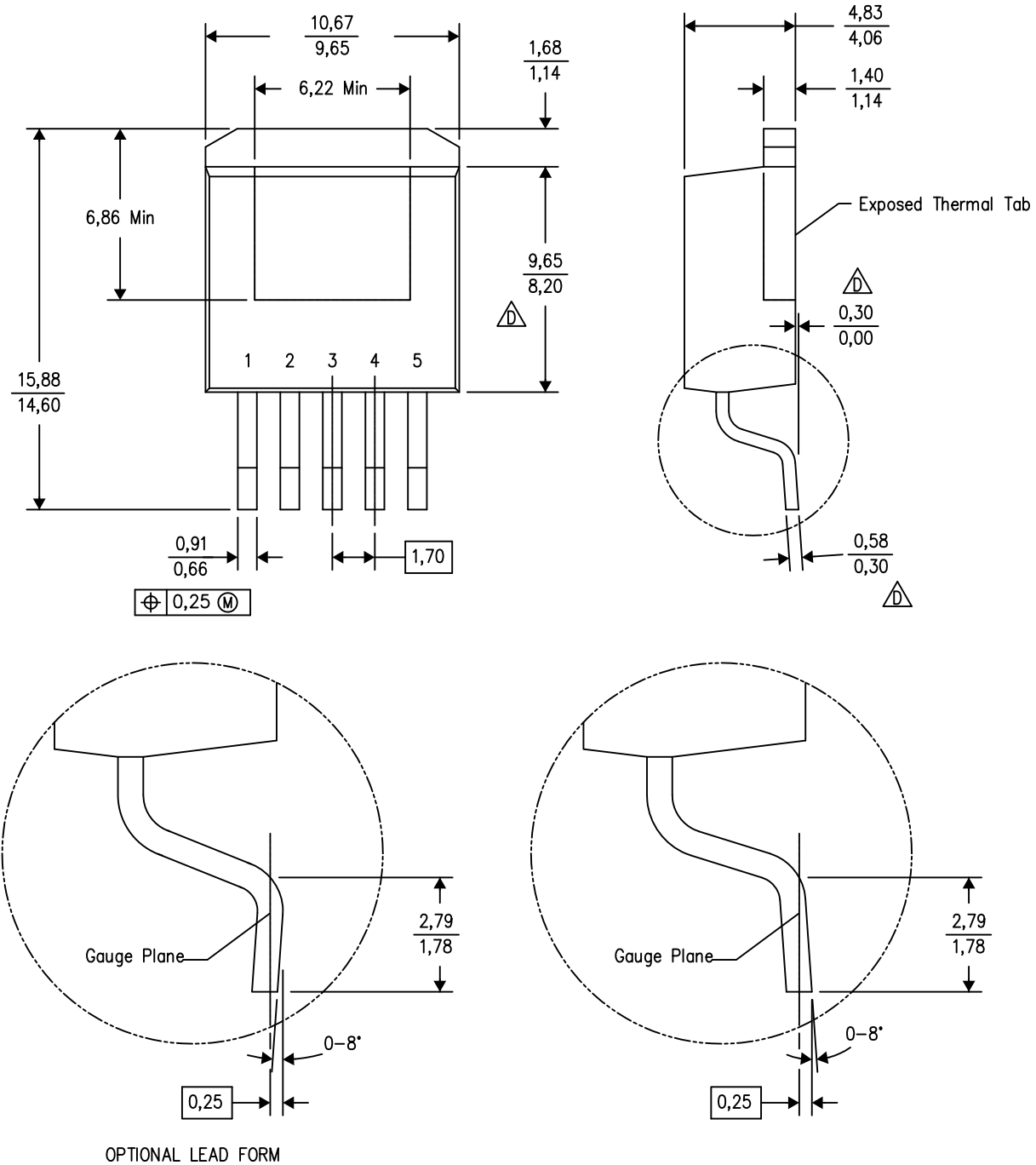


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-SM-782 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
  - F. This package is designed to be soldered to a thermal pad on the board. Refer to the Product Datasheet for specific thermal information, via requirements, and recommended thermal pad size. For thermal pad sizes larger than shown a solder mask defined pad is recommended in order to maintain the solderable pad geometry while increasing copper area.



KTT (R-PSFM-G5)

PLASTIC FLANGE-MOUNT PACKAGE

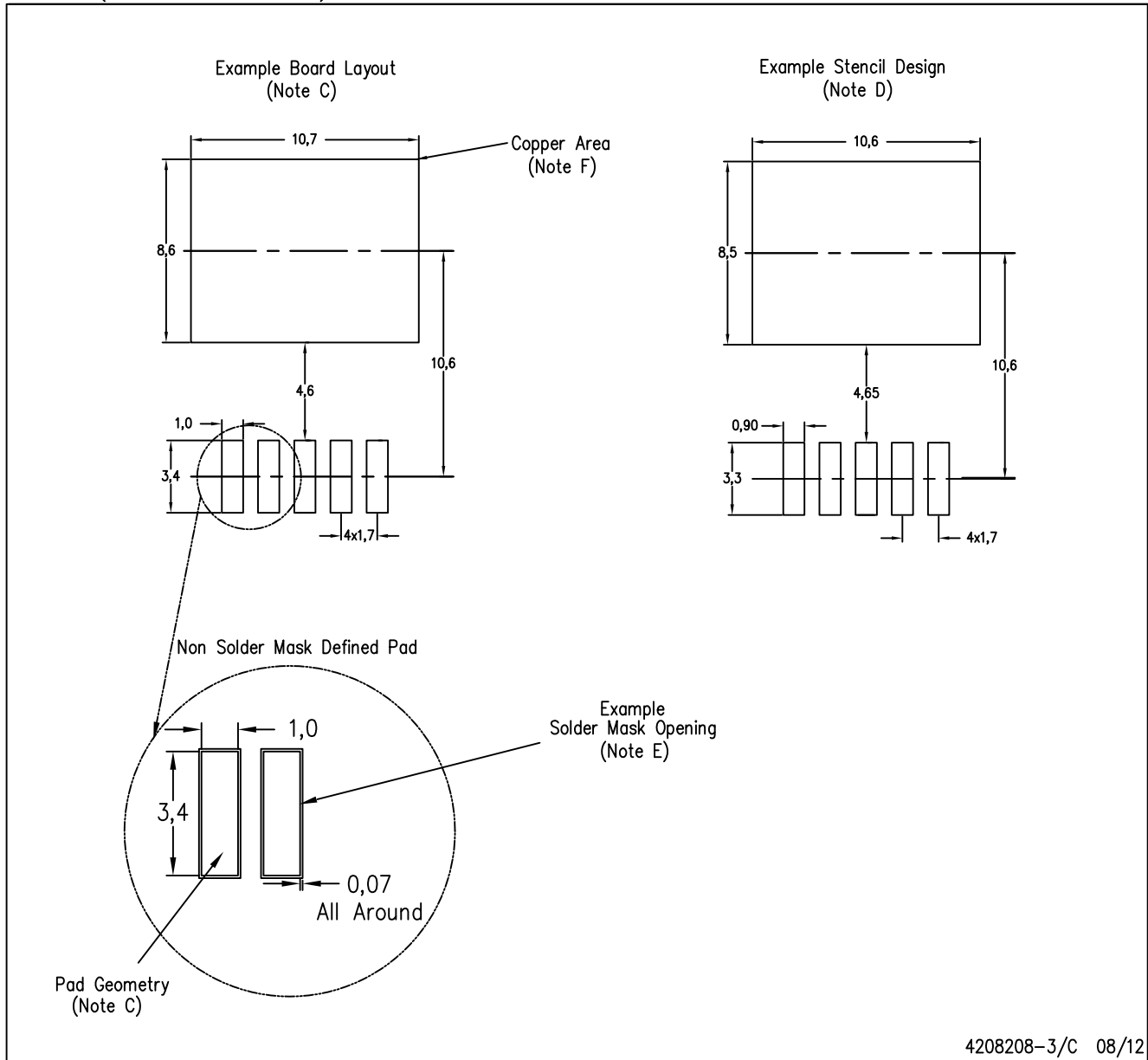


4200577-4/G 01/13

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
- $\triangle$  Falls within JEDEC TO-263 variation BA, except minimum lead thickness, maximum seating height, and minimum body length.

KTT (R-PSFM-G5)

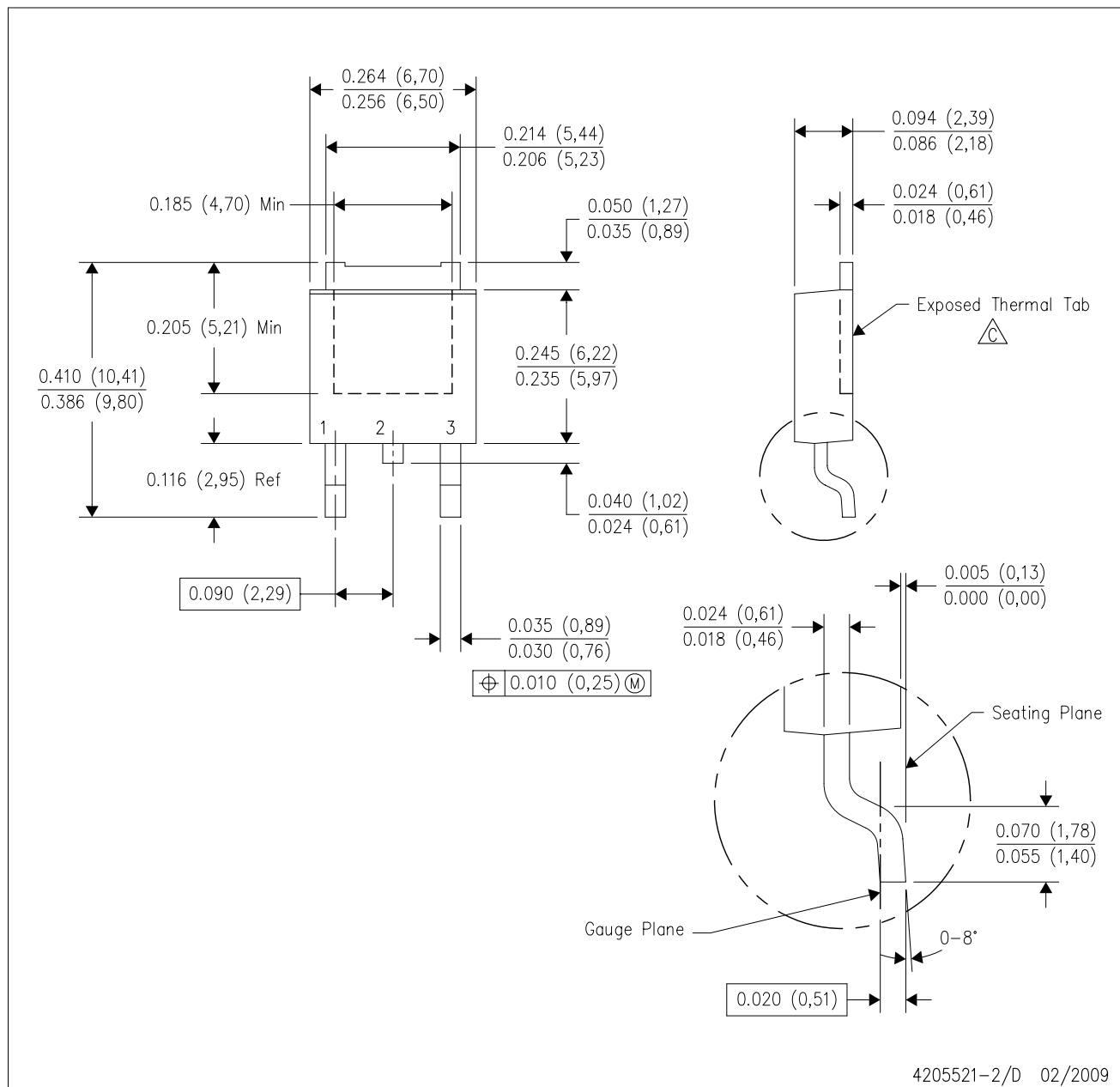
PLASTIC FLANGE-MOUNT PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-SM-782 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
  - F. This package is designed to be soldered to a thermal pad on the board. Refer to the Product Datasheet for specific thermal information, via requirements, and recommended thermal pad size. For thermal pad sizes larger than shown a solder mask defined pad is recommended in order to maintain the solderable pad geometry while increasing copper area.

KVU (R-PSFM-G3)

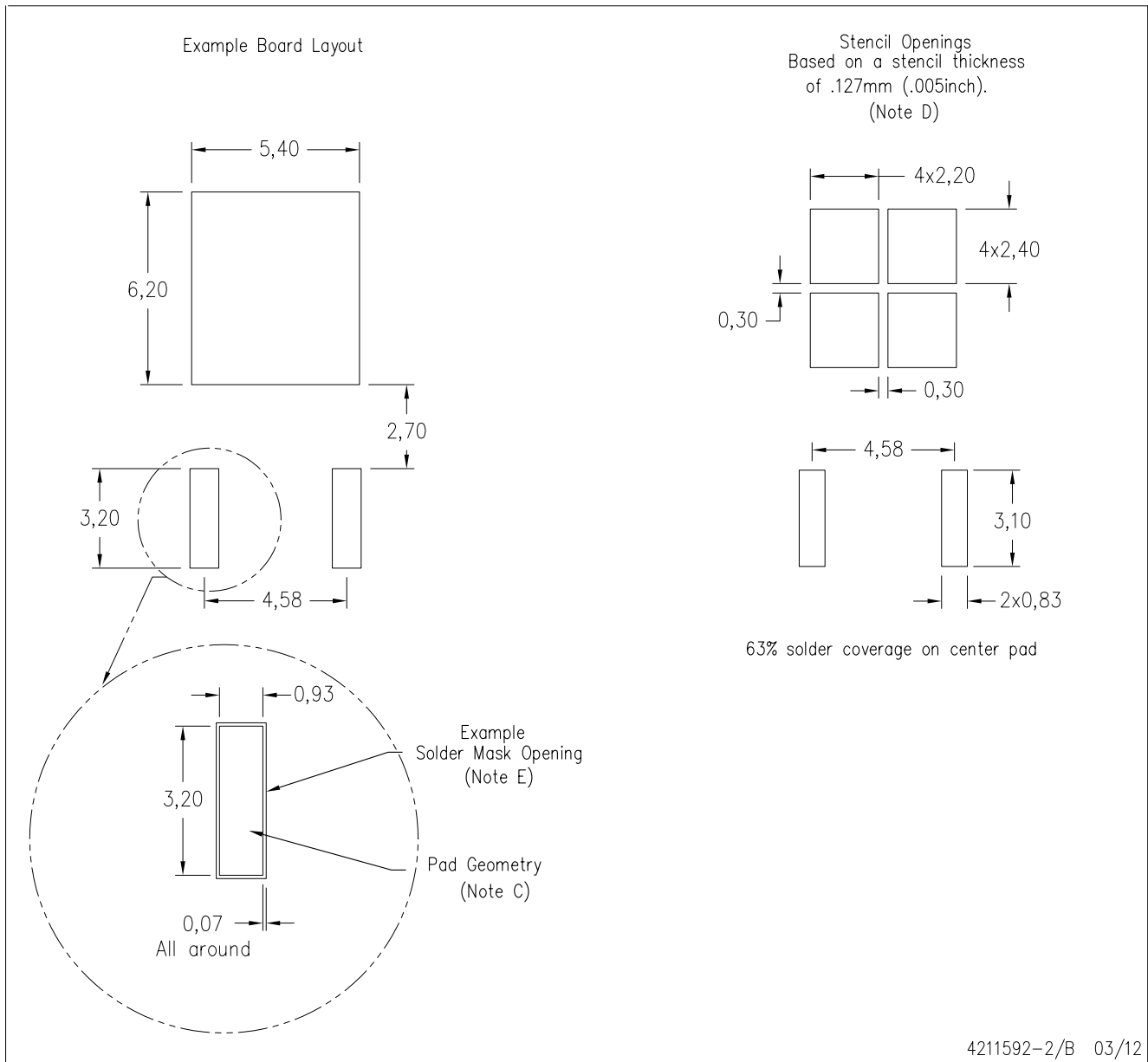
PLASTIC FLANGE-MOUNT PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. The center lead is in electrical contact with the exposed thermal tab.
  - D. Body Dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.006 (0,15) per side.
  - E. Falls within JEDEC TO-252 variation AA.

KVU (R-PSFM-G3)

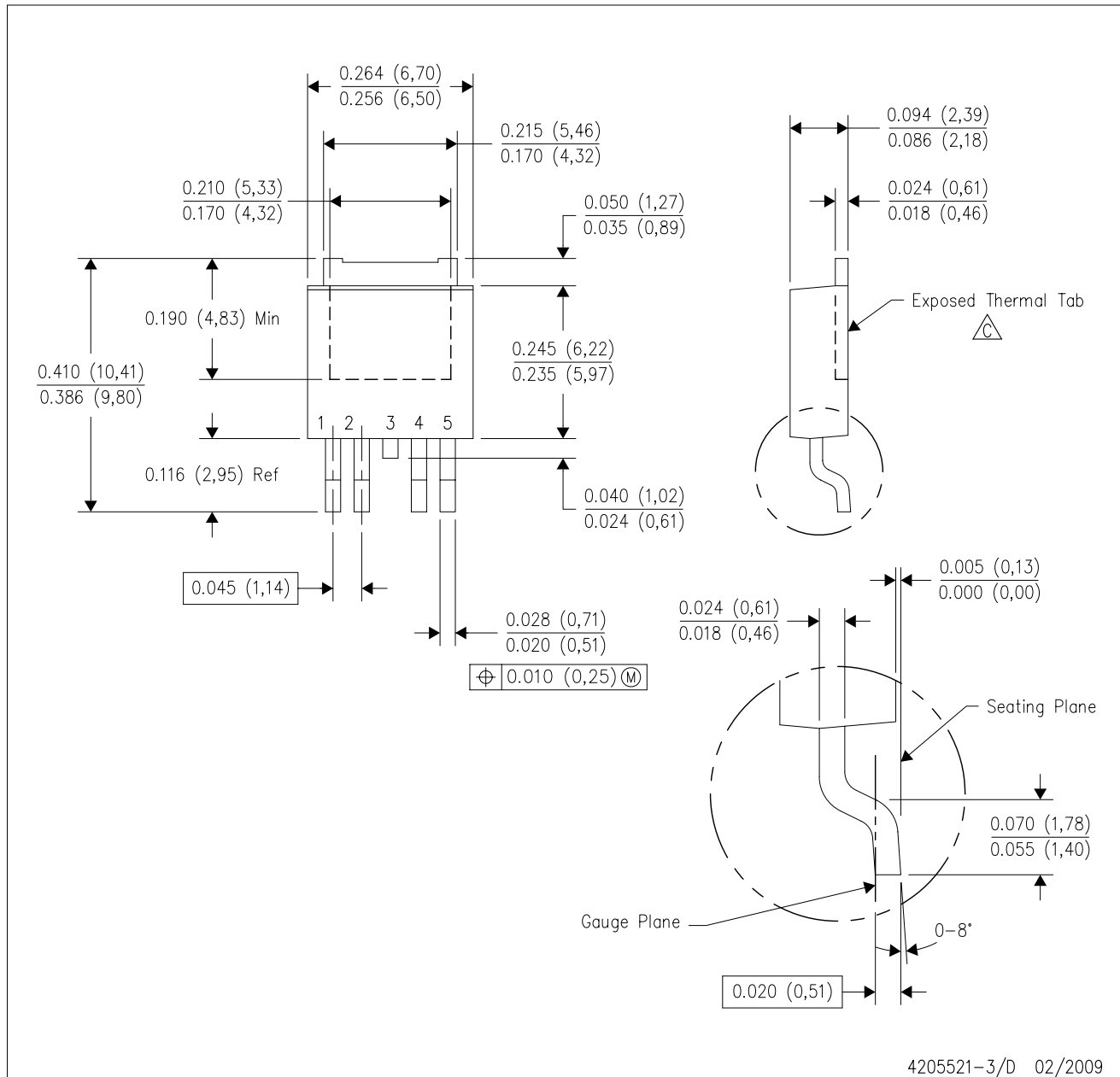
PLASTIC FLANGE MOUNT PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-SM-782 is an alternate information source for PCB land pattern designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

KVU (R-PSFM-G5)

PLASTIC FLANGE-MOUNT PACKAGE

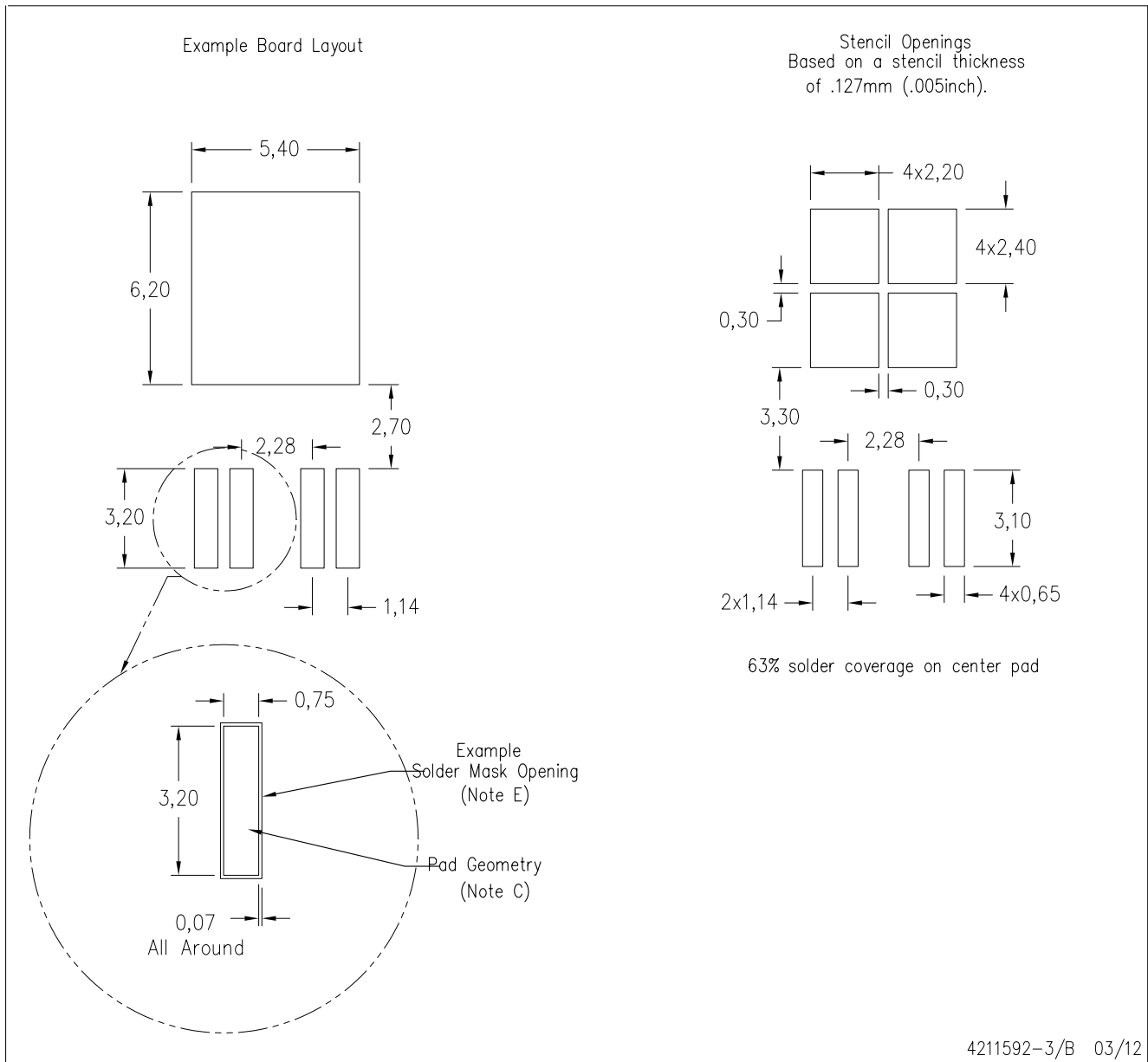


4205521-3/D 02/2009

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. The center lead is in electrical contact with the exposed thermal tab.
  - D. Body Dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.006 (0,15) per side.
  - E. Falls within JEDEC TO-252 variation AD.

KVU (R-PSFM-G5)

PLASTIC FLANGE MOUNT PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-SM-782 is an alternate information source for PCB land pattern designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

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