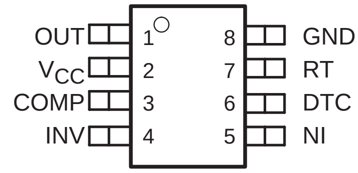
SLVS304A − SEPTEMBER 2000 − REVISED AUGUST 2002

- **Complete PWM Power Control**
- **3.6-V to 40-V Operation**
- **Internal Undervoltage-Lockout Circuit**
- **Oscillator Frequency . . . 20 kHz to 500 kHz**
- **Variable Dead Time Provides Control Over Total Range**
- **Ideal Controller for DDR Memory Application**
- **Uncommitted Error Amplifier Inputs**

**D PACKAGE**
**(TOP VIEW)**




## description

The TL5002 incorporates on a single monolithic chip all the functions required for a pulse-width-modulation (PWM) control circuit. Designed primarily for power-supply control, the TL5002 contains an error amplifier, a regulator, an oscillator, a PWM comparator with a dead-time-control input, undervoltage lockout (UVLO), and an open-collector output transistor.

The error-amplifier input common-mode voltage ranges from 0.9 V to 1.5 V. Dead-time control (DTC) can be set to provide 0% to 100% dead time by connecting an external resistor between DTC and GND. The oscillator frequency is set by terminating RT with an external resistor to GND. During low $V_{CC}$ conditions, the UVLO circuit turns the output off until $V_{CC}$ recovers to its normal operating range.

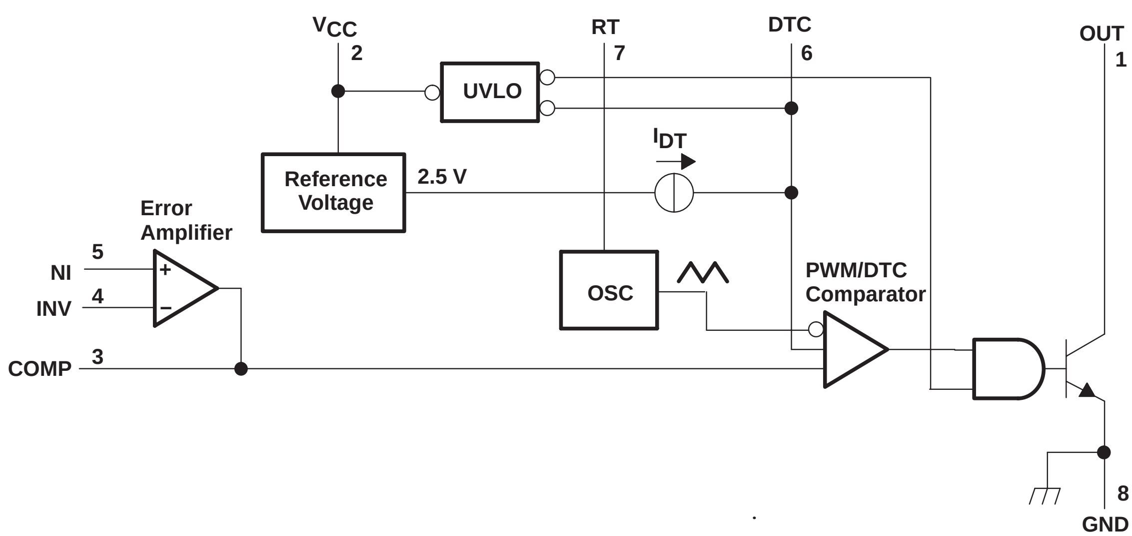
The TL5002 is characterized for operation from −40°C to 85°C.

**AVAILABLE OPTIONS**

| $T_A$ | SMALL OUTLINE (D) |
|---|---|
| −20°C to 85°C | TL5002CD |
| −40°C to 85°C | TL5002ID |

The D package is available taped and reeled. Add the suffix R to the device type (e.g., TL5002CDR).

## functional block diagram




Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

## detailed description

### voltage reference

A 2.5-V regulator operating from $V_{CC}$ is used to power the internal circuitry of the TL5002.

### error amplifier

The error amplifier compares a sample of the dc-to-dc converter output voltage to an external reference voltage and generates an error signal for the PWM comparator. The dc-to-dc converter output voltage is set by selecting the error-amplifier gain (see Figure 1), using the following expression:

$$V_O = (1 + R1/R2)\ (1\ V)$$

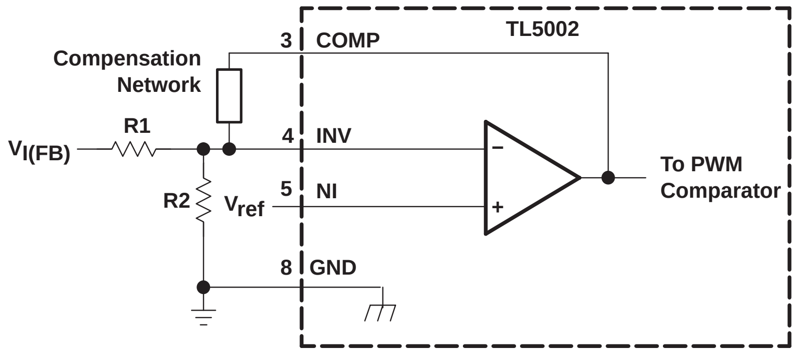



**Figure 1. Error-Amplifier Gain Setting**

The error-amplifier output is brought out as COMP for use in compensating the dc-to-dc converter control loop for stability. Because the amplifier can only source 45 µA, the total dc load resistance should be 100 kΩ or more.

### oscillator/PWM

The oscillator frequency ($f_{osc}$) can be set between 20 kHz and 500 kHz by connecting a resistor between RT and GND. Acceptable resistor values range from 15 kΩ to 250 kΩ. The oscillator frequency can be determined by using the graph shown in Figure 5.

The oscillator output is a triangular wave with a minimum value of approximately 0.7 V and a maximum value of approximately 1.3 V. The PWM comparator compares the error-amplifier output voltage and the DTC input voltage to the triangular wave and turns the output transistor off whenever the triangular wave is greater than the lesser of the two inputs.

### dead-time control (DTC)

DTC provides a means of limiting the output-switch duty cycle to a value less than 100%, which is critical for boost and flyback converters. A current source generates a reference current ($I_{DT}$) at DTC that is nominally equal to the current at the oscillator timing terminal, RT. Connecting a resistor between DTC and GND generates a dead-time reference voltage ($V_{DT}$), which the PWM/DTC comparator compares to the oscillator triangle wave as described in the previous section. Nominally, the maximum duty cycle is 0% when $V_{DT}$ is 0.7 V or less and 100% when $V_{DT}$ is 1.3 V or greater. Because the triangle wave amplitude is a function of frequency and the source impedance of RT is relatively high (1250 Ω), choosing $R_{DT}$ for a specific maximum duty cycle, D, is accomplished using the following equation and the voltage limits for the frequency in question as found in Figure 11 ($V_{osc}$max and $V_{osc}$min are the maximum and minimum oscillator levels):

### dead-time control (DTC) (continued)

$$R_{DT} = \left(R_t + 1250\right)\left[D\left(V_{osc}max - V_{osc}min\right) + V_{osc}min\right]$$

Where

$R_{DT}$ and $R_t$ are in ohms, D in decimal

Soft start can be implemented by paralleling the DTC resistor with a capacitor ($C_{DT}$) as shown in Figure 2. During soft start, the voltage at DTC is derived by the following equation:

$$V_{DT} \approx I_{DT}R_{DT}\left(1-e^{\left(-t/R_{DT}C_{DT}\right)}\right)$$

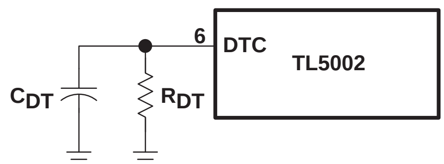



**Figure 2. Soft-Start Circuit**

If the dc-to-dc converter must be in regulation within a specified period of time, the time constant, $R_{DT}C_{DT}$, should be $t_0/3$ to $t_0/5$. The TL5002 remains off until $V_{DT} \approx 0.7$ V, the minimum ramp value. $C_{DT}$ is discharged every time UVLO becomes active.

### undervoltage-lockout (UVLO) protection

The undervoltage-lockout circuit turns the output transistor off whenever the supply voltage drops too low (approximately 3 V at 25°C) for proper operation. A hysteresis voltage of 200 mV eliminates false triggering on noise and chattering.

### output transistor

The output of the TL5002 is an open-collector transistor with a maximum collector current rating of 21 mA and a voltage rating of 51 V. The output is turned on under the following conditions: the oscillator triangle wave is lower than both the DTC voltage and the error-amplifier output voltage, and the UVLO circuit is inactive.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|---|
| Supply voltage, $V_{CC}$ (see Note 1) | 41 V |
| Amplifier input voltage, $V_{I(INV)}$, $V_{I(NI)}$ | 20 V |
| Output voltage, $V_O$, OUT | 51 V |
| Output current, $I_O$, OUT | 21 mA |
| Output peak current, $I_{O(peak)}$, OUT | 100 mA |
| Continuous total power dissipation | See Dissipation Rating Table |
| Operating ambient temperature range, $T_A$ | −40°C to 85°C |
| Storage temperature range, $T_{stg}$ | −65°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | 260°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network ground terminal.

**DISSIPATION RATING TABLE**

| PACKAGE | $T_A \le 25°C$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25°C$ | $T_A = 70°C$ POWER RATING | $T_A = 85°C$ POWER RATING | $T_A = 125°C$ POWER RATING |
|---|---|---|---|---|---|
| D | 725 mW | 5.8 mW/°C | 464 mW | 377 mW | 145 mW |

## recommended operating conditions

| | MIN | MAX | UNIT |
|---|---|---|---|
| Supply voltage, $V_{CC}$ | 3.6 | 40 | V |
| Amplifier input voltage, $V_{I(INV)}$, $V_{I(NI)}$ | 0.9 | 1.5 | V |
| Output voltage, $V_O$, OUT | | 50 | V |
| Output current, $I_O$, OUT | | 20 | mA |
| COMP source current | | 45 | μA |
| COMP dc load resistance | 100 | | kΩ |
| Oscillator timing resistor, $R_t$ | 15 | 250 | kΩ |
| Oscillator frequency, $f_{osc}$ | 20 | 500 | kHz |
| Operating ambient temperature, $T_A$ | −40 | 85 | °C |

## electrical characteristics over recommended operating free-air temperature range, $V_{CC}$ = 6 V, $f_{osc}$ = 100 kHz (unless otherwise noted)

### undervoltage lockout

| PARAMETER | TEST CONDITIONS | TL5002C | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP† | MAX | |
| Upper threshold voltage | $T_A$ = 25°C | | 3 | | V |
| Lower threshold voltage | $T_A$ = 25°C | | 2.8 | | V |
| Hysteresis | $T_A$ = 25°C | 100 | 200 | | mV |

† All typical values are at $T_A$ = 25°C.

### oscillator

| PARAMETER | TEST CONDITIONS | TL5002C | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | TYP† | MAX | |
| Frequency | $R_t$ = 100 kΩ | | 100 | | kHz |
| Standard deviation of frequency | | | 15 | | kHz |
| Frequency change with voltage | $V_{CC}$ = 3.6 V to 40 V | | 1 | | kHz |
| Frequency change with temperature | $T_A$ = −40°C to 25°C | −4 | −0.4 | 4 | kHz |
| | $T_A$ = −20°C to 25°C | −4 | −0.4 | 4 | kHz |
| | $T_A$ = 25°C to 85°C | −4 | −0.2 | 4 | kHz |
| Voltage at RT | | | 1 | | V |

† All typical values are at $T_A$ = 25°C.

### dead-time control

| PARAMETER | | TEST CONDITIONS | TL5002C | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP† | MAX | |
| Output (source) current | TL5002 | $V_{(DT)}$ = 1.5 V | $0.9 \times I_{RT}$‡ | | $1.2 \times I_{RT}$ | μA |
| Input threshold voltage | | Duty cycle = 0% | 0.5 | 0.7 | | V |
| | | Duty cycle = 100% | | 1.3 | 1.5 | |

† All typical values are at $T_A$ = 25°C.
‡ Output source current at RT

### error amplifier

| PARAMETER | | TEST CONDITIONS | TL5002C | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP† | MAX | |
| Input voltage | | $V_{CC}$ = 3.6 V to 40 V | 0.3 | | 1.5 | V |
| Input bias current | | | | −160 | −500 | nA |
| Output voltage swing | Positive | | 1.5 | 2.3 | | V |
| | Negative | | | 0.3 | 0.4 | V |
| Open-loop voltage amplification | | | | 80 | | dB |
| Unity-gain bandwidth | | | | 1.5 | | MHz |
| Output (sink) current | | $V_{I(INV)}$ = 1.2 V, COMP = 1 V | 100 | 600 | | μA |
| Output (source) current | | $V_{I(INV)}$ = 0.8 V, COMP = 1 V | −45 | −70 | | μA |

† All typical values are at $T_A$ = 25°C.

## electrical characteristics over recommended operating free-air temperature range, $V_{CC}$ = 6 V, $f_{osc}$ = 100 kHz (unless otherwise noted) (continued)

### output

| PARAMETER | TEST CONDITIONS | TL5002C MIN | TL5002C TYP† | TL5002C MAX | UNIT |
|---|---|---|---|---|---|
| Output saturation voltage | $I_O$ = 10 mA | | 1.5 | 2 | V |
| Off-state current | $V_O$ = 50 V, $V_{CC}$ = 0 | | | 10 | µA |
| | $V_O$ = 50 V | | | 10 | |
| Short-circuit output current | $V_O$ = 6 V | | 40 | | mA |

† All typical values are at $T_A$ = 25°C.

### total device

| PARAMETER | | TEST CONDITIONS | TL5002C MIN | TL5002C TYP† | TL5002C MAX | UNIT |
|---|---|---|---|---|---|---|
| Standby supply current | Off state | | | 1 | 1.5 | mA |
| Average supply current | | $R_t$ = 100 kΩ | | 1.4 | 2.1 | mA |

† All typical values are at $T_A$ = 25°C.

## PARAMETER MEASUREMENT INFORMATION

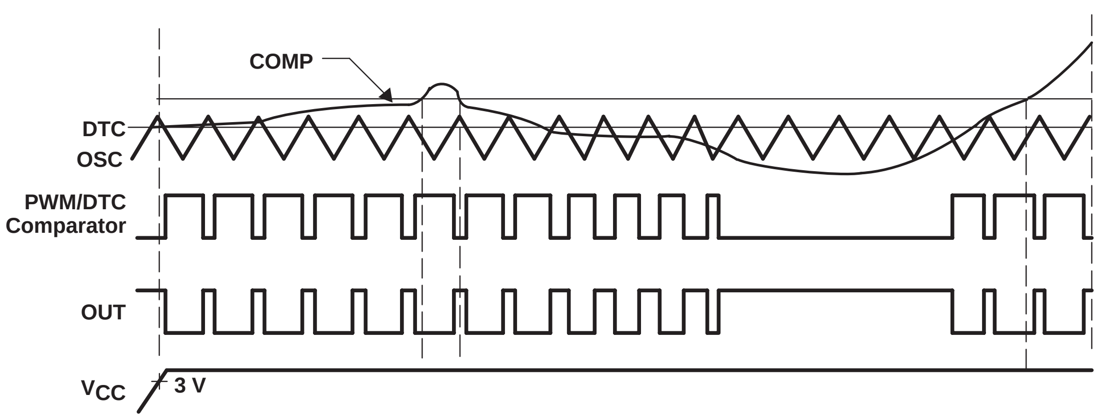



Figure 3. PWM Timing Diagram

## TYPICAL CHARACTERISTICS

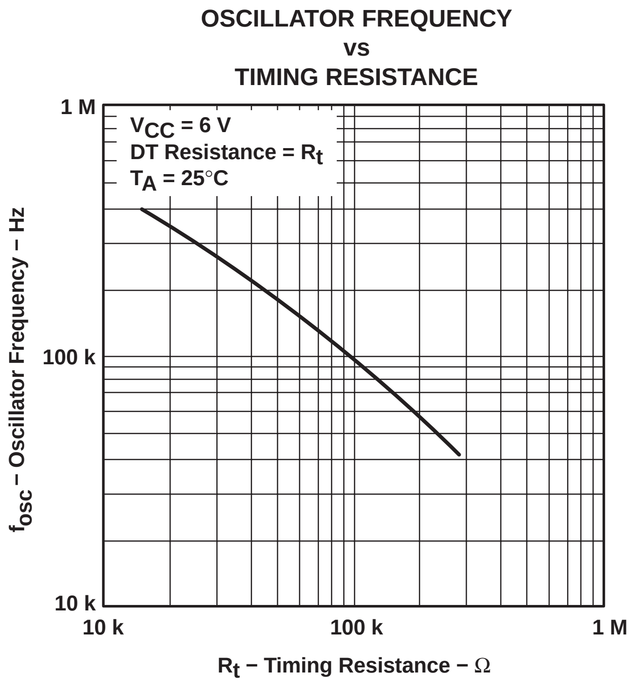



Figure 4

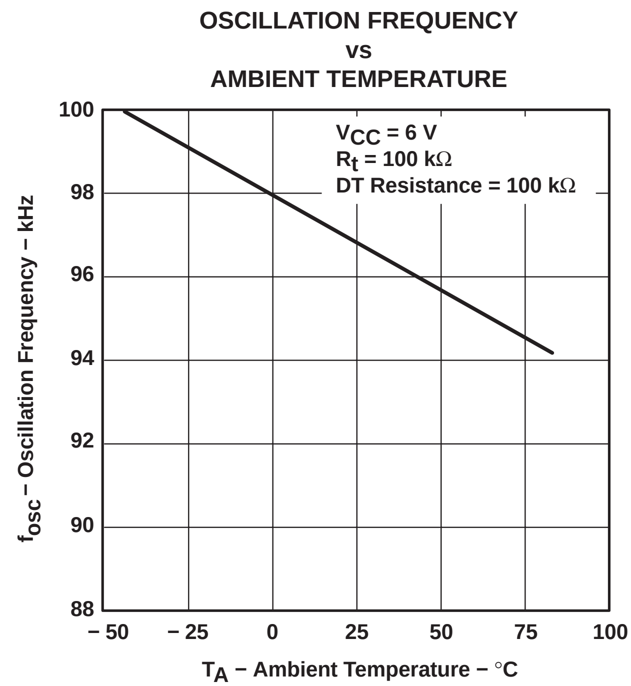



Figure 5

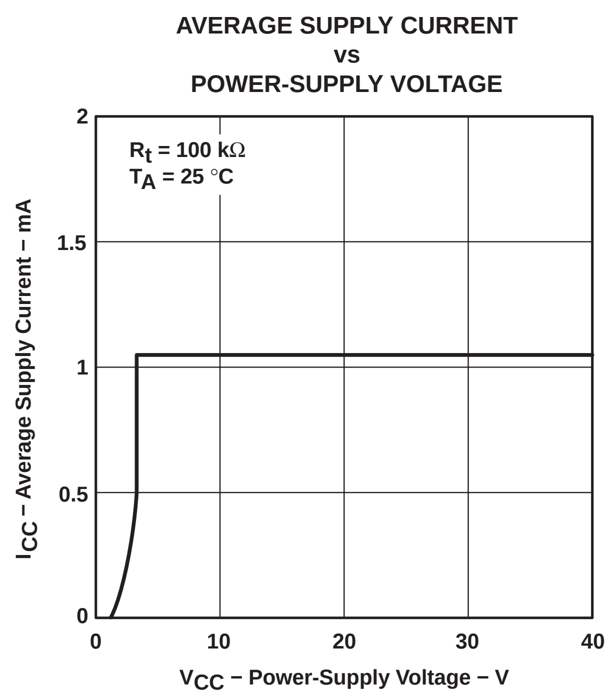



Figure 6

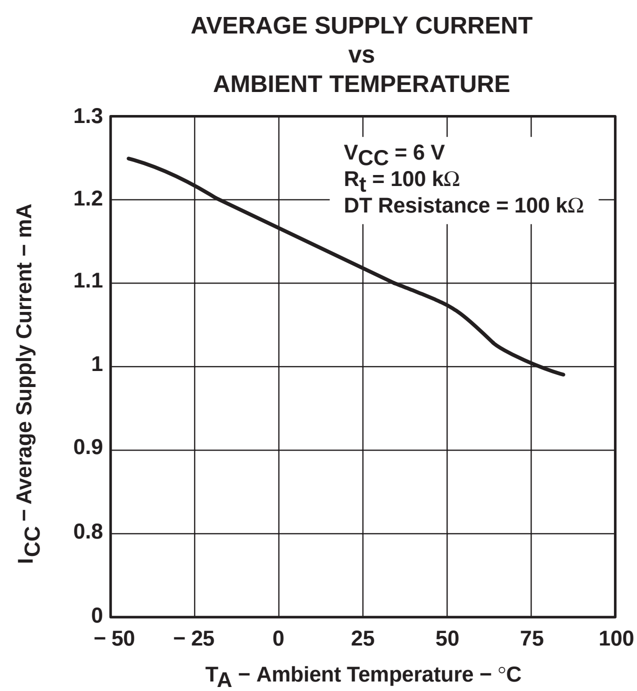



Figure 7

## TYPICAL CHARACTERISTICS

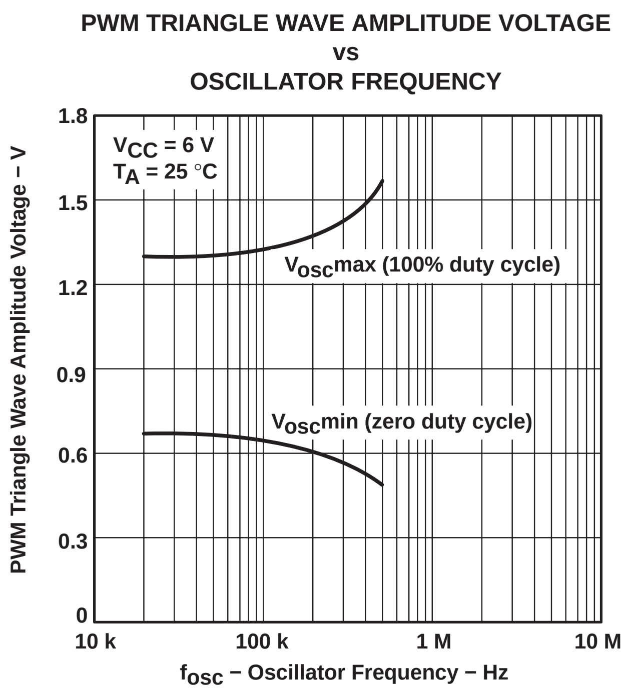



**Figure 8**

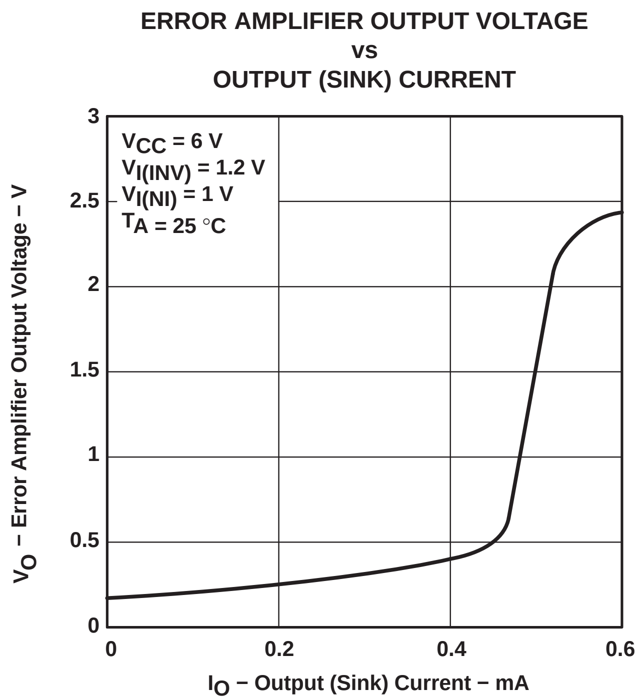



**Figure 9**

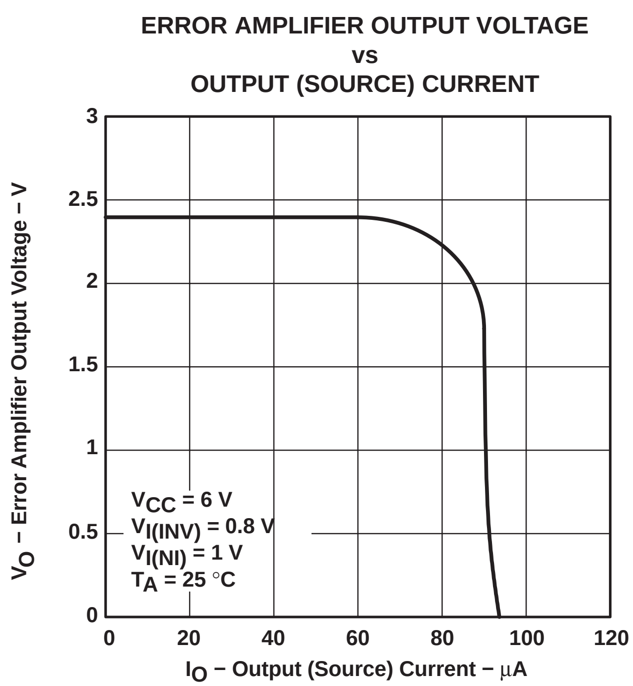



**Figure 10**

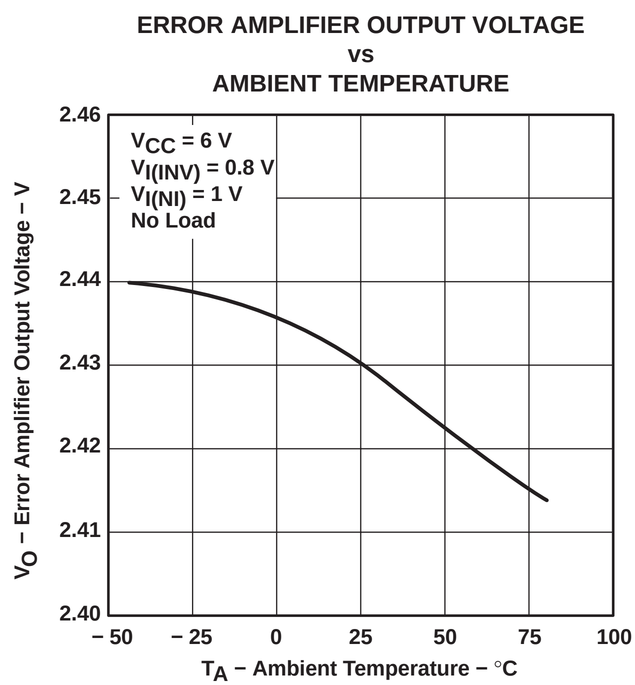



**Figure 11**

## TYPICAL CHARACTERISTICS

**ERROR AMPLIFIER OUTPUT VOLTAGE**
**vs**
**AMBIENT TEMPERATURE**

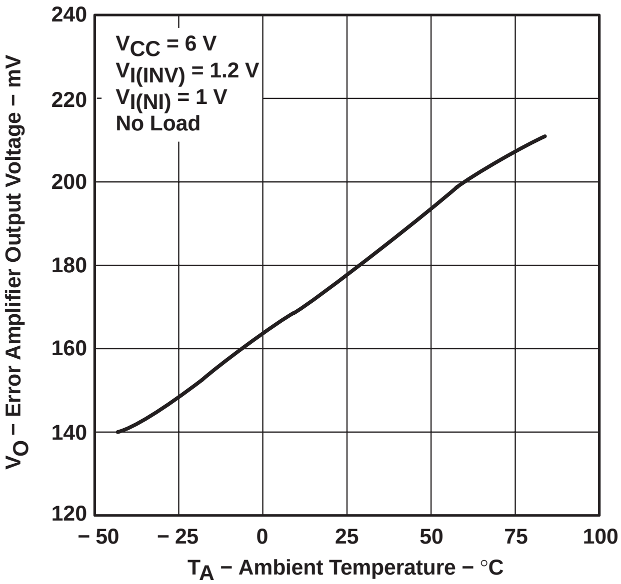



**Figure 12**

**OUTPUT DUTY CYCLE**
**vs**
**DTC VOLTAGE**

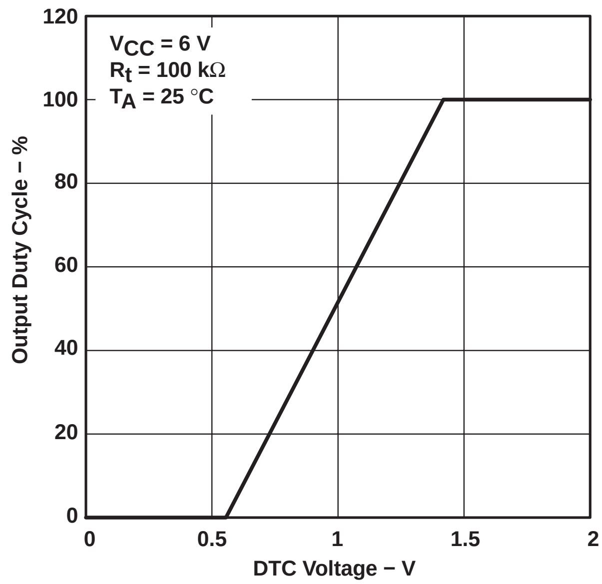



**Figure 13**

**ERROR AMPLIFIER CLOSED-LOOP GAIN AND PHASE SHIFT**
**vs**
**FREQUENCY**

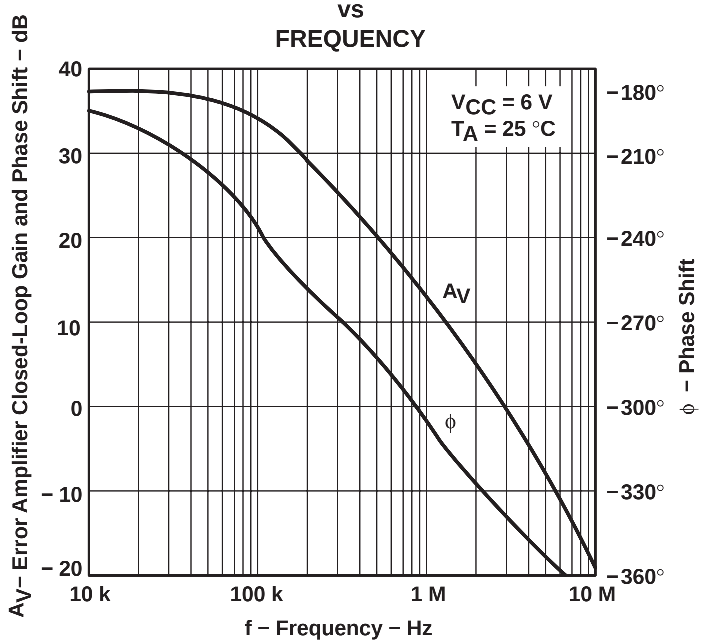



**Figure 14**

## TYPICAL CHARACTERISTICS

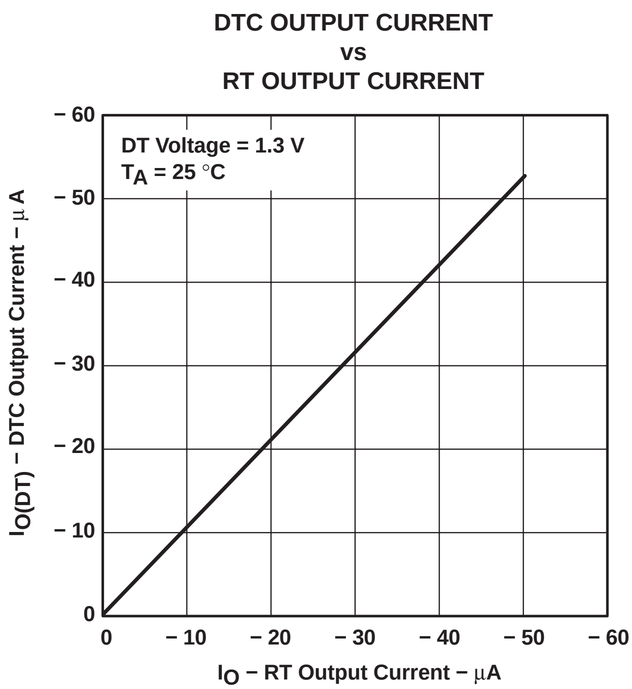



**Figure 15**

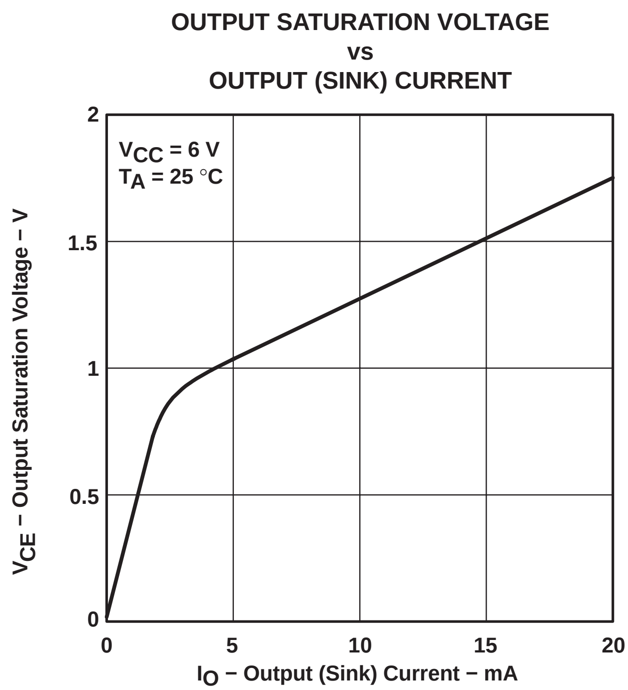



**Figure 16**

## APPLICATION INFORMATION

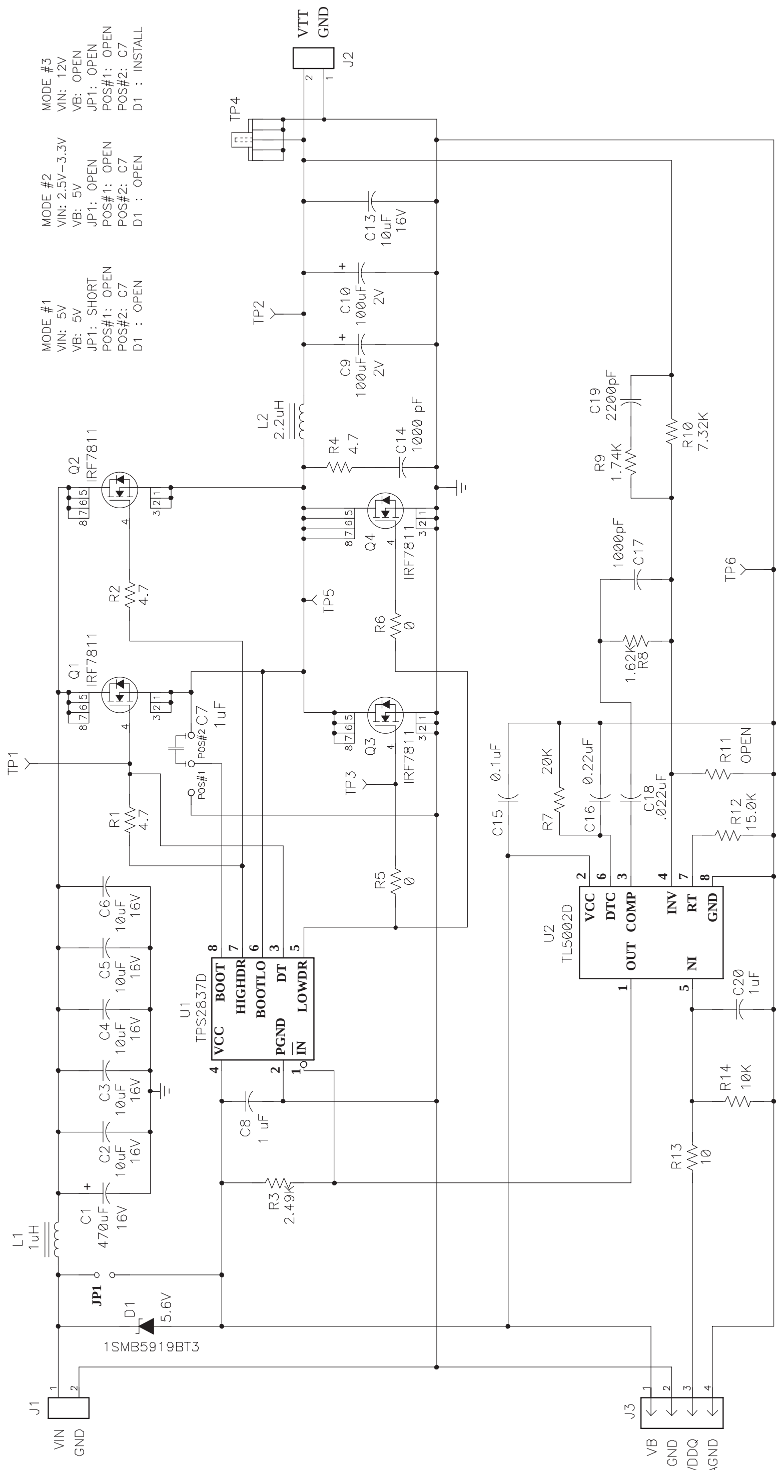



**Figure 17. DDRI Application**

## APPLICATION INFORMATION

**PARTIAL BILL OF MATERIALS**

| QUANTITY | REF DES | PART NUMBER | DESCRIPTION | MANUFACTURER | SIZE |
|---|---|---|---|---|---|
| 1 | C1 | UUD1C471MNR1GS | Capacitor, aluminum | Nichicon | 0.327 x 0.327 |
| 6 | C2 − C6, C13 | EMK325BJ106MN−B | Capacitor, ceramic | Taiyo Yuden | 1210 |
| 3 | C7, C8, C20 | GRM40X7R105K16PT | Capacitor, ceramic, jumper | Murata | 805 |
| 2 | C9, C10 | EEF−CD0D101R | Capacitor, aluminum | Panasonic | 7343 |
| 1 | C14 | 08055A102JAT2A | Capacitor, ceramic | AVX | 805 |
| 1 | C15 | GRM39X7R104K016D | Capacitor, ceramic | Murata | 603 |
| 1 | C16 | NMC0805X7R224K16TR | Capacitor, ceramic | NIP | 603 |
| 1 | C17 | VJ0603Y222KXANT | Capacitor, ceramic | Murata | 603 |
| 1 | C18 | C0603C223J3RACTU | Capacitor, ceramic | Kemet | 603 |
| 1 | C19 | GRM39X7R223K16 | Capacitor, ceramic | Murata | 603 |
| 1 | D1 | 1SMB5919BT3 | Diode, zener, 5.6 V | On Semi | SMB |
| 2 | J1, J2 | ED1609 | Terminal block, 2-pin | OST | |
| 1 | J3 | PTC36SAAN | Header, 4-pin | Sullins | |
| 1 | JP1 | PTC36SAAN | Header, 2-pin | Sullins | |
| 1 | L1 | UP2B−1R0 | Inductor, SMT | Coiltronics | 0.55 x 0.41 |
| 1 | L2 | UP4B−2R2 | Inductor, SMT | Coiltronics | |
| 4 | Q1 − Q4 | IRF7811 | MOSFET, N−ch, 30 V | IR | SO8 |
| 3 | R1, R2, R4 | Std | Resistor, chip, 4.7 Ω | Std | 603 |
| 1 | R3 | Std | Resistor, chip, 2.49 KΩ | Std | 603 |
| 2 | R5, R6 | Std | Resistor, chip, 0 Ω | Std | 603 |
| 1 | R7 | Std | Resistor, chip, 20 KΩ | Std | 603 |
| 1 | R8 | Std | Resistor, chip, 162 KΩ | Std | 603 |
| 1 | R9 | Std | Resistor, chip, 1.74 KΩ | Std | 603 |
| 1 | R10 | Std | Resistor, chip, 7.32 KΩ | Std | 603 |
| 1 | R11 | Std | Open | Std | 603 |
| 1 | R12 | Std | Resistor, chip, 15 KΩ | Std | 603 |
| 1 | R13 | Std | Resistor, chip, 10 Ω | Std | 603 |
| 1 | R14 | Std | Resistor, chip, 10 KΩ | Std | 603 |
| 4 | TP1 − TP3, TP5 | 240-345 | Test point, red, 1 mm | Farnell | 0.038 |
| 1 | TP4 | 131-4244-00 or 131-5031-00 | Adaptor, 3.5 mm probe | Tektronix | 0.200 |
| 1 | TP6 | 1045-3-17-15-30-14-02-0 | Post, wirewrap | Mill-Max | 0.043 |
| 1 | U1 | TPS2837D | IC, MOSFET driver | Texas Instruments | SO8 |
| 1 | U2 | TL5002D | IC, low-cost PMW | Texas Instruments | SO8 |

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| TL5002CD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TL5002CDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TL5002CDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TL5002CDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TL5002ID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TL5002IDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TL5002IDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| TL5002IDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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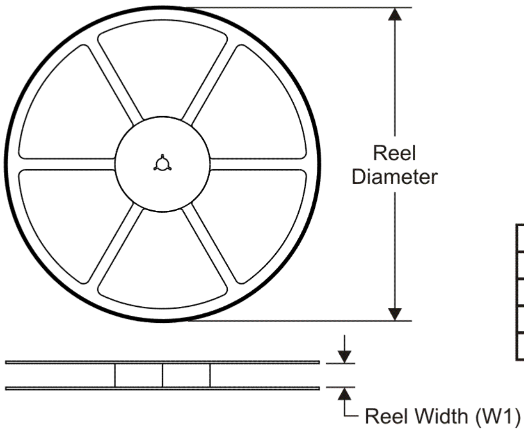
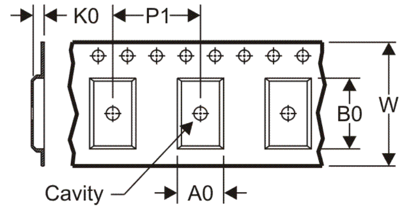
## TAPE AND REEL INFORMATION

### REEL DIMENSIONS

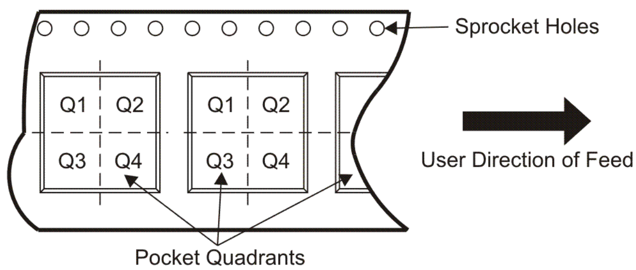



### TAPE DIMENSIONS




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

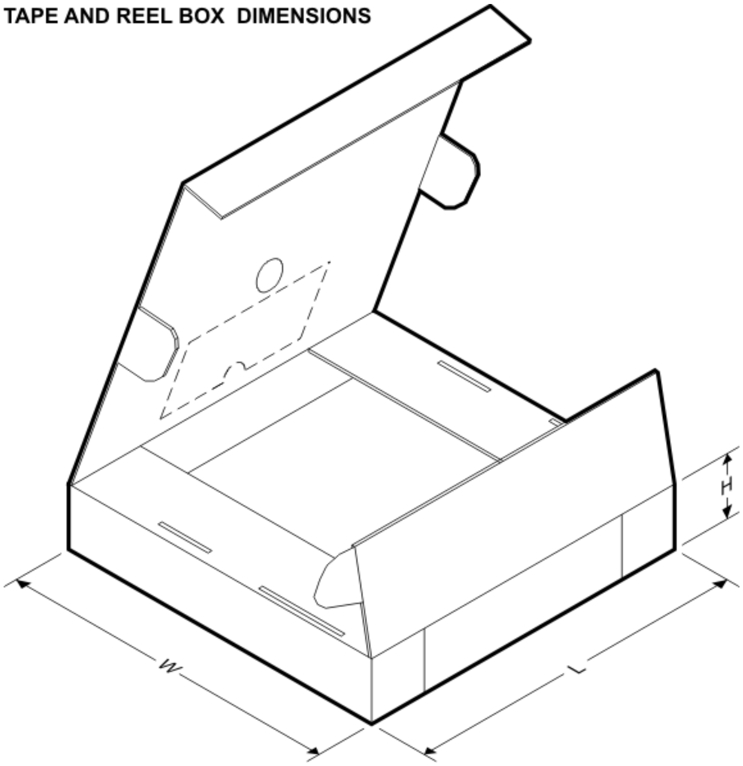
### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TL5002CDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TL5002IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

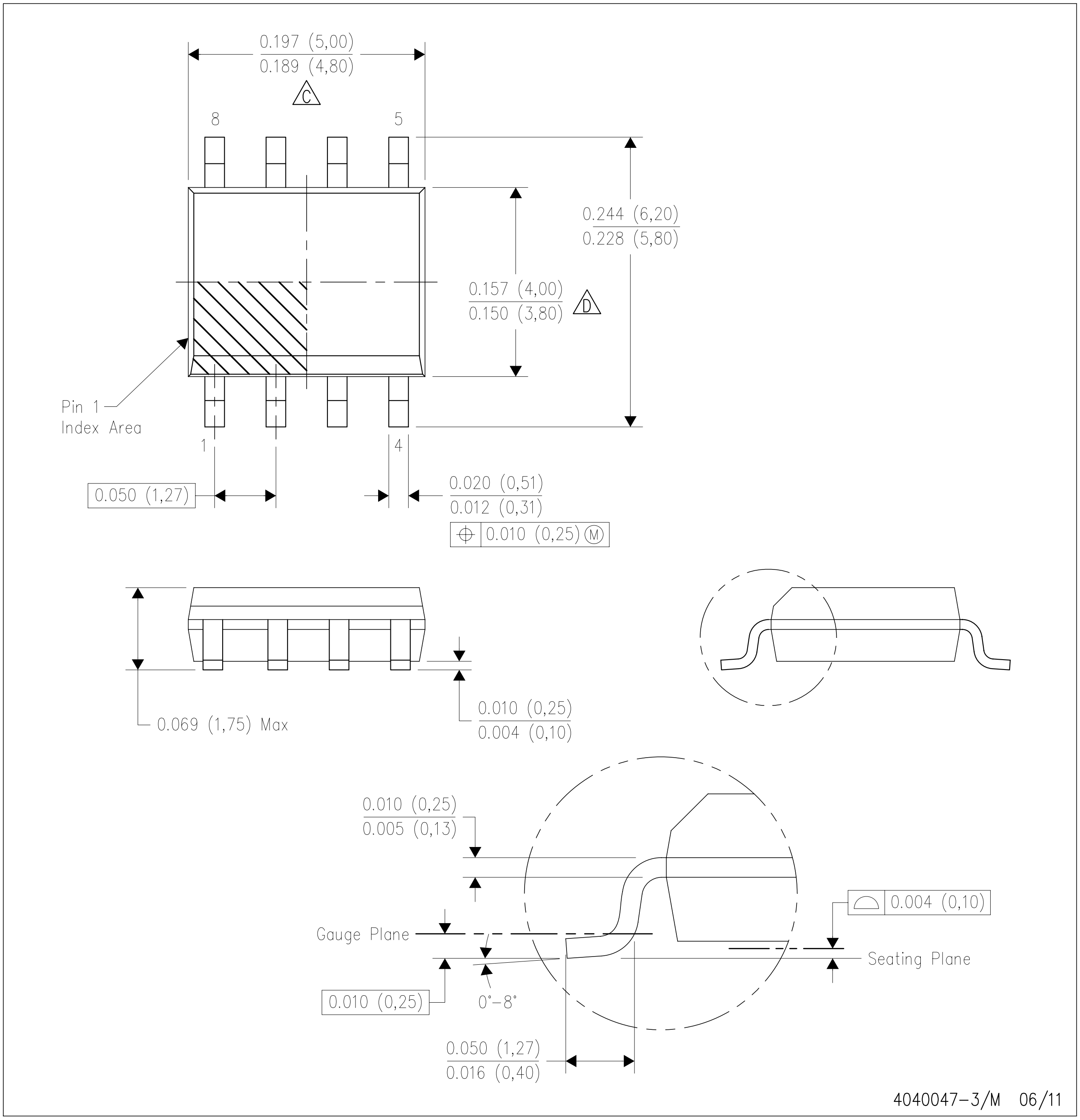
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

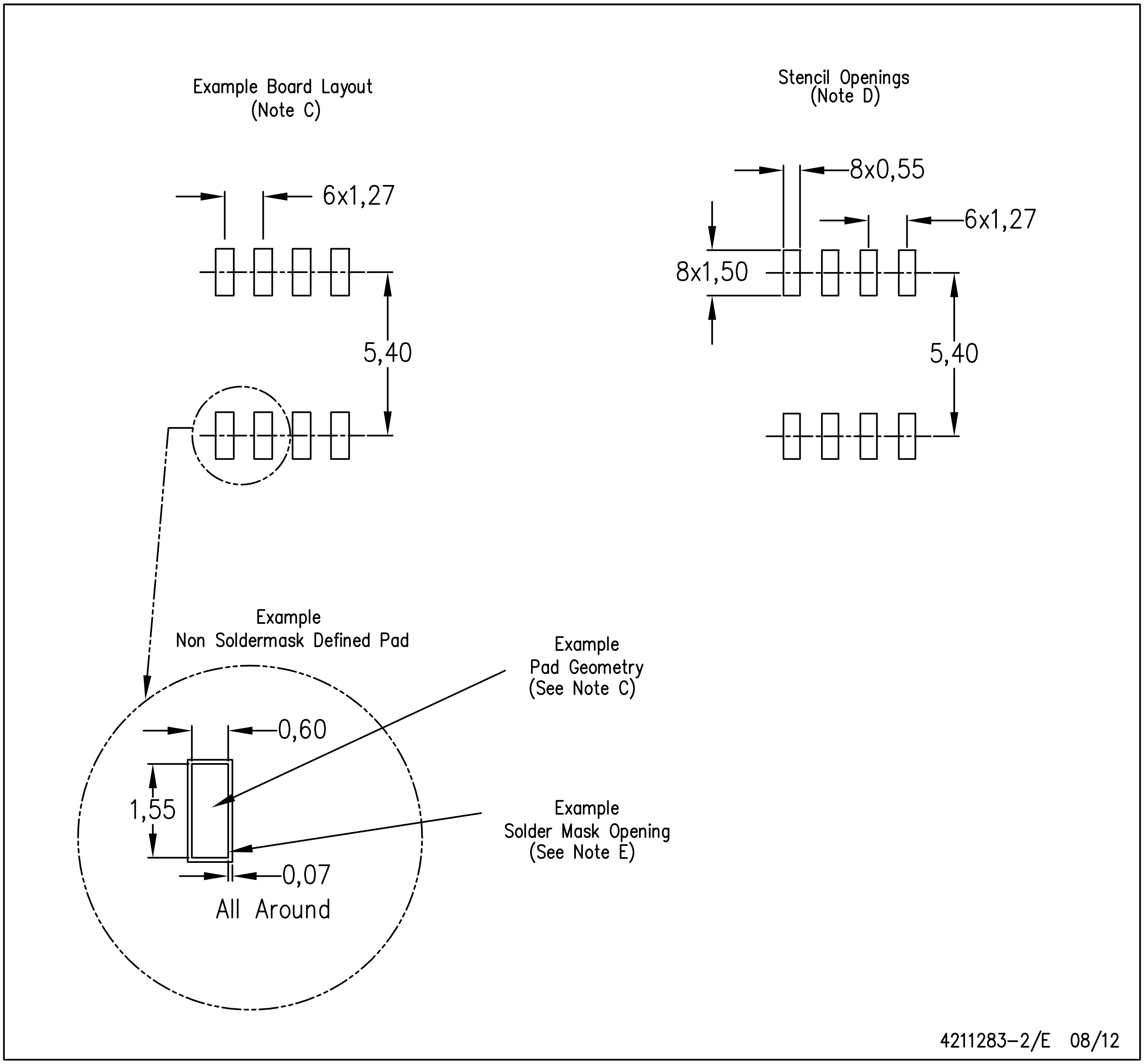
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TL5002CDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TL5002IDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |

D (R–PDSO–G8) PLASTIC SMALL OUTLINE




NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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