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- Integrated Asynchronous Communications Element (ACE) Compatible With PCMCIA PC Card Standard Release 2.01
- Consists of a Single TL16C550 ACE Plus PCMCIA Interface Logic
- Provides Common I-Bus/Z-Bus Microcontroller Inputs for Most Intel<sup>™</sup> and Ziloq<sup>™</sup> Subsystems
- Fully Programmable 256-Byte Card Information Structure (CIS) and 8-Byte Card Configuration Register (CCR)
- Adds or Deletes Standard Asynchronous Communication Bits (Start, Stop and Parity) to or From Serial Data Stream
- Independently Controlled Transmit, Receive, Line Status, and Data Set Interrupts
- Subsystem Selectable Serial-Bypass Mode Provides Subsystem With Direct Parallel Access to the FIFOs

- Fully Programmable Serial-Interface Characteristics:
  - 5-, 6-, 7-, or 8-Bit Characters
  - Even-, Odd-, or No-Parity Bit Generation and Detection
  - 1-, 1 1/2-, or 2-Stop Bit Generation
  - Baud-Rate Generation
- Fully Prioritized Interrupt System Controls
- Modem Control Functions
- Provides TL16C450 Mode at Reset Plus Selectable Normal TL16C550 Operation or Extended 64-Byte FIFO Mode
- Selectable Auto-RTS Mode Deactivates RTS at 14 Bytes in 550 Mode and at 56 Bytes in Extended 550 Mode
- Selectable Auto-CTS Mode Deactivates
   Serial Transfers When CTS is Inactive
- Available in 100 Pin Thin Quad Flatpack (PZ) Package or 100-Ball (GGM) MicroStar BGA™ Package

### description

The TL16PC564B/BLV is designed to provide all the functions necessary for a Personal Computer Memory Card International Association (PCMCIA) universal asynchronous receiver transmitter (UART) subsystem interface. This interface provides a serial-to-parallel conversion for data to and from a modem coder-decoder/digital signal processor (CODEC/DSP) function to a PCMCIA parallel data-port format. A computer central processing unit (CPU), through a PCMCIA host controller, can read the status of the asynchronous communications element (ACE) interface at any point in the operation. Reported status information includes the type of transfer operation in process, the status of the operation, and any error conditions encountered.

Attribute memory consists of a 256-byte card information structure (CIS) and eight 8-byte card configuration registers (CCR). The CIS, implemented with a dual-port random-access memory (DPRAM), is available to both the host CPU and subsystem (modem), as are the CCRs. This DPRAM is used in place of the electrically erasable programmable read-only memory (EEPROM) normally used for the CIS. At power up, attribute memory is initialized by the subsystem.

The TL16PC564B/BLV uses a TL16C550 ACE-type core with an expanded  $64 \times 11$  receiver first-in-first-out (FIFO) memory and a  $64 \times 8$  transmitter FIFO memory. The receiver trigger logic flags have been adjusted in order to take full advantage of the increased capacity when in the extended mode. In addition, eight of the UART registers have been mapped into the subsystem (modem) memory space as read-only registers. This allows the subsystem to read UART status information.

A subsystem-selectable serial-bypass mode has been implemented to allow the subsystem to bypass the serial portion of the UART and write directly to the receiver FIFO and read directly from the transmitter FIFO. Interrupt operation is not affected in this mode.



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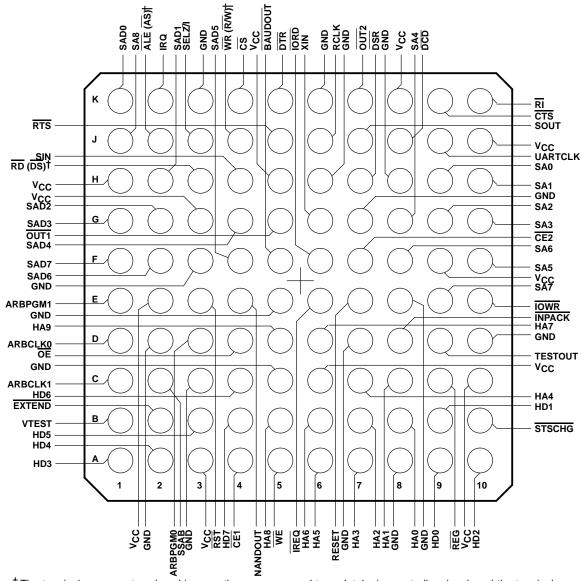
ALE (

#### **PZ PACKAGE** (TOP VIEW) HD3 HD4 HD5 VCC HD6 HD7 GRD HA8 WE NE HA7 VCC HA6 HA5 HA3 HA3 HA3 HA3 GND HA1 HD0 HD1 $\begin{array}{c} 000 \\$ EXTEND [ 75 ∃ HD2 □ STSCHG VTEST □ 2 74 SSAB [ 3 73 REG GND □ □ V<sub>CC</sub> 72 ARBCLKI 🗆 □ INPACK 71 GND □ ☐ TESTOUT 70 ARBCLKO □ 69 ARBPGM0 □ □ GND 68 RESET ARBPGM1 □ 67 V<sub>CC</sub> □ 10 66 GND RST 🗆 65 🗆 SA7 NANDOUT [ 64 D TOWR GND □ 13 63 D IORD SAD7 14 62 CE2 SAD6 ☐ 15 61 □ SA6 GND □ 16 60 □ V<sub>CC</sub> SAD5 □ 17 59 □ SA5 □ SA4 SAD4 18 58 □ SA3 SAD3 □ 19 57 □ SA2 SAD2 20 56 V<sub>CC</sub> □ 21 V<sub>CC</sub> □ 22 SAD1 □ 23 55 □ SA1 54 $\square$ GND □ SA0 53 b vcc SA8 24 52 SAD0 🗆 UARTCLK 25 51 SELZÍ SELZÍ RD(DS)† OUT1 BAUDOUT GND GND GND GND WR(R/W)



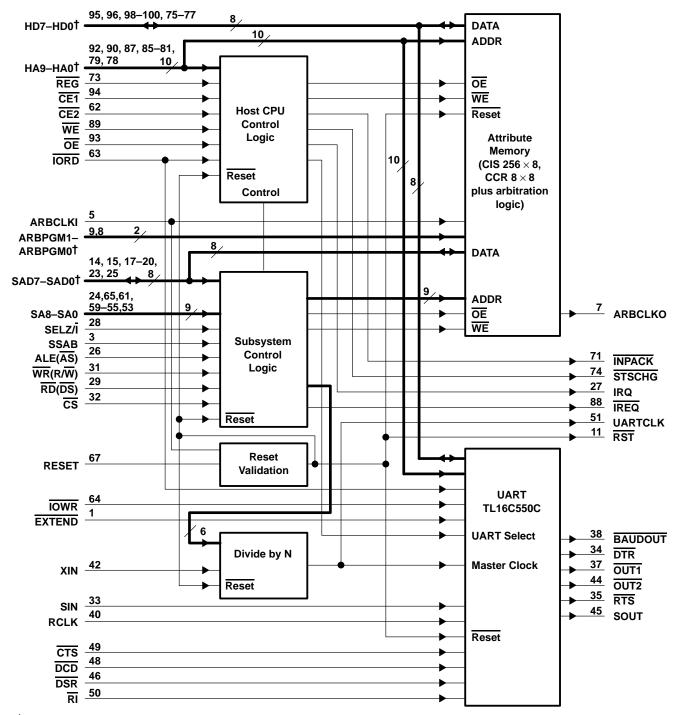
<sup>&</sup>lt;sup>†</sup>The terminal names not enclosed in parentheses correspond to an Intel microcontroller signal, and the terminal names enclosed in parentheses correspond to a Zilog microcontroller signal.

### GGM PACKAGE (BOTTOM VIEW)



<sup>†</sup>The terminal names not enclosed in parentheses correspond to an Intel microcontroller signal, and the terminal names enclosed in parentheses correspond to a Zilog microcontroller signal.

### block diagram



<sup>†</sup>Bit 0 is the least significant bit.



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### **Terminal Functions**

	TERMINAL		INTER-		
NAME	PZ NO.	GGM NO.	FACE†	1/0	DESCRIPTION
ALE (AS)	26	J2	S	I	Address-latch enable/address strobe. ALE $(\overline{AS})$ is an address-latch enable in the Intel mode and an address strobe in the Zilog mode. ALE $(\overline{AS})$ is active high for an Intel subsystem and active low for a Zilog subsystem.
ARBCLKO	7	D1	М	0	Arbitration clock output. ARBCLKO is equal to the input on ARBCLKI divided by the binary-coded divisor input on ARBPGM (1–0).
ARBCLKI	5	C1	М	I	Arbitration clock input. ARBCLKI is the base clock used in arbitration for the attribute memory DRAM and the reset validation circuitry.
ARBPGM0 ARBPGM1	8 9	D3 E1	М	I	Arbitration clock divisor program. These two bits set the divisor for ARBCLKI. Divide by 1, 2, 4, and 8 are available.
BAUDOUT	38	F5	U	0	Baud output. BAUDOUT is an active-low 16× signal for the transmitter section of the UART. The clock rate is established by the reference clock (UARTCLK) frequency divided by a divisor specified by the baud generator divisor latches. BAUDOUT may also be used for the receiver section by tying this output to the RCLK input.
CE1 CE2	94 62	A4 F7	Н	I	Card enable 1 and card enable 2 are active-low signals. CE1 enables even-numbered address bytes, and CE2 enables odd-numbered address bytes. A multiplexing scheme based on HA0, CE1, and CE2 allows an 8-bit host to access all data on HD0 through HD7 if desired. These signals have internal pullup resistors.
CS	32	K4	S	I	Chip select. CS is the active-low chip select from the Zilog or Intel microcontroller.
CTS	49	К9	U	I	Clear to send. CTS is an active-low modem status signal whose condition can be checked by reading bit 4 (CTS) of the modem status register (MSR). Bit 0 (delta clear to send) of the MSR indicates that the signal has changed states since the last read from the MSR. If the modem-status interrupt is enabled when CTS changes states, an interrupt is generated.
DCD	48	J8	U	I	Data carrier detect. $\overline{DCD}$ is an active-low modem-status signal whose condition can be checked by reading bit 7 (DCD) of the MSR. Bit 3 (delta data carrier detect) of the MSR indicates that the signal has changed states since the last read from the MSR. If the modem-status interrupt is enabled when $\overline{DCD}$ changes states, an interrupt is generated.
DSR	46	H7	U	I	Data set ready.    \overline{DSR} is an active-low modem status signal whose condition can be checked by reading bit 5 (DSR) of the MSR. Bit 1 (delta data set ready) of the MSR indicates that the signal has changed states since the last read from the MSR. If the modem-status interrupt is enabled when DSR changes states, an interrupt is generated.
DTR	34	K5	U	0	Data terminal ready. $\overline{\text{DSD}}$ is an active-low signal. When active, $\overline{\text{DTR}}$ informs the modem or data set that the UART is ready to establish communication. $\overline{\text{DTR}}$ is placed in the active state by setting the DTR bit 0 of the modem control register (MCR) to a high level. $\overline{\text{DTR}}$ is placed in the inactive state either as a result of a reset, doing a loop-mode operation, or resetting bit 0 (DTR) of the MCR.
EXTEND	1	B2	U	I	FIFO extend. When EXTEND is high, the UART is configured as a standard TL16C550 with 16-byte transmit and receive FIFOs. When EXTEND is low and FIFO control register (FCR) bit 5 is high, the FIFOs are extended to 64 bytes and the receiver-interrupt trigger levels adjust accordingly. EXTEND low in conjunction with FIFO control register (FCR) bit 4 set high enables the auto-RTS function.
GND	4,6,13,16,30, 39,41,43,54, 66,68,69,80,91	C3,D2,E5,F3, K3,K6,H6,G7, H8,E8,D7,D10 A8,C5	М		Common ground

<sup>†</sup> Host = H, Subsystem = S, UART = U, Miscellaneous = M



### **Terminal Functions**

TERMINAL		INTER- 1/0		DESCRIPTION		
NAME	PZ NO.	GGM NO.	FACE†	1/0	DESCRIPTION	
HA0 HA1 HA2	78 79 81	B8 C8 B7	Н	I	The 10-bit address bus addresses the attribute memory (bits 1–8) and addresses the internal UART as either PCMCIA I/O (bits 0–2) or as a standard COM port (bits 0–9).	
HA3	82	A7				
HA4	83	C7				
HA5	84	A6				
HA6	85	B6				
HA7	87	D6				
HA8	90	B5				
HA9	92	D5				
HD0	77	A9	Н	I/O	The 8-bit bidirectional data bus transfers data to and from the attribute memory and	
HD1	76	B9			the internal UART.	
HD2	75	A10				
HD3	100	A1				
HD4	99	A2				
HD5	98	B3				
HD6	96	C4				
HD7	95	B4				
INPACK	71	D8	Н	0	Input port acknowledge. INPACK is an active-low output signal that is asserted when the card responds to an I/O read cycle at the address on the HA bus.	
IORD	63	F6	Н	_	I/O read strobe. $\overline{\text{IORD}}$ is an active-low input signal activated to read data from the card I/O space. The $\overline{\text{REG}}$ signal and at least one of the card enable inputs ( $\overline{\text{CE1}}$ , $\overline{\text{CE2}}$ ) must also be active for the I/O transfer to take place. This signal has an internal pullup resistor.	
IOWR	64	E10	Н	I	I/O write strobe. IORW is an active-low input signal activated to write data to the call/O space. The REG signal and at least one of the card enable inputs (CE1, CE2) multiple also be active for the I/O transfer to take place. This signal has an internal pullipresistor.	
IREQ	88	E6	Н	0	Interrupt request. IREQ is an active-low output signal asserted by the card to indicate to the host CPU that a card device requires host software service. This signal doub as READY/BUSY during power-up initialization.	
IRQ	27	K2	S	0	Interrupt request. This active-high IRQ to the subsystem indicates a host CPU write to attribute memory has occurred.	
NANDOUT	12	E4	М	0	This is a production test output.	
ŌĒ	93	D4	Н	I	Output enable. OE is an active-low input signal used to gate memory read data from the card. This signal has an internal pullup resistor.	
OUT1 OUT2	37 44	G5 K7	U	0	Output 1 and output 2 are active-low signals. OUT1 and OUT2 are user-defined output terminals that are set to their active state by setting respective MCR bits (OUT1 and OUT2) high. OUT1 and OUT2 are set to their inactive (high) state as a result of a reset, doing loop-mode operation, or by resetting bit 2 (OUT1) or bit 3 (OUT2) of the MCR. This signal has an open-drain outputs.	
RCLK	40	J6	U	I	Receiver clock. RCLK is the 16×-baud-rate clock input for the receiver section of the UART.	
RD(DS)	29	H3	S	I	Read enable or data strobe input. $\overline{RD}(\overline{DS})$ is the active-low read enable in the Intel mode and the active-low data strobe in the Zilog mode.	
REG	73	C9	Н	I	Attribute memory select. This active-low input signal is generated by the host CPU and accesses attribute memory (OE and WE active) and I/O space (IORD or IOWF active). PCMCIA common memory access is excluded. This signal has an internal pullup resistor and hysteresis on the input buffer.	
RESET	67	E7	Н	I	Reset. RESET is an active-high input that serves as the master reset for the device. RESET clears the UART, placing the card in an unconfigured state. This signal has an internal pullup resistor.	

<sup>†</sup> Host = H, Subsystem = S, UART = U, Miscellaneous = M



### **Terminal Functions**

NAME	TERMINAL PZ NO.	GGM NO.	INTER- FACET	1/0	DESCRIPTION
RI	50	K10	U	I	Ring indicator. $\overline{RI}$ is an active-low modem status signal whose condition can be checked by reading bit 6 (RI) of the MSR. The trailing-edge ring indicator (TERI) bit 2 of the MSR indicates that $\overline{RI}$ has transitioned from a low to a high state since the last read from the MSR. If the modem status interrupt is enabled when this transition occurs, an interrupt is generated.
RST	11	E3	М	0	This is the qualified active-low reset signal. RST has a fail-safe open-drain output.
RTS	35	J5	U	0	Request to send is an active-low signal. When active, RTS informs the modem of the data set that the UART is ready to receive data. RTS is set to its active state by setting the RTS modem control register bit and is set to its inactive (high) state either as a result of a reset, doing loop-mode operation, or by resetting bit 1 (RTS) of the MCR.
SA0 SA1 SA2 SA3 SA4 SA5 SA6 SA7	53 55 56 57 58 59 61	H9 H10 G9 G10 G8 F10 F8 E9	S	I	When SSAB is high, this is the subsystem address bus and SAD (7–0) is the subsystem data bus. When SSAB is low, this bus is not used and SAD(7–0) is the subsystem multiplexed address/data bus.
SA8	24	J1	S	ı	Address bit 8 is bit 8 of the subsystem address bus.
SAD0 SAD1 SAD2 SAD3 SAD4 SAD5 SAD6 SAD7	25 23 20 19 18 17 15	K1 H2 G2 G1 G4 F4 F2 F1	S	I/O	Subsystem address/data 7–0. This is a multiplexed bidirectional address/data bus to the attribute-memory DPRAM and CCRs when SSAB is low. This becomes a bidirectional data bus when SSAB is high.
SELZ/Ī	28	J3	S	I	Select Zilog or Intel mode. SELZ/Ī is used to select between a Zilog-like or Intel-like microcontroller. 1 = Zilog, 0 = Intel.
SIN	33	H4	U	I	Serial data input. SIN moves information from the communication line or modem to the TL16PC564B UART receiver circuits. Data on the serial bus is disabled when operating in the loop mode.
SOUT	45	J7	U	0	Serial out. SOUT is the composite serial data output to a connected communication device. SOUT is set to the marking (logic 1) state as a result of a reset.
SSAB	3	C2	S	I	Separate subsystem address bus. SSAB is used to select between a multiplexed address/data bus subsystem interface (SSAB = 0) and a subsystem interface with separate address and data buses (SSAB = 1). This signal has an internal pulldown resistor.
STSCHG	74	B10	Н	0	Status change. STSCHG is an optional active-low output signal used to alert the host that a subsystem write to attribute memory has occurred. This signal has an open-drain output.
TESTOUT	70	D9	М	0	This is a production test output.
UARTCLK	51	J9	М	0	UART clock. UARTCLK is a clock output whose frequency is determined by the frequency on XIN and the divisor value on the PGMCLK register.
VCC	10,21,22,36, 47,52,60, 72,86,97	E2,G3,H1, H5,K8,J10, F9,C10,C6,A 3	М		3.3-V or 5-V supply voltage

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#### **Terminal Functions**

	TERMINAL		INTER-		DESCRIPTION
NAME	PZ NO.	GGM NO.	FACE†	1/0	DESCRIPTION
WE	89	A5	Н	_	Write enable. WE is an active-low input signal used for strobing attribute-memory write data into the card. This signal has an internal pullup resistor
WR(R/W)	31	J4	S	I	Write or read/write enable. $\overline{WR}(R/\overline{W})$ is the active-low write enable in the Intel mode and read/write in the Zilog mode.
XIN	42	G6	М	I	Crystal input. XIN is a clock input divided internally based on the PGMCLK register value, then used as the primary UART clock input.
VTEST	2	B1	М	I	VTEST is an active-high production test input with an internal pulldown resistor. It can be left open or tied to ground.

<sup>†</sup> Host = H, Subsystem = S, UART = U, Miscellaneous = M

### detailed description

#### reset-validation circuit

A reset-validation circuit has been implemented to qualify the active-high RESET input. At power up, the level on the  $\overline{RST}$  output is unknown. Whenever RESET is stable for at least eight ARBCLKIs,  $\overline{RST}$  reflects the inverted state of that stable value of RESET. Any changes on RESET must be valid for eight ARBCLKI clocks before the change is reflected on  $\overline{RST}$ . This 8-clock filter provides needed hysteresis on the master reset input.  $\overline{RST}$  is driven by a low-noise, open-drain, fail-safe output buffer.

### host CPU memory map

The host CPU attribute memory space is mapped as follows:

Host CPU Address Bits 9-1 (HA0 = 0)	Attribute Memory Space
0 – 255	CIS
256	CCR0
257	CCR1
258	CCR2
259	CCR3
260	CCR4
261	CCR5
262	CCR6
263	CCR7

The host CPU I/O space is mapped as follows:

A dd = 000	Mada	(hav)
Address	Mode	(hex)

<b>Normal Mode</b>	COM1	COM2	COM3	COM4	I/O Space
$0 (DLAB = 0)^{\dagger}$	3F8	2F8	3E8	2E8	UART receiver buffer register (RBR) – read only
$0 (DLAB = 0)^{\dagger}$	3F8	2F8	3E8	2E8	UART transmitter holding register (THR) – write only
$0 (DLAB = 1)^{\dagger}$	3F8	2F8	3E8	2E8	UART divisor latch LSB (DLL)
1 (DLAB = 0) $^{\dagger}$	3F9	2F9	3E9	2E9	UART interrupt enable register (IER)
1 (DLAB = 1) $^{\dagger}$	3F9	2F9	3E9	2E9	UART divisor latch MSB (DLM)
2	3FA	2FA	3EA	2EA	UART interrupt identification register (IIR) – read only
2	3FA	2FA	3EA	2EA	UART FIFO control register (FCR) – write only
3	3FB	2FB	3EB	2EB	UART line control register (LCR)
4	3FC	2FC	3EC	2EC	UART modem control register (MCR) – bit 5 read only
5	3FD	2FD	3ED	2ED	UART line status register (LSR)
6	3FE	2FE	3EE	2EE	UART modem status rgister (MSR)
7	3FF	2FF	3EF	2EF	UART scratch register (SCR)

† DLAB is bit 7 of the line control register (LCR).



#### subsystem memory map

The subsystem attribute memory space is mapped as follows:

Subsystem Address Bits 8–0	Attribute Memory Space
0 – 255	CIS
256	CCR0
257	CCR1
258	CCR2
259	CCR3
260	CCR4
261	CCR5
262	CCR6
263	CCR7

The subsystem control space is mapped as follows:

Subsystem Address Bits 8–0	Control Space
272	Control Register
288	PGMCLK Register (write only)

The subsystem UART space is mapped as follows:

Subsystem Address Bits 8–0	UART Space
304	UART MCR bit 5 (write only)
304	UART DLL (read only)
305	UART IER (read only)
306	UART FCR (read only)
307	UART LCR (read only)
308	UART MCR (read only)
309	UART LSR (read only)
310	UART MSR (read only)
311	UART DLM (read only)
320	UART transmitter FIFO (read only)†
320	UART receiver FIFO (write only) <sup>†</sup>

<sup>†</sup>Only when serial bypass mode is enabled

#### host CPU/attribute-memory interface

The host CPU/attribute-memory interface is comprised of one port of the internal DPRAM, the eight CCRs, and necessary control circuitry. Signals HA0 and  $\overline{\text{CE1}}$  are gated together internally so that the output of the gate is low when both signals have been asserted by the host CPU. This output is combined with  $\overline{\text{REG}}$  and the decoded address, HA(9–1), to provide the chip enable for the DPRAM and CCRs. This composite chip enable in combination with  $\overline{\text{WE}}$  or  $\overline{\text{OE}}$  allows writes and reads to the DPRAM and CCRs.

#### subsystem/attribute-memory interface

The subsystem/attribute-memory interface is comprised of the second port of the internal DPRAM, the eight CCRs, and necessary control circuitry. When in multiplexed mode (SSAB = 0), the combination of signals SELZ/ $\overline{l}$  and ALE( $\overline{AS}$ ) allows either a positive-pulse Intel or a negative-pulse Zilog address latch-enable strobe to latch the address on SA8 and SAD(7–0). When in the Zilog mode (SELZ/ $\overline{l}$  high), the combination of read/write [ $\overline{WR}(R/\overline{W})$ ], data strobe [ $\overline{RD}(\overline{DS})$ ], and decoded address allows ZBUS access. When in the Intel configuration (SELZ/ $\overline{l}$  low), the combination of read [ $\overline{RD}(\overline{DS})$ ], write [ $\overline{WR}(R/\overline{W})$ ], and decoded address allows IBUS access.



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When in nonmultiplexed mode (SSAB = 1), SA(7–0) become the lower-order address bits, SAD(7–0) are strictly the bidirectional data bus, and  $ALE(\overline{AS})$  is nonfunctional. All other interface signals function the same.

SSAB	SELZ/Ī	RD(DS)	$\overline{WR}(R/\overline{W})$	Address	Operation
0	0	0	1	SA8, SAD(7-0)	Intel read
0	0	1	0	SA8, SAD(7-0)	Intel write
0	1	0	1	SA8, SAD(7-0)	Zilog read
0	1	0	0	SA8, SAD(7-0)	Zilog write
1	0	0	1	SA(8-0)	Intel read
1	0	1	0	SA(8-0)	Intel write
1	1	0	1	SA(8-0)	Zilog read
1	1	0	0	SA(8-0)	Zilog write

### attribute-memory arbitration

Arbitration for the attribute memory is necessary whenever there is simultaneous access to the same DPRAM or CCR address for the conditions of:

- Host CPU read and subsystem write
- Host CPU write and subsystem read
- Host CPU write and subsystem write

If arbitration were not provided, attribute-memory data would be corrupted and invalid data read due to uncontrolled access to the same DPRAM or CCR address.

The arbitration control circuitry synchronizes the asynchronous accesses of the host CPU and subsystem to the DPRAM and CCR and controls the access based on the pending host CPU and subsystem attribute-memory operation. The synchronizing and control circuitry needs a clock called the arbitration clock. The external clock (ARBCLKI) goes through a programmable divider and can be divided by one, two, four, or eight to generate a clock frequency within an allowed range for the arbitration logic to work correctly. The output of this frequency divider is named ARBCLKO. The programmable divider bits are defined as follows:

ARBPGM1	ARBPGM0	INTERNAL ARITRATION CLOCK
L	L	ARBCLKI/1
L	Н	ARBCLKI/2
Н	L	ARBCLKI/4
Н	Н	ARBCLKI/8

The upper period limit of ARBCLKO is N/6, where N (ns) is the shortest of the two attribute-memory accesses, host CPU or subsystem. The lower period limit of ARBCLKO is based on the DPRAM specifications at the supply voltage used:

5 V = 14-ns clock cycle (71 MHz)

3 V = 26-ns clock cycle (38.5 MHz)

For any arbitration condition, attribute-memory access is controlled to ensure valid data is read for a port that is doing a read operation and valid data is written for a port that is doing a write operation. When both the host CPU and subsystem are performing simultaneous write operations to the same address, the host CPU is allowed to write and the subsystem write is ignored.

#### host CPU/subsystem handshake

Two signals are provided for handshaking between the host CPU and the subsystem. The active-high IRQ signifies to the subsystem that the host CPU has written data into attribute memory. The subsystem can clear IRQ by writing a 1 to bit 6 of the subsystem control register. The active-low STSCHG signifies to the host CPU



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that the subsystem has written data to attribute memory provided bit 2 of the subsystem control register (STSCHG enable) is high. The host CPU can clear STSCHG by reading any location in attribute memory. The control of these signals is synchronized to ARBCLKO to ensure there are no false assertions/deassertions.

There is additional arbitration performed for instances of simultaneous assertion/deasseration of IRQ or STSCHG. When a subsystem write and host CPU read occurs simultaneously, STSCHG may be briefly deasserted prior to being asserted, but the write ultimately wins arbitration. When the host CPU read occurs more than one-half an arbitration clock after the subsystem write, STSCHG is deasserted. IRQ is arbitrated in a similar fashion.

#### host CPU/UART interface

The UART select is derived from either host CPU address information or logic levels on  $\overline{\text{CE1}}$ ,  $\overline{\text{CE2}}$  and  $\overline{\text{REG}}$ . In the address mode, host CPU address bits HA9, HA7, HA6, HA5, and HA3 are combined with conditional derivatives of HA4 and HA8 to select the UART (HA4 and HA8 select COM ports 1–4 based on settings in the subsystem control register).  $\overline{\text{CE1}}$  and  $\overline{\text{CE2}}$  are combined such that either of these two signals in combination with  $\overline{\text{REG}}$  enable the UART in the event that these signals are present. In the event that  $\overline{\text{CE1}}$  or  $\overline{\text{CE2}}$  are not present, the UART must be accessed in the address mode previously described. The UART select in conjunction with  $\overline{\text{IORD}}$  and  $\overline{\text{IOWR}}$  allows host CPU accesses to the UART. Host CPU address bits HA2–HA0 are decoded to select which UART register is to be accessed.

All UART registers remain intact with the exception of the FIFO control register (FCR) and the modem-control register (MCR). The FCR (host CPU write-only address 2) bits 4 and 5 in conjunction with EXTEND control RTS operation and FIFO depth as follows:

BIT 5	BIT 4	EXTEND	RTS OPERATION	FIFO DEPTH
X	Х	Н	Normal	16 bytes
0	0	L	Normal	16 bytes
0	1	L	Auto	16 bytes
1	0	L	Normal	64 bytes
1	1	L	Auto	64 bytes

FCR bit 5 high and EXTEND low redefine the receiver FIFO trigger levels set by FCR bits 6 and 7 as follows:

BIT 7	BIT 6	TRIGGER LEVEL
0	0	1
0	1	16
1	0	32
1	1	56

The MCR (host CPU address 4) bit 5 is read only. Bit 5 is controlled by the subsystem to enable (high) the auto-CTS mode of operation

#### subsystem/UART interface

The UART provides a serial-communications channel to the subsystem with enhanced  $\overline{\text{RTS}}$  control (see auto- $\overline{\text{RTS}}$  description). This channel is capable of operating at 115 kbps and is the main communications channel to the subsystem (refer to the TL16C550 specification for the detailed description of the serial-communications channel).

Many of the UART registers have been mapped into the subsystems memory space as read only. In addition, MCR bit 5 (subsystem address 130 hex) is controlled by the subsystem to enable (high) auto-CTS. The subsystem can read the MCR at address 134 hex. When reading the FCR (subsystem address 132 hex), bits 1 and 2 are always high, and bits 4 and 5 are low only when EXTEND is low and the host CPU has set them high (64-byte FIFOs and auto-RTS enabled) (refer to the subsystem memory map).



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### subsystem control register

The subsystem control register is an 8-bit register located at subsystem address 110 (hex). This register is programmed based on host CPU configuration information and has a default selection of COM2 after a valid reset. The bit definitions are as follows (0 = LSB):

Bits 0 and 1 define which host COM port the UART is connected to when the chip is in the address mode. COM2 is the default (power-up) condition.

BIT 1	BIT 0	COM PORT
0	0	COM1
1	0	COM2
0	1	COM3
1	1	COM4

Bit 2 is a host CPU interrupt-enable bit. When bit 2 is set, any subsystem attribute-memory write cycle causes STSCHG to be asserted. Bit 2 is cleared after a valid reset.

Bit 3 enables or disables address-mode selection as described in the host CPU/UART interface description. Bit 3 is cleared (disabling the address mode) after a valid reset.

Bits 4 and 5 together ensure adherence to PCMCIA power-up requirements. At power up, the card must operate as a memory card and all host CPU I/O operations must be disabled. IREQ, which doubles as the host CPU READY/BUSY line, powers up low, indicating that the memory card is busy. Once the subsystem initializes attribute memory, the subsystem sets bit 4 to indicate that the memory card is ready. Then bit 5 is reset, changing the configuration from a memory card to an I/O card, enabling host CPU UART accesses. IREQ now becomes the host CPU interrupt-request line.

BIT 5	BIT 4	CONFIGURATION
1	0	Memory card, I/O operation (UART) disabled; $\overline{\text{IREQ}}$ is low, indicating card is busy (power-up and reset condition)
1	1	Memory card, I/O operation (UART) disabled; IREQ is high, indicating card is ready
0	Х	I/O card, I/O operation (UART) enabled; IREQ now functions as the host CPU interrupt-request line

Bit 6 is a self-clearing bit that resets the subsystem IRQ signal. Writing a 1 to this location clears the IRQ interrupt.

Bit 7 enables or disables serial-bypass mode as described in the subsystem serial-bypass-mode description. Bit 7 is cleared (disabling serial-bypass mode) after a valid reset.

### subsystem PGMCLK register/divide-by-n circuit

The subsystem PGMCLK register is a 6-bit write-only register located at address 120 hex and is used to select the divisor of the divide-by-n-and-a-half circuitry. Any write to this register generates a reset to the UART and the divide-by-n circuitry.

The divide-by-n circuitry allows for a divisor from 0 to 31.5 in 0.5 increments (PGMCLK0 is the half bit). The divided clock output drives the UART clock input and can be seen on UARTCLK. The UART requires a clock with a minimum high pulse duration of 50 ns and a minimum low pulse duration of 50 ns (10-MHz maximum operating frequency). A programmed divisor between 2 and 7.5 drives the UART clock low for one XIN clock cycle for integer divisors and one-and-a-half XIN clock cycles for integer-plus-a-half divisors. A programmed divisor of eight or greater drives the UART clock low for four XIN clock cycles for integer divisors. A



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four-and-a-half XIN clock cycles for integer-plus-a-half divisors. Based on the above parameters, the acceptable XIN/divisor combinations can be derived. The precision of the programmable clock generator for integer-plus-a-half divisors depends on the closeness to a 50% duty cycle for the XIN input clock.

#### NOTE

With a divisor less than or equal to 8 (whole number), the UART clock will have a low pulse equal to one clock cycle of the XIN clock. Caution should be used as noted in the following example.

A 20 MHz clock period yields 50 ns total, including rise time and fall time, if a divisor of less than or equal to 8 (whole number) is used. This provides a total down period less than 50 ns to the UART clock, which is less than that which is required for the UART to function properly.

Caution should be used when selecting the XIN and divisor combination.

PGMCLK(0-5) VALUE (HEX)		RESULT
0	(0)	No clock (driven high)
0.5	(1)	Divide-by-1
1	(2)	Divide-by-1
1.5	(3)	Divide-by-1
2	(4) to 31.5 (3F)	Divide-by-2 to divide-by-31.5

### subsystem serial-bypass mode

The optional serial-bypass mode is implemented to allow a high-throughput path to/from the host CPU. When this mode is enabled and subsystem control register bit 7 is high, the serial portion of the UART is bypassed and the subsystem has direct parallel access to the receiver FIFO (write address 140 hex) and the transmitter FIFO (read address 140 hex). All host CPU interrupts operate normally except for receiver parity, framing, and breaking interrupts.

### auto-CTS operation

The optional <u>auto-CTS</u> operation is implemented so that the host CPU cannot overflow the modem receive buffer. Auto-CTS operation is enabled when the subsystem sets MCR (subsystem address 130 hex) bit 5 high. When enabled, deactivating CTS (high) halts the transmitter section of the UART after it completes the current transfer. Once CTS is reactivated (low) by the modem, transfers resume. Interrupt operation is not affected by enabling auto-CTS.

#### auto-RTS operation

The optional auto-\$\overline{RTS}\$ operation is implemented so that the subsystem cannot overflow the receiver FIFO. Auto-\$\overline{RTS}\$ operation is enabled when FCR bit 4 is high and \$\overline{EXTEND}\$ is low and operates independently from the trigger-level circuitry. In the 16-byte FIFO mode, the RTS bit in the modem-control register (bit 1) clears when 14 characters are in the receive FIFO. This action causes \$\overline{RTS}\$ to go high (inactive). In the 64-byte FIFO mode, the MCR RTS bit clears when 56 characters are in the receiver FIFO. Interrupt operation is not affected and operates the same way in either auto-\$\overline{RTS}\$ or nonauto-\$\overline{RTS}\$ mode. When enabled, a receive-data-available interrupt occurs after the trigger level is reached. The MCR RTS bit must then be set by the host CPU after the receiver FIFO has been read.



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### power consumption

The TL16PC564B has low power consumption under the following conditions:

- 32-MHz signal on XIN
- Divide-by-n is set to give a 1.8432-MHz UARTCLK signal
- Nominal data
- V<sub>CC</sub> = 5 V

The current (I<sub>CC</sub>) and power consumption are 18 mA (typical) and 90 mW (typical), respectively. These current and power figures fluctuate with changes in the above conditions.

### absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V <sub>CC</sub>	–0.5 V to 6 V
Input voltage range, V <sub>I</sub> (standard)	0.5 V to V <sub>CC</sub> + 0.5 V
Input voltage range, V <sub>I</sub> (fail safe)	
Output voltage range, VO (standard)	0.5 V to V <sub>CC</sub> + 0.5 V
Output voltage range, VO (fail safe)	
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (see Note 1)	
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) (see Note 2)	±20 mA
Operating free-air operating temperature range, T <sub>A</sub>	0°C to 70°C
Storage temperature range, T <sub>Stg</sub>	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. Applies for external input and bidirectional buffers. V<sub>I</sub> > V<sub>CC</sub> does not apply to fail-safe pins.
  - 2. Applies for external output and bidirectional buffers. VO > VCC does not apply to fail-safe pins.

### recommended operating conditions

### low voltage (3.3 V nominal)

		MIN	NOM	MAX	UNIT
Complementage V	TL16PC564B	3	3.3	3.6	V
Supply voltage, V <sub>CC</sub>	TL16PC564BLV	2.7	3	3.3	V
Input voltage, V <sub>I</sub>	•	0		Vcc	V
High-level input voltage (CMOS), V	IH (see Note 3)	0.7V <sub>CC</sub>			V
Low-level input voltage (CMOS), V	L (see Note 3)			0.3V <sub>CC</sub>	V
Output voltage, VO (see Note 4)		0		VCC	V
High-level output current, IOH	All outputs except RST, STSCHG, OUT1, OUT2 (see Note 5)			1.8	mA
Low-level output current, IOI	All outputs except RST			3.2	mA
Low-level output current, IOF	RST			6.4	ША
Input transition time, t <sub>t</sub>		0		25	ns
Operating free-air temperature rang	ge, T <sub>A</sub>	0	25	70	°C
Junction temperature range, T <sub>J</sub> (se	e Note 6)	0	25	115	°C

- NOTES: 3. Meets TTL levels, VIHmin = 2 V and VILmax = 0.8 V on nonhysteresis inputs
  - 4. Applies for external output buffers
  - 5. RST, STSCHG, OUT1, and OUT2 are open-drain outputs, so IOH does not apply.
  - 6. These junction temperatures reflect simulation conditions. Absolute maximum junction temperature is 150°C. The customer is responsible for verifying junction temperature.



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### standard voltage (5 V nominal)

		MIN	NOM	MAX	UNIT
Supply voltage, V <sub>CC</sub>		4.75	5	5.25	V
Input voltage, V <sub>I</sub>		0		VCC	V
High-level input voltage (CMOS), V	ΊΗ	0.7V <sub>CC</sub>			V
Low-level input voltage (CMOS), V	IL			0.2V <sub>CC</sub>	V
Output voltage, V <sub>O</sub> (see Note 4)		0		VCC	V
High-level output current, IOH	All outputs except RST, STSCHG, OUT1, OUT2 (see Note 5)			4	mA
I am laval autout aumant I	All outputs except RST			4	
Low-level output current, IOL	RST			8	mA
Input transition time, t <sub>t</sub>		0		25	ns
Operating free-air temperature range, T <sub>A</sub>		0	25	70	°C
Junction temperature range, T <sub>J</sub> (see	ee Note 6)	0	25	115	°C

NOTES: 4. Applies for external output buffers

- 5. RST, STSCHG, OUT1, and OUT2 are open-drain outputs, so IOH does not apply.
- 6. These junction temperatures reflect simulation conditions. Absolute maximum junction temperature is 150°C. The customer is responsible for verifying junction temperature.

### electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

### low voltage (3.3 V nominal)

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Vон	High-level output voltage	I <sub>OH</sub> = rated	V <sub>CC</sub> -0.55		V
VOL	Low-level output voltage	I <sub>OL</sub> = rated		0.5	V
V <sub>IT+</sub>	Positive-going input threshold voltage (see Note 7)			0.7 V <sub>CC</sub>	V
$V_{IT-}$	Negative-going input threshold voltage (see Note 7)		0.3 V <sub>CC</sub>		V
V <sub>hys</sub>	Hysteresis (V <sub>IT+</sub> – V <sub>IT-</sub> ) (see Note 7)		0.1 V <sub>CC</sub>	0.3 V <sub>CC</sub>	V
loz	3-state-output high-impedance current (see Note 8)	$V_I = V_{CC}$ or GND		±10	μΑ
IլL	Low-level input current (see Note 9)	V <sub>I</sub> = GND		-1	μΑ
lн	High-level input current (see Note 10)	VI = VCC		1	μΑ

#### standard voltage (5 V nominal)

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Vон	High-level output voltage	I <sub>OH</sub> = rated	V <sub>CC</sub> -0.8		V
VOL	Low-level output voltage	I <sub>OL</sub> = rated		0.5	V
V <sub>IT+</sub>	Positive-going input threshold voltage (see Note 7)			0.7 V <sub>CC</sub>	V
VIT-	Negative-going input threshold voltage (see Note 7)		0.2 V <sub>CC</sub>		V
$V_{hys}$	Hysteresis (V <sub>IT+</sub> – V <sub>IT</sub> –) (see Note 7)		0.1 V <sub>C</sub> C	0.3 V <sub>CC</sub>	V
loz	3-state-output high-impedance current (see Note 8)	$V_I = V_{CC}$ or GND		±10	μΑ
I <sub>IL</sub>	Low-level input current (see Note 9)	V <sub>I</sub> = GND		-1	μΑ
lιΗ	High-level input current (see Note 10)	V <sub>I</sub> = V <sub>CC</sub>		1	μΑ

NOTES: 7. Applies for external input and bidirectional buffers with hysteresis

- 8. The 3-state or open-drain output must be in the high-impedance state.
- 9. Specifications only apply with pullup terminator turned off.
- 10. Specifications only apply with pulldown terminator turned off.



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### XIN timing requirements over recommended operating free-air temperature range (see Figure 1)

		TEST CONDITIONS	MIN	MAX	UNIT
	land for successive	V <sub>CC</sub> = 3.3 V, See Note 11		50	NAL I-
Input frequency		V <sub>CC</sub> = 5 V		60	MHz
	Cycle time, XIN	V <sub>CC</sub> = 3.3 V, See Note 11	20		
t <sub>c1</sub>		V <sub>CC</sub> = 5 V	16.7		ns
		$V_{CC} = 3.3 \text{ V},$ See Note 11	10		
tw1	Pulse duration, XIN clock high	V <sub>CC</sub> = 5 V	8		ns
	B. I. S. WIN I I I	V <sub>CC</sub> = 3.3 V, See Note 11	10		
t <sub>w2</sub>	Pulse duration, XIN clock low	V <sub>CC</sub> = 5 V	8		ns

NOTE 11: TL16PC564BLV device tested at  $V_{CC} = 3 \text{ V}$ .

### clock switching characteristics over recommended operating free-air temperature range (see Figure 1)

	PARAMETER	TEST CONDITIONS	MIN MAX	UNIT
	Delevision of VINA to HARTCHIA	V <sub>CC</sub> = 3.3 V, See Note 11	14	
<sup>t</sup> d1	Delay time, XIN↑ to UARTCLK↑	V <sub>CC</sub> = 5 V	8	ns
t 10	Delay time, XIN↓ to UARTCLK↓	V <sub>CC</sub> = 3.3 V, See Note 11	16	ns
t <sub>d2</sub>	Delay time, AIN to OAK I CLK	V <sub>CC</sub> = 5 V	10	115
+	Delevitime VINT to HADTOLK	$V_{CC} = 3.3 \text{ V},$ See Note 11	19.8	20
td3	Delay time, XIN↑ to UARTCLK↓	V <sub>CC</sub> = 5 V	13	ns
4	Delevision of VINA to HARTCHIA	V <sub>CC</sub> = 3.3 V, See Note 11	20.6	20
t <sub>d4</sub>	Delay time, XIN↑ to UARTCLK↑	V <sub>CC</sub> = 5 V	13.5	ns
4	Deleviting VIIII to HADTOUK	V <sub>CC</sub> = 3.3 V, See Note 11	21	
<sup>t</sup> d5	Delay time, XIN↓ to UARTCLK↑	V <sub>CC</sub> = 5 V	13.8	ns

NOTE 11: TL16PC564BLV device tested at  $V_{CC} = 3 \text{ V}$ .

### host CPU I/O read-cycle timing requirements over recommended ranges of operating free-air temperature and supply voltage (see Figure 2 and Note 12)

		MIN	MAX	UNIT
t <sub>h1</sub>	Hold time, HA(9–0) valid after IORD↑	20		ns
t <sub>h2</sub>	Hold time, REG↑ valid after IORD↑	0		ns
t <sub>w4</sub>	Pulse duration, IORD low	165		ns
t <sub>su1</sub>	Setup time, HA(9–0) valid before IORD↓	70		ns
t <sub>su2</sub>	Setup time, $\overline{CEx} \downarrow before \ \overline{IORD} \downarrow$	5		ns
t <sub>h3</sub>	Hold time, CEx↑ after IORD↑	20		ns
t <sub>h4</sub>	Hold time, HD(7–0) valid after IORD↑	0		ns
t <sub>su3</sub>	Setup time, REG↓ before IORD↓	5		ns
t <sub>d6</sub>	Delay time, HD(7–0) valid after IORD↓		100	ns

NOTE 12: The maximum load on INPACK is one low power shot with 50-pF total load. All timing is measured in nanoseconds.

### host CPU I/O read-cycle switching characteristics over recommended ranges of operating free-air temperature and supply voltage (see Figure 2 and Note 11)

	PARAMETER	MIN	MAX	UNIT
t <sub>d7</sub>	Delay time, INPACK↓ after IORD↓		45	ns
t <sub>d8</sub>	Delay time, INPACK↑ after IORD↑		45	ns

NOTE 12: The maximum load on INPACK is one low power Schottky (LSTTL) diode with 50-pF total load. All timing is measured in nanoseconds.



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### host CPU I/O write-cycle timing requirements over recommended ranges of operating free-air temperature and supply voltage (see Figure 3)

		MIN	MAX	UNIT
t <sub>su4</sub>	Setup time, HD(7–0) valid before IOWR↓	60		ns
t <sub>h5</sub>	Hold time, HA(9–0) valid after IOWR↑	20		ns
tw6	Pulse duration, IOWR low	165		ns
t <sub>su5</sub>	Setup time, HA(9–0) valid before <del>IOWR</del> ↓	70		ns
th6	Hold time, REG↑ after IOWR↑	0		ns
t <sub>su6</sub>	Setup time, CEx↓ before IOWR↓	5		ns
t <sub>h7</sub>	Hold time, CEx↑ after IOWR↑	20		ns
t <sub>su7</sub>	Setup time, REG↓ before IOWR↓	5		ns
th8	Hold time, HD(7–0) valid after IOWR↑	30		ns

### transmitter switching characteristics over recommended ranges of operating free-air temperature and supply voltage (see Figure 4)

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t <sub>d</sub> 9	Delay time, SOUT↓ after IOWR↑		8	24	Baud cycles
t <sub>d10</sub>	Delay time, IREQ↓ after SOUT↓		8	8	Baud cycles
<sup>t</sup> d11	Delay time, IREQ↓ after IOWR↑		16	32	Baud cycles
t <sub>d12</sub>	Delay time, IREQ↑ after IOWR↑	C <sub>L</sub> = 100 pF		140	ns
t <sub>d13</sub>	Delay time, IREQ↑ after IORD↑	C <sub>L</sub> = 100 pF		140	ns

### receiver switching characteristics over recommended ranges of operating free-air temperature and supply voltage (see Figure 5)

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t <sub>d14</sub>	Delay time, sample CLK↑ after RCLK↑			100	ns
<sup>t</sup> d15	Delay time, IREQ↓ after SIN↓			1	RCLK cycles
<sup>t</sup> d16	Delay time, IREQ↑ after IORD↑	C <sub>L</sub> = 100 pF		150	ns

### modem-control switching characteristics over recommended ranges of operating free-air temperature and supply voltage, $C_L = 100 \text{ pF}$ (see Figure 6)

	PARAMETER	MIN	MAX	UNIT
t <sub>d17</sub>	Delay time, RTS, DTR, OUT1, OUT2 ↓ or ↑ after IOWR↑		50	ns
<sup>t</sup> d18	Delay time, IREQ↓ after CTS, DSR, DCD↓		30	ns
t <sub>d19</sub>	Delay time, IREQ↑ after IORD↑		35	ns
t <sub>d20</sub>	Delay time, IREQ↓ after RI↑		30	ns



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### host CPU attribute-memory write-cycle timing requirements over recommended ranges of operating free-air temperature and supply voltage (see Figures 7 and 8)

		MIN	MAX	UNIT
t <sub>c2</sub>	Write cycle tlme, HA(9-0)	250		ns
t <sub>w8</sub>	Pulse duration, WE low	150		ns
t <sub>su8</sub>	Setup time, CEx↓ before WE↑	180		ns
t <sub>su9</sub>	Setup time, HA(9–0) before WE↑ (see Note 12)	180		ns
tsu10	Setup time, HA(9–0) before WE↓ and CEx↓(see Note 13)	30		ns
t <sub>su11</sub>	Setup time, <del>OE</del> ↑ before <del>WE</del> ↓	10		ns
t <sub>h</sub> 9	Hold time, HD(7–0) after WE↑	30		ns
t <sub>rec1</sub>	Recovery time, HA(9–0) after WE↑	30		ns
t <sub>su12</sub>	Setup time, HD(7–0) before WE↑	80		ns
th10	Hold time, <del>OE</del> ↓ after <del>WE</del> ↑	10		ns
t <sub>su13</sub>	Setup time, CEx↓ before WE↓	0		ns
th11	Hold time, CEx↑ after WE↑	20		ns

NOTE 13: The REG signal timing is identical to address signal timing.

### host CPU attribute-memory write-cycle switching characteristics over recommended ranges of operating free-air temperature and supply voltage (see Figure 7)

	PARAMETER	MIN	MAX	UNIT
tdis1	Disable time, HD(7–0) after WE↓		100	ns
tdis2	Disable time, HD(7–0) after OE↑		100	ns
t <sub>en1</sub>	Enable time, HD(7–0) after WE↑	5		ns
t <sub>en2</sub>	Enable time, HD(7–0) after OE↓	5		ns

## host CPU attribute-memory read-cycle timing requirements over recommended ranges of operating free-air temperature and supply voltage (see Figure 9)

		MIN	MAX	UNIT
t <sub>c3</sub>	Read cycle time	300		ns
t <sub>d22</sub>	Delay time, HD(7-0) after HA(9-0)		300	ns
t <sub>d23</sub>	Delay time, HD(7–0) after CEx↓		300	ns
t <sub>d24</sub>	Delay time, HD(7–0) after OE↓		150	ns
t <sub>h12</sub>	Hold time, HD(7–0) after HA(9–0)	0		ns
t <sub>su14</sub>	Setup time, $\overline{CE}x\downarrow$ before $\overline{OE}\downarrow$	0		ns
th13	Hold time, HA(9–0) after OE↑	20		ns
t <sub>su15</sub>	Setup time, HA(9–0) before OE↓	30		ns
th14	Hold time, CEx↑ after OE↑	20		ns

### host CPU attribute-memory read-cycle switching characteristics over recommended ranges of operating free-air temperature and supply voltage (see Figure 9)

	PARAMETER			UNIT
t <sub>dis3</sub>	Disable time, HD(7–0) after CEx↑		100	ns
t <sub>dis4</sub>	Disable time, HD(7–0) after OE↑		100	ns
t <sub>en3</sub>	Enable time, HD(7–0) after CEx↓	5		ns
t <sub>en4</sub>	Enable time, HD(7–0) after OE↓	5		ns



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### subsystem Intel-mode timing requirements (32 MHz) (see Figure 10)

INTEL SYMBOL	JEDEC SYMBOL		MIN	MAX	UNIT
tLHLL	tw11	Pulse duration, ALE high	48		ns
t <sub>AVLL</sub>	t <sub>su16</sub>	Setup time, SA8, SAD(7–0) valid to ALE low	21		ns
tPLLL	t <sub>d25</sub>	Delay time, CS low to ALE low	21		ns
tLLAX	th15	Hold time, SA8, SAD(7–0) valid after ALE↓	21		ns
tLLWL	t <sub>d26</sub>	Delay time, ALE low to WR low	16		ns
tLLRL	t <sub>d27</sub>	Delay time, ALE low to RD low	16		ns
tWHLH	t <sub>d28</sub>	Delay time, WR high to ALE high	21		ns
t <sub>AFRL</sub>	t <sub>d29</sub>	Delay time, SA8, SAD(7–0) in high-impedance state to RD low	0		ns
tRLRH	tw12	Pulse duration, RD low	120		ns
tWLWH	tw13	Pulse duration, WR low	120		ns
tRHAX	t <sub>d30</sub>	Delay time, RD high to SA8, SAD(7–0) active	48		ns
tWHDX	th16	Hold time, SA8, SAD(7-0) valid after WR high	48		ns
tWHPH	<sup>t</sup> d31	Delay time, WR high to CS high	21		ns
<sup>t</sup> RHPH	t <sub>d32</sub>	Delay time, RD high to CS high	21		ns
<sup>t</sup> PHPL	tw14	Pulse duration, CS high	21	·	ns

### subsystem Zilog-mode timing requirements (20 MHz) (see Figure 11)

ZILOG SYMBOL	JEDEC SYMBOL		MIN	MAX	UNIT
tdA(AS)	tsu17	Setup time, SA8 and SAD(7–0) valid before $\overline{\text{AS}}$ high	20		ns
tdAS(A)	t <sub>d33</sub>	Delay time, $\overline{\text{AS}}$ high to SA8 and SAD(7–0) invalid	35		ns
tdAS(DR)	t <sub>d34</sub>	Delay time, $\overline{AS}$ high to data in on SAD(7–0)		150	ns
t <sub>wAS</sub>	tw15	Pulse duration, AS low	35		ns
tdA(DS)	t <sub>d35</sub>	Delay time, SA8 and SAD(7–0) invalid to $\overline{\text{DS}}$ low	0		ns
twDS(read)	tw16	Pulse duration, DS low (read)	125		ns
twDS(write)	tw17	Pulse duration, DS low (write)	65		ns
tdDS(DR)	t <sub>d</sub> 36	Delay time, DS low to data in valid		80	ns
thDS(DR)	th17	Hold time, DS high to data in invalid	0		ns
<sup>t</sup> dDS(A)	th18	Hold time, DS high to data out invalid	20		ns
tdDS(AS)	t <sub>d37</sub>	Delay time, DS high to AS low	30		ns
tdDO(DS)	t <sub>d38</sub>	Delay time, SAD(7–0) (write data from μP) valid to DS low	10		ns
tdRW(AS)	t <sub>d39</sub>	Delay time, R/W active to AS high	20		ns

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### subsystem Intel nonmultiplexed timing requirements (see Figure 12)

		MIN	MAX	UNIT
t <sub>su18</sub>	Setup time, SA(8–0), CS valid to RD, WR↓	30		ns
tw18	Pulse duration, RD low	120		ns
tw19	Pulse duration, WR low	120		ns
t <sub>su19</sub>	Setup time, SAD(7–0) valid to WR↑	50		ns
ten4	Enable time, RD↓ to SAD(7–0) driving	5		ns
t <sub>d40</sub>	Delay time, $\overline{\text{RD}}$ to SAD(7–0) valid		105	ns
th19	Hold time, SA(8–0), CS valid after RD, WR↑	30		ns
th20	Hold time, SAD(7–0) valid after WR↑	30		ns
t <sub>dis3</sub>	Disable time, RD↑ to SAD(7–0) high impedance	5	15	ns

### subsystem Zilog nonmultiplexed timing requirments (see Figure 13)

		MIN	MAX	UNIT
t <sub>su20</sub>	Setup time, SA(8–0), $\overline{CS}$ , R/ $\overline{W}$ valid to $\overline{DS}\downarrow$ (write)	90		ns
t <sub>su21</sub>	Setup time, SA(8–0), $\overline{CS}$ , R/ $\overline{W}$ valid to $\overline{DS}\downarrow$ (read)	30		ns
t <sub>w20</sub>	Pulse duration, DS low (write)	65		ns
t <sub>w21</sub>	Pulse duration, DS low (read)	125		ns
t <sub>su22</sub>	Setup time, SAD(7–0) valid to DS↑	50		ns
t <sub>en5</sub>	Enable time, <del>DS</del> ↓ to SAD(7–0) driving	5		ns
<sup>t</sup> d41	Delay time, DS↓ to SAD(7–0) valid		105	ns
th21	Hold time, SA(8–0), CS, R/W valid after DS↑	30		ns
th22	Hold time, SAD(7–0), CS, R/W valid after DS↑	30		ns
<sup>t</sup> dis4	Hold time, DS↑ to SAD(7–0) high impedance	5	15	ns

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### ARBCLK switching characteristics over recommended operating free-air temperature range (see Figure 14)

		TEST CC	NDITIONS	MIN	MAX	UNIT	
	Cycle time internal arbitration alock (ARROLK) ARROCAN	$V_{CC} = 3.3 \text{ V},$	See Note 11	26	Note 14		
t <sub>c4</sub>	Cycle time, internal arbitration clock ( ARBCLKI ÷ ARBPGM)	V <sub>CC</sub> = 5 V		14	Note 14	ns	
	Cycle time exhitration alock	$V_{CC} = 3.3 \text{ V},$	See Note 11	26		20	
t <sub>c5</sub>	Cycle time, arbitration clock	$V_{CC} = 5 V$		14		ns	
4	Delevitime ARROLKIT to ARROLKOT (-4)	$V_{CC} = 3.3 \text{ V},$	See Note 11		13	20	
t <sub>d42</sub>	Delay time, ARBCLKI↑ to ARBCLK0↑ (÷1)	V <sub>CC</sub> = 5 V			7.3	ns	
	Delevitime ADDOLIGI to ADDOLIGO (.4)	$V_{CC} = 3.3 \text{ V},$	See Note 11		15.5		
t <sub>d43</sub>	Delay time, ARBCLKI↓ to ARBCLK0↓ (÷1)	$V_{CC} = 5 V$			10	ns	
	Delevitime ARROLKIT to ARROLKOT (+2)	$V_{CC} = 3.3 \text{ V},$	See Note 11		15.3		
t <sub>d44</sub>	Delay time, ARBCLKI↑ to ARBCLK0↑ (÷2)	$V_{CC} = 5 V$			8.8	ns	
	Delevitime ADDOLKIT to ADDOLKO ( 0)	$V_{CC} = 3.3 \text{ V},$	See Note 11		17.5		
<sup>t</sup> d45	Delay time, ARBCLKI↑ to ARBCLK0↓ (÷2)	V <sub>CC</sub> = 5 V			11	ns	
		$V_{CC} = 3.3 \text{ V},$	See Note 11		19.5		
<sup>t</sup> d46	Delay time, ARBCLKI↑ to ARBCLK0↑ (÷4)	$V_{CC} = 5 V$			11.5	ns	
	Delegation ADDOLKIT to ADDOLKO ( 4)	$V_{CC} = 3.3 \text{ V},$	See Note 11		21.5		
td47	Delay time, ARBCLKI↑ to ARBCLK0↓ (÷4)	V <sub>CC</sub> = 5 V			13.5	ns	
	Deleviting ADDOLKIT is ADDOLKOT ( a)	$V_{CC} = 3.3 \text{ V},$	See Note 11		22.7		
t <sub>d48</sub>	Delay time, ARBCLKI↑ to ARBCLK0↑ (÷8)	V <sub>CC</sub> = 5 V			13.5	ns	
	Delevitime ADDOLKIT to ADDOLKO ()	V <sub>CC</sub> = 3.3 V,	See Note 11		25		
t <sub>d49</sub>	Delay time, ARBCLKI↑ to ARBCLK0↓ (÷8)	V <sub>CC</sub> = 5 V			15.7	ns	

NOTES: 11. TL16PC564BLV device tested at 3 V.

### reset timing requirements over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted) (see Figure 15)

		TEST CON	NDITIONS	MIN	MAX	UNIT
t <sub>w22</sub>	Pulse duration, RESET active			8⋅t <sub>C5</sub>		ns
tw23	Pulse duration, RESET inactive			8⋅t <sub>C5</sub>		ns
	Polovičino APPOLICIÓ IN POT Loro	$V_{CC} = 3.3 \text{ V},$	See Note 11		10.4	
td50	Delay time, ARBCLKI↑ to RST low	V <sub>CC</sub> = 5 V			7.5	ns
	Delay time, ARBCLKI↑ to RST high impedance	$V_{CC} = 3.3 \text{ V},$	See Note 11		13.9 9.7	
td51	Delay time, ARBCLKIT to RST nign impedance	V <sub>CC</sub> = 5 V				ns

NOTE 11: TL16PC564BLV device tested at 3 V.

## subsystem interrupt-request timing requirements over recommended ranges of operating free-air temperature and supply voltage (see Figure 16)

		MIN	MAX	UNIT
t <sub>d52</sub>	Delay time, WE↑ to IRQ↑ (see Note 15)	2t <sub>C5</sub>	3t <sub>c5</sub>	ARBCLKI cycles
t <sub>d53</sub>	Delay time, SCR bit 6↑ to IRQ↓ (see Note 16)	t <sub>C5</sub>	2t <sub>C5</sub>	ARBCLKI cycles

NOTES: 11. TL16PC564BLV device tested at 3 V.

- 15. Synchronized to rising edge of ARBCLKI
- 16. Synchronized to falling edge of ARBCLKI



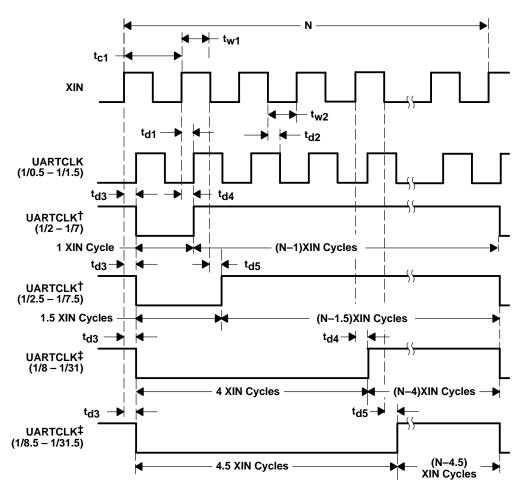
<sup>14.</sup>  $t_{C4}$  MAX = N/6, where N = shortest (in ns) of the two attribute-memory accesses, host CPU or subsystem.

### host CPU status change timing requirements over recommended ranges of operating free-air temperature and supply voltage (see Figure 17)

		MIN	MAX	UNIT
t <sub>d54</sub>	Delay time, subsystem write↑ to STSCHG↓ (see Note 14)	2t <sub>C5</sub>	3t <sub>C5</sub>	ARBCLKI cycles
t <sub>d55</sub>	Delay time, OE↓ to STSCHG high impedance (see Note 15)	t <sub>C5</sub>	2t <sub>C5</sub>	ARBCLKI cycles

NOTES: 15. Synchronized to rising edge of ARBCLKI

16. Synchronized to falling edge of ARBCLKI

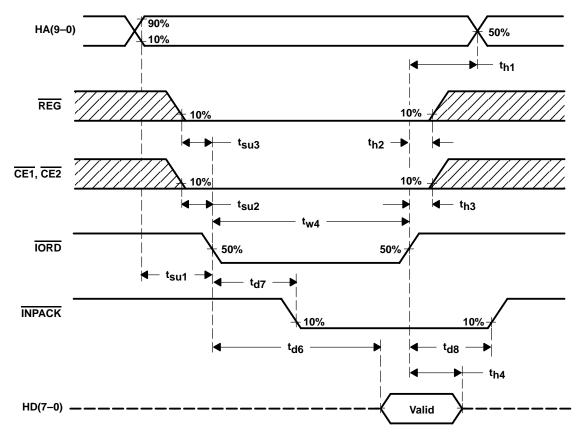


<sup>†</sup> The low portion of the UARTCLK cycle = 1 XIN cycle for PGMCLK integer values of 2 to 7 and 1.5 XIN cycles for PGMCLK noninteger values 2.5 to 7.5.

Figure 1. XIN Clock Timing Waveforms

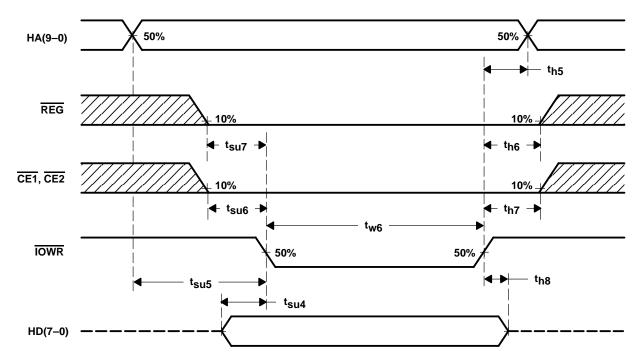


<sup>‡</sup> The low portion of the UARTCLK cycle = 4 XIN cycles for PGMCLK integer values of 8 to 31 and 4.5 XIN cycles for PGMCLK noninteger values 8.5 to 31.5.



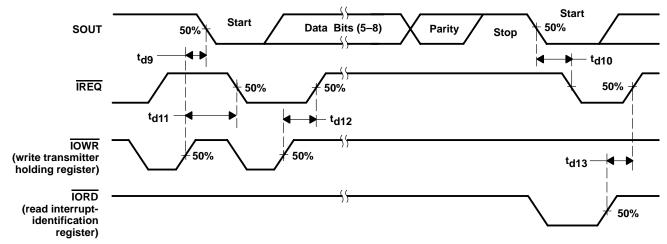
NOTE A: All timings are measured at the card. Skews and delays from the system driver/receiver to the card must be accounted for by the system design.

Figure 2. Host CPU I/O Read Timing Waveforms



NOTE A: All timings are measured at the card. Skews and delays from the system driver/receiver to the card must be accounted for by the system design.

Figure 3. Host CPU I/O Write Timing Waveforms



**Figure 4. Transmitter Timing Waveforms** 



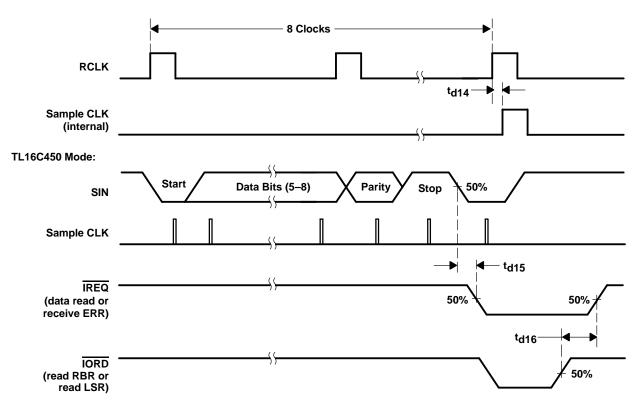
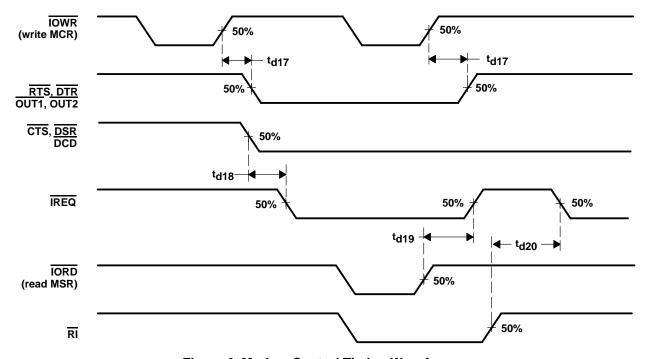
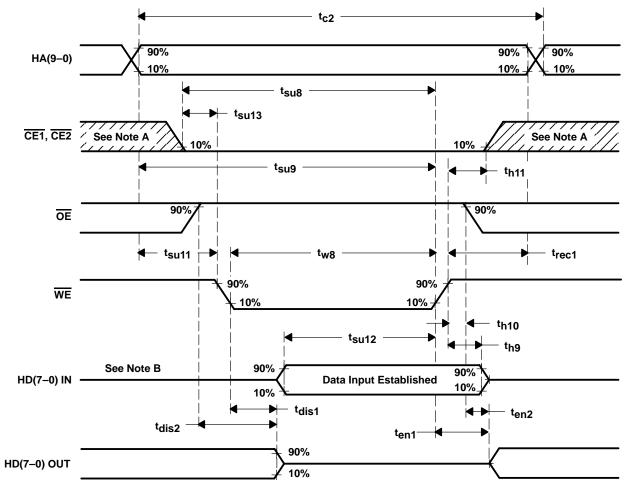


Figure 5. Receiver Timing Waveforms



**Figure 6. Modem Control Timing Waveforms** 



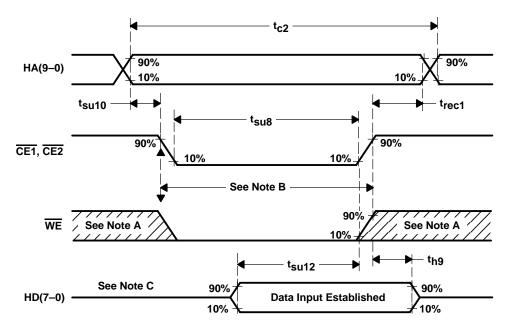


NOTES: A. The hatched portion may be either high or low.

B. When the data I/O terminal is in the output state, no signals should be applied to HD(7–0) by the system.

Figure 7. Host CPU Attribute-Memory Write Timing Waveforms (WE Control)

### PARAMETER MEASUREMENT INFORMATION

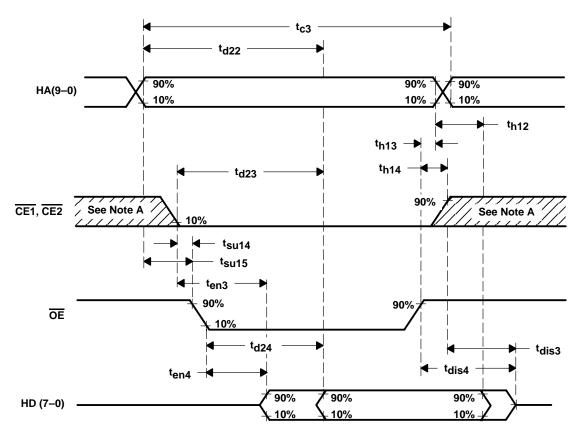


NOTES: A. The hatched portion may be either high (H) or low (L).

B. OE must be high (H).

C. When the data I/O terminal is in the output state, no signals should be applied to HD(7-0) by the system.

Figure 8. Host CPU Attribute-Memory Write Timing Waveforms (CE Control)



NOTE A: The shaded portion may be either high or low.

Figure 9. Host CPU Attribute-Memory Read Timing Waveforms

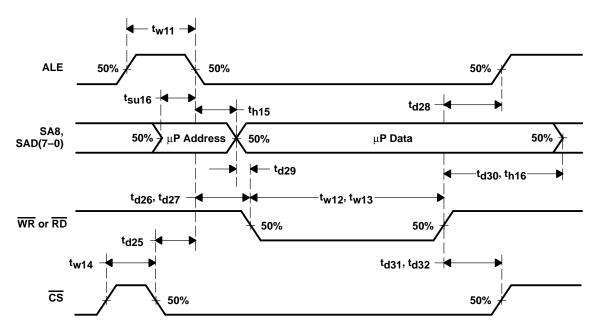
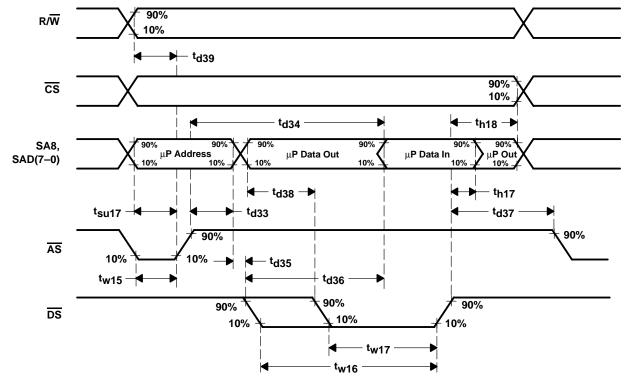


Figure 10. Subsystem Intel-Mode Timing Waveforms



NOTE A: Figures 10 and 11 are from the microprocessor perspective, not from the UART perspective.

Figure 11. Subsystem Zilog-Mode Timing Waveforms



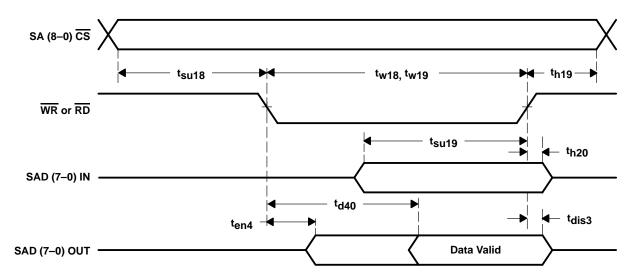


Figure 12. Subsystem Intel Nonmultiplexed Timing Waveforms

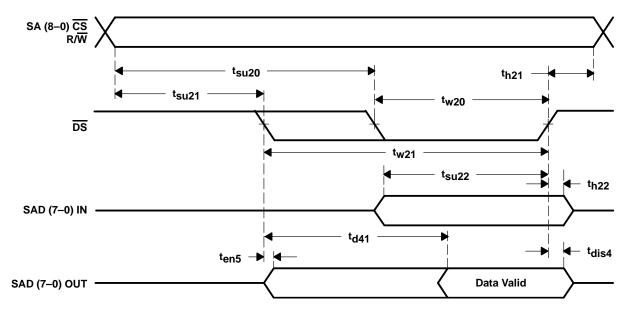


Figure 13. Subsystem Zilog Nonmultiplexed Timing Waveforms

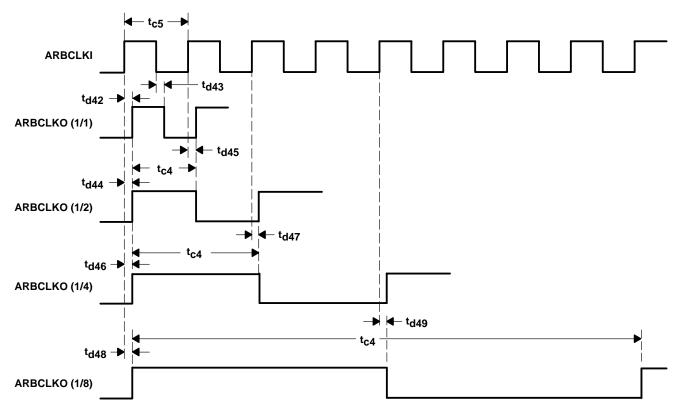
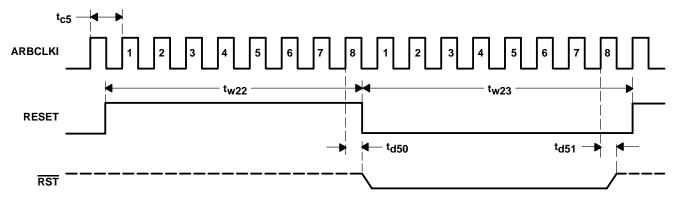


Figure 14. Arbitration-Clock Timing Waveforms



**Figure 15. Reset Timing Waveforms** 

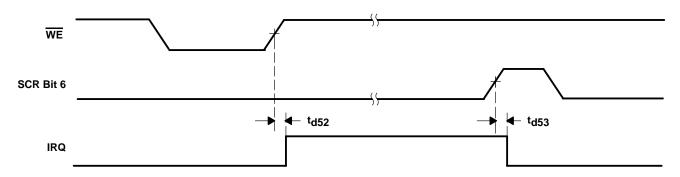


Figure 16. IRQ Timing Waveforms

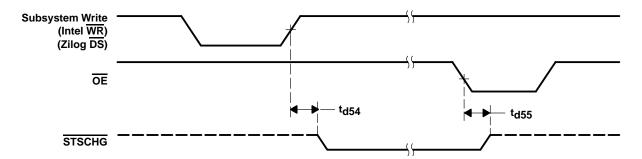
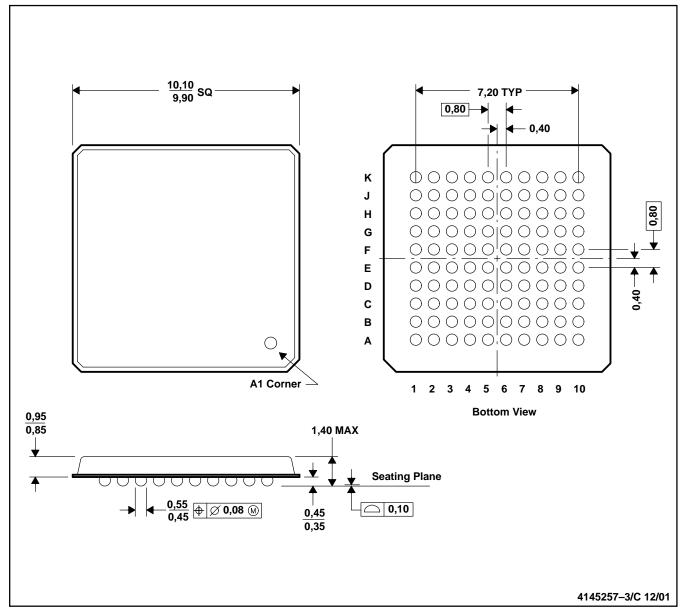


Figure 17. STSCHG Timing Waveforms

### **MECHANICAL DATA**

### GGM (S-PBGA-N100)

### **PLASTIC BALL GRID ARRAY**



NOTES: A. All linear dimensions are in millimeters.

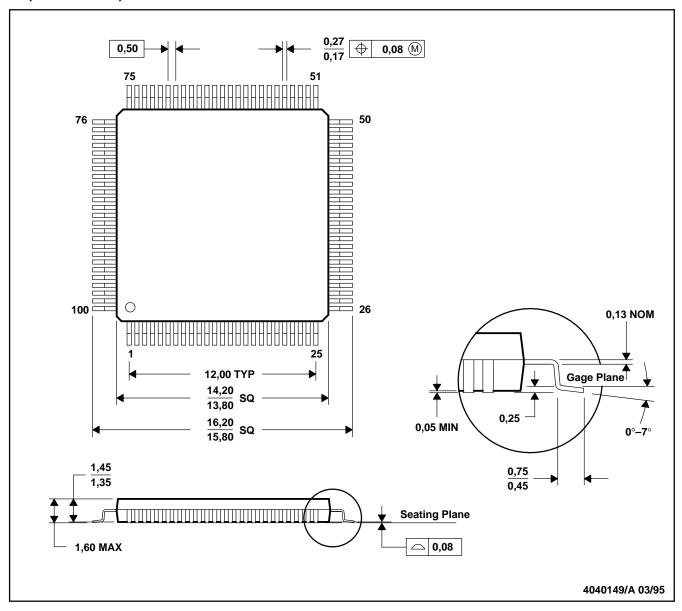
B. This drawing is subject to change without notice

C. MicroStar BGA configuration.

### **MECHANICAL DATA**

### PZ (S-PQFP-G100)

### PLASTIC QUAD FLATPACK



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Falls within JEDEC MO-136





com 10-Apr-2008

#### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins F	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TL16PC564BPZ	ACTIVE	LQFP	PZ	100	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
TL16PC564BPZG4	ACTIVE	LQFP	PZ	100	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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