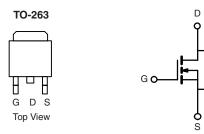
SQM110N08-05



Vishay Siliconix

Automotive N-Channel 75 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY					
V _{DS} (V)	75				
$R_{DS(on)}(\Omega)$ at $V_{GS} = 10 V$	0.0048				
I _D (A)	120				
Configuration	Single				



FEATURES

- Halogen-free According to IEC 61249-2-21
 Definition
- TrenchFET® Power MOSFET
- Package with Low Thermal Resistance
- AEC-Q101 Qualified^d
- 100 % $\rm R_g$ and UIS Tested
- Compliant to RoHS Directive 2002/95/EC



ORDERING INFORMATION				
Package	TO-263			
Lead (Pb)-free and Halogen-free	SQM110N08-05-GE3			

N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (To	_C = 25 °C, unless	s otherwise notec	l)		
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-Source Voltage		V _{DS}	75	V	
Gate-Source Voltage	V _{GS}	± 20			
Continuous Drain Current	T _C = 25 °C ^a	I	120	A	
	T _C = 125 °C	- I _D	106		
Continuous Source Current (Diode Conduction) ^a		I _S	120		
Pulsed Drain Current ^b	I _{DM}	480			
Single Pulse Avalanche Current	L = 0.1 mH	I _{AS}	66		
Single Pulse Avalanche Energy		E _{AS}	217	mJ	
Maximum Dawar Dissinctionh	T _C = 25 °C	D	375	W	
Maximum Power Dissipation ^b	T _C = 125 °C	P _D	125	vv	
Operating Junction and Storage Temperature Ran	ige	T _J , T _{stg}	- 55 to + 175	°C	

THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	LIMIT	UNIT		
Junction-to-Ambient	PCB Mount ^c	R _{thJA}	40	°C/W	
Junction-to-Case (Drain)		R _{thJC}	0.4	0/10	

Notes

- a. Package limited.
- b. Pulse test; pulse width \leq 300 $\mu s,\,duty\,cycle \leq$ 2 %.

c. When mounted on 1" square PCB (FR-4 material).

d. Parametric verification ongoing.

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PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static	-			1		<u> </u>	1	
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0, I_D = 250 \ \mu A$		75	-	-	v	
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} =	$V_{DS} = V_{GS}, I_{D} = 250 \ \mu A$		-	3.5	V	
Gate-Source Leakage	I _{GSS}	V _{DS} =	$V_{DS} = 0 V, V_{GS} = \pm 20 V$		-	± 100	nA	
		$V_{GS} = 0 V$	V _{DS} = 75 V	-	-	1		
Zero Gate Voltage Drain Current	I _{DSS}	$V_{GS} = 0 V$	V _{DS} = 75 V, T _J = 125 °C	-	-	50	μA	
		$V_{GS} = 0 V$	V _{DS} = 75 V, T _J = 175 °C	-	-	250		
On-State Drain Current ^a	I _{D(on)}	V _{GS} = 10 V	$V_{DS} \ge 5 V$	120	-	-	Α	
		$V_{GS} = 10 V$	I _D = 30 A	-	0.0039	0.0048	Ω	
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V	I _D = 30 A, T _J = 125 °C	-	-	0.0087		
		V _{GS} = 10 V	I _D = 30 A, T _J = 175 °C	-	-	0.0110	1	
Forward Transconductance ^{a, b}	9 _{fs}	V _{DS} = 15 V, I _D = 30 A		-	102	-	S	
Dynamic ^b								
Input Capacitance	C _{iss}			-	8158	10 200		
Output Capacitance	C _{oss}	$V_{GS} = 0 V$	V _{DS} = 25 V, f = 1 MHz	-	865	1085	pF	
Reverse Transfer Capacitance	C _{rss}			-	567	710		
Total Gate Charge ^c	Qg			-	141	212		
Gate-Source Charge ^c	Q _{gs}	V _{GS} = 10 V	$V_{DS} = 35 \text{ V}, \text{ I}_{D} = 110 \text{ A}$	-	32.6	-	nC	
Gate-Drain Charge ^c	Q _{gd}			-	39.1	-	1	
Gate Resistance	Rg		f = 1 MHz		1.2	1.9	Ω	
Turn-On Delay Time ^c	t _{d(on)}				19	29		
Rise Time ^c	t _r	$V_{DD} = 35 \text{ V}, \text{ R}_{\text{L}} = 0.32 \Omega$ $I_{D} \cong 110 \text{ A}, \text{ V}_{\text{GEN}} = 10 \text{ V}, \text{ R}_{\text{g}} = 1 \Omega$		-	31	47	ns	
Turn-Off Delay Time ^c	t _{d(off)}			-	55	83		
Fall Time ^c	t _f			-	15	23		
Source-Drain Diode Ratings and Chara	acteristics ^b					•		
Pulsed Current ^a	I _{SM}			-	-	480	Α	
Forward Voltage	V _{SD}	I _F = 100 A, V _{GS} = 0		-	0.9	1.5	V	

Notes

a. Pulse test; pulse width $\leq 300~\mu\text{s},~\text{duty}~\text{cycle} \leq 2~\%.$

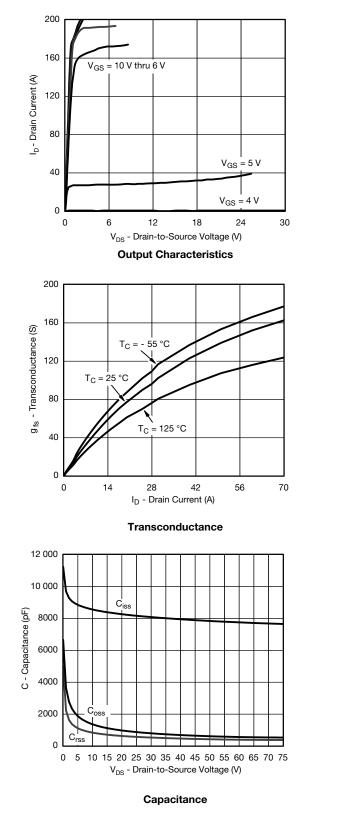
b. Guaranteed by design, not subject to production testing.

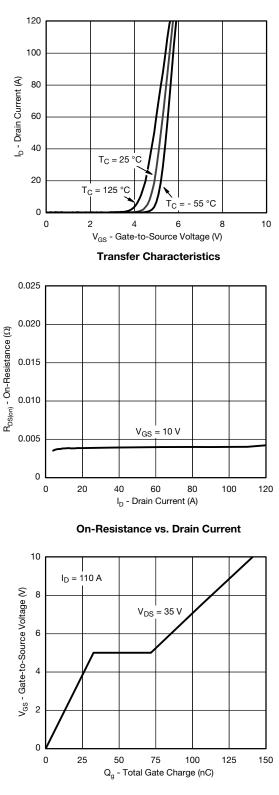
c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



TYPICAL CHARACTERISTICS ($T_A = 25 \text{ °C}$, unless otherwise noted)





Gate Charge

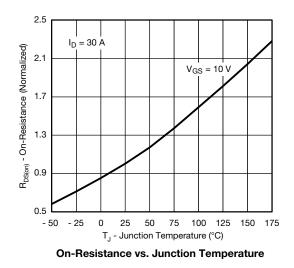
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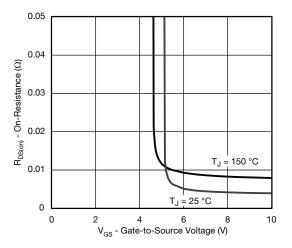
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Document Number: 64729

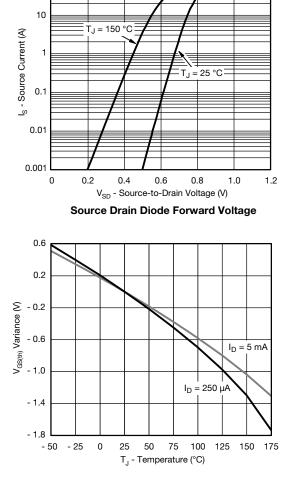


TYPICAL CHARACTERISTICS ($T_A = 25 \text{ °C}$, unless otherwise noted)



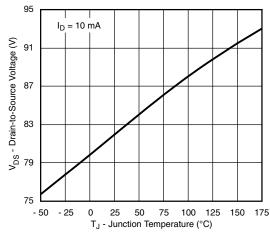


On-Resistance vs. Gate-to-Source Voltage



100





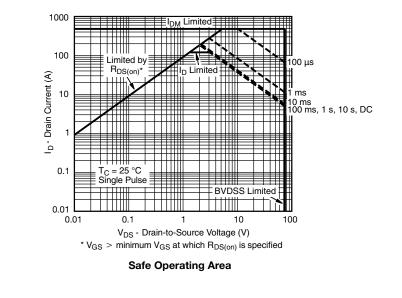
Drain Source Breakdown vs. Junction Temperature

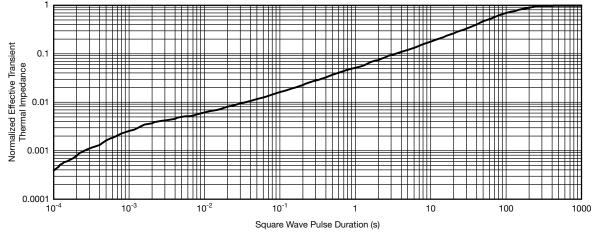
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THERMAL RATINGS ($T_A = 25 \text{ °C}$, unless otherwise noted)

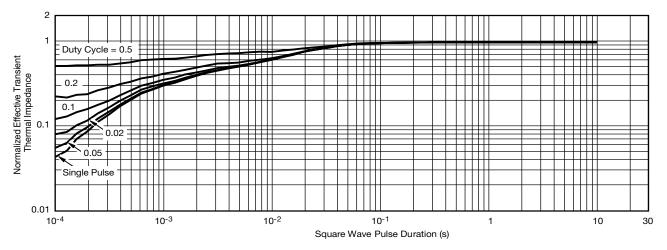




Normalized Thermal Transient Impedance, Junction-to-Ambient



THERMAL RATINGS ($T_A = 25 \text{ °C}$, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

Note

· The characteristics shown in the two graphs

- Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)

- Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <u>www.vishay.com/ppg?64729</u>.



TO-263 (D²PAK): 3-LEAD









DETAIL A (ROTATED 90°)



		INCHES		MILLIMETERS		
DIM.		MIN.	MAX.	MIN.	MAX.	
A		0.160	0.190	4.064	4.826	
	b	0.020	0.039	0.508	0.990	
	b1	0.020	0.035	0.508	0.889	
	b2	0.045	0.055	1.143	1.397	
с*	Thin lead	0.013	0.018	0.330	0.457	
C	Thick lead	0.023	0.028	0.584	0.711	
c1	Thin lead	0.013	0.017	0.330	0.431	
CI	Thick lead	0.023	0.027	0.584	0.685	
	c2	0.045	0.055	1.143	1.397	
	D	0.340	0.380	8.636	9.652	
	D1	0.220	0.240	5.588	6.096	
	D2	0.038	0.042	0.965	1.067	
D3		0.045	0.055	1.143	1.397	
D4		0.044	0.052	1.118	1.321	
	E	0.380	0.410	9.652	10.414	
	E1	0.245	-	6.223	-	
E2		0.355	0.375	9.017	9.525	
E3		0.072	0.078	1.829	1.981	
	е	0.100 BSC		2.54 BSC		
	К	0.045	0.055	1.143	1.397	
L		0.575	0.625	14.605	15.875	
L1		0.090	0.110	2.286	2.794	
L2		0.040	0.055	1.016	1.397	
L3		0.050	0.070	1.270	1.778	
L4 0.01		0.010) BSC	0.254 BSC		
М		-	0.002	-	0.050	
ECN: T13-0707-Rev. K, 30-Sep-13 DWG: 5843						

Notes

- 1. Plane B includes maximum features of heat sink tab and plastic. 2. No more than 25 % of L1 can fall above seating plane by
- max. 8 mils.3. Pin-to-pin coplanarity max. 4 mils.
- 4. *: Thin lead is for SUB, SYB.
 - Thick lead is for SUM, SYM, SQM.
- 5. Use inches as the primary measurement.

This feature is for thick lead.

Revison: 30-Sep-13



RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads Dimensions in Inches/(mm)

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