

## Stellaris® LM3S6420 RevA2 Errata

This document contains known errata at the time of publication for the Stellaris LM3S6420 microcontroller. The table below summarizes the errata and lists the affected revisions. See the data sheet for more details.

See also the ARM® Cortex™-M3 errata, ARM publication number PR326-PRDC-009450 v2.0.

**Table 1. Revision History**

| Date           | Revision | Description   |
|----------------|----------|---|
| August 2011    | 3.0      | <ul style="list-style-type: none"> <li>Added issue "Standard R-C network cannot be used on <math>\overline{RST}</math> to extend POR timing" on page 5.</li> <li>Added issue "Writes to Hibernation module registers may change the value of the RTC" on page 8.</li> <li>Clarified issue "General-purpose timer 16-bit Edge Count or Edge Time mode does not load reload value" on page 10 to include Edge-Time mode.</li> </ul> |
| September 2010 | 2.10     | <ul style="list-style-type: none"> <li>Minor edits and clarifications.</li> </ul>   |
| July 2010      | 2.9      | <ul style="list-style-type: none"> <li>Added issue "The RTRIS bit in the UARTRIS register is only set when the interrupt is enabled" on page 11.</li> </ul>   |
| June 2010      | 2.8      | <ul style="list-style-type: none"> <li>Added issue "External reset does not reset the XTAL to PLL Translation (PLLCFG) register" on page 5.</li> </ul>  |
| May 2010       | 2.7      | <ul style="list-style-type: none"> <li>Minor edits and clarifications.</li> </ul>   |
| April 2010     | 2.6      | <ul style="list-style-type: none"> <li>Minor edits and clarifications.</li> </ul>   |
| April 2010     | 2.5      | <ul style="list-style-type: none"> <li>Minor edits and clarifications.</li> </ul>   |
| February 2010  | 2.4      | <ul style="list-style-type: none"> <li>Added issue "The General-Purpose Timer match register does not function correctly in 32-bit mode" on page 10.</li> </ul>   |
| Jan 2010       | 2.3      | <ul style="list-style-type: none"> <li>"Hard Fault possible when waking from Sleep or Deep-Sleep modes and Cortex-M3 Debug Access Port (DAP) is enabled" has been removed and the content added to the LM3S6420 data sheet.</li> <li>"Ethernet number of Packets decremented early" has been removed and the content added to the LM3S6420 data sheet.</li> </ul>   |
| Dec 2009       | 2.2      | Started tracking revision history.  |

**Table 2. List of Errata**

| Erratum Number | Erratum Title   | Module Affected            | Revision(s) Affected |
|----------------|---|----------------------------|----------------------|
| 1.1            | JTAG pins do not have internal pull-ups enabled at power-on reset                 | JTAG and Serial Wire Debug | A2                   |
| 1.2            | JTAG INTEST instruction does not work   | JTAG and Serial Wire Debug | A2                   |
| 2.1            | Clock source incorrect when waking up from Deep-Sleep mode in some configurations | System Control             | A2                   |

| Erratum Number | Erratum Title   | Module Affected        | Revision(s) Affected |
|----------------|---|------------------------|----------------------|
| 2.2            | PLL may not function properly at default LDO setting  | System Control         | A2                   |
| 2.3            | I/O buffer 5-V tolerance issue  | System Control         | A2                   |
| 2.4            | PLL Runs Fast When Using a 3.6864-MHz Crystal   | System Control         | A2                   |
| 2.5            | External reset does not reset the XTAL to PLL Translation (PLLCFG) register   | System Control         | A2                   |
| 2.6            | Standard R-C network cannot be used on $\overline{\text{RST}}$ to extend POR timing   | System Control         | A2                   |
| 3.1            | Hibernation module low VBAT detection does not work as expected   | Hibernation Module     | A2                   |
| 3.2            | Performing a system-wide reset also resets the Hibernation module and all of its registers  | Hibernation Module     | A2                   |
| 3.3            | Hibernation module may have higher current draw than specified in data sheet under certain conditions                                     | Hibernation Module     | A2                   |
| 3.4            | Hibernation module returns from the Hibernation state to the Wake state regardless of the status of the VDD supply to the microcontroller | Hibernation Module     | A2                   |
| 3.5            | Certain Hibernation module register writes cause RTC Counter register inaccuracy  | Hibernation Module     | A2                   |
| 3.6            | Hibernation module state retention registers may corrupt after Wake sequence  | Hibernation Module     | A2                   |
| 3.7            | Writes to Hibernation module registers may change the value of the RTC  | Hibernation Module     | A2                   |
| 4.1            | GPIO input pin latches in the Low state if pad type is open drain   | GPIO                   | A2                   |
| 4.2            | GPIO pins may glitch during power supply ramp up  | GPIO                   | A2                   |
| 5.1            | General-purpose timer Edge Count mode count error when timer is disabled  | General-Purpose Timers | A2                   |
| 5.2            | General-purpose timer 16-bit Edge Count or Edge Time mode does not load reload value  | General-Purpose Timers | A2                   |
| 5.3            | The General-Purpose Timer match register does not function correctly in 32-bit mode   | General-Purpose Timers | A2                   |
| 6.1            | The RTRIS bit in the UARTRIS register is only set when the interrupt is enabled   | UART                   | A2                   |

# 1 JTAG and Serial Wire Debug

## 1.1 JTAG pins do not have internal pull-ups enabled at power-on reset

### Description:

Following a power-on reset, the JTAG pins  $\overline{\text{TRST}}$ , TCK, TMS, TDI, and TDO (PB7 and PC[3:0]) do not have internal pull-ups enabled. Consequently, if these pins are not driven from the board, two things may happen:

- The JTAG port may be held in reset and communication with a four-pin JTAG-based debugger may be intermittent or impossible.

- The receivers may draw excess current.

**Workaround:**

There are a number of workarounds for this problem, varying in complexity and impact:

1. Add external pull-up resistors to all of the affected pins. This workaround solves both issues of JTAG connectivity and current consumption.
2. Add an external pull-up resistor to  $\overline{\text{TRST}}$ . Firmware should enable the internal pull-ups on the affected pins by setting the appropriate  $\text{PUE}$  bits of the appropriate **GPIO Pull-Up Select (GPIOPUR)** registers as early in the reset handler as possible. This workaround addresses the issue of JTAG connectivity, but does not address the current consumption other than to limit the affected period (from power-on reset to code execution).
3. Pull-ups on the JTAG pins are unnecessary for code loaded via the SWD interface or via the serial boot loader. Loaded firmware should enable the internal pull-ups on the affected pins by setting the appropriate  $\text{PUE}$  bits of the appropriate **GPIOPUR** registers as early in the reset handler as possible. This method does not address the current consumption other than to limit the affected period (from power-on reset to code execution).

**Silicon Revision Affected:**

A2

## 1.2 JTAG INTEST instruction does not work

**Description:**

The JTAG INTEST (Boundary Scan) instruction does not properly capture data.

**Workaround:**

None.

**Silicon Revision Affected:**

A2

## 2 System Control

### 2.1 Clock source incorrect when waking up from Deep-Sleep mode in some configurations

**Description:**

In some clocking configurations, the core prematurely starts executing code before the main oscillator (MOSC) has stabilized after waking up from Deep-Sleep mode. This situation can cause undesirable behavior for operations that are frequency dependent, such as UART communication.

This issue occurs if the system is configured to run off the main oscillator, with the PLL bypassed and the  $\text{DSOSCSRC}$  field of the **Deep-Sleep Clock Configuration (DSLPCCLKCFG)** register set to use the internal 12-MHz oscillator, 30-KHz internal oscillator, or 32-KHz external oscillator. When the system is triggered to wake up, the core should wait for the main oscillator to stabilize before starting to execute code. Instead, the core starts executing code while being clocked from the deep-sleep clock source set in the **DSLPCCLKCFG** register. When the main oscillator stabilizes, the clock to the core is properly switched to run from the main oscillator.

**Workaround:**

Run the system off of the main oscillator (MOSC) with the PLL enabled. In this mode, the clocks are switched at the proper time.

If the main oscillator must be used to clock the system without the PLL, a simple wait loop at the beginning of the interrupt handler for the wake-up event should be used to stall the frequency-dependent operation until the main oscillator has stabilized.

**Silicon Revision Affected:**

A2

## 2.2 PLL may not function properly at default LDO setting

**Description:**

In designs that enable and use the PLL module, unstable device behavior may occur with the LDO set at its default of 2.5 volts or below (minimum of 2.25 volts). Designs that do not use the PLL module are not affected.

**Workaround:**

Prior to enabling the PLL module, it is recommended that the default LDO voltage setting of 2.5 V be adjusted to 2.75 V using the **LDO Power Control (LDOPCTL)** register.

**Silicon Revision Affected:**

A2

## 2.3 I/O buffer 5-V tolerance issue

**Description:**

GPIO buffers are not 5-V tolerant when used in open-drain mode. Pulling up the open-drain pin above 4 V results in high current draw.

**Workaround:**

When configuring a pin as open drain, limit any pull-up resistor connections to the 3.3-V power rail.

**Silicon Revision Affected:**

A2

## 2.4 PLL Runs Fast When Using a 3.6864-MHz Crystal

**Description:**

If the PLL is enabled, and a 3.6864-MHz crystal is used, the PLL runs 4% fast.

**Workaround:**

Use a different crystal whose frequency is one of the other allowed crystal frequencies (see the values shown for the XTAL bit in the **RCC** register).

**Silicon Revision Affected:**

A2

## 2.5 External reset does not reset the XTAL to PLL Translation (PLLCFG) register

### Description:

Performing an external reset (anything but power-on reset) reconfigures the `XTAL` field in the **Run-Mode Clock Configuration (RCC)** register to the 6 MHz setting, but does not reset the **XTAL to PLL Translation (PLLCFG)** register to the 6 MHz setting.

Consider the following sequence:

1. Performing a power-on reset results in `XTAL` = 6 MHz and **PLLCFG** = 6 MHz
2. Write an 8 MHz value to the `XTAL` field results in `XTAL` = 8 MHz and **PLLCFG** = 8 MHz
3.  $\overline{\text{RST}}$  asserted results in `XTAL` = 6 MHz and **PLLCFG** = 8 MHz

In the last step, **PLLCFG** was not reset to its 6MHz setting. If this step is followed by enabling the PLL to run from an attached 6-MHz crystal, the PLL then operates at 300MHz instead of 400MHz. Subsequently configuring the `XTAL` field with the 8 MHz setting does not change the setting of **PLLCFG**.

### Workaround:

Set `XTAL` in **PLLCFG** to an incorrect value, and then to the desired value. The second change updates the register correctly. Do not enable the PLL until after the second change.

### Silicon Revision Affected:

A2

## 2.6 Standard R-C network cannot be used on $\overline{\text{RST}}$ to extend POR timing

### Description:

The standard R-C network on  $\overline{\text{RST}}$  does not work to extend POR timing beyond the 10 ms on-chip POR. Instead of following the standard capacitor charging curve,  $\overline{\text{RST}}$  jumps straight to 3 V at power on. The capacitor is fully charged by current out of the  $\overline{\text{RST}}$  pin and does not extend or filter the power-on condition. As a result, the reset input is not extended beyond the POR.

### Workaround:

Add a diode to block the output current from  $\overline{\text{RST}}$ . This helps to extend the  $\overline{\text{RST}}$  pulse, but also means that the R-C is not as effective as a noise filter.

### Silicon Revision Affected:

A2

## 3 Hibernation Module

### 3.1 Hibernation module low VBAT detection does not work as expected

#### Description:

The Hibernation module is designed to detect a low  $V_{\text{BAT}}$  condition. This feature is enabled by setting the `LOWBATEN` bit in the **Hibernation Control (HIBCTL)** register. When enabled, the low  $V_{\text{BAT}}$

detection incorrectly detects a low  $V_{BAT}$  condition at 3.15 V. This is supposed to trigger a low  $V_{BAT}$  condition at 2.35 V.

**Workaround:**

This feature should not be used and must be disabled by clearing the `LOWBATEN` bit in the `HIBCTL` register. The battery voltage can be sensed using a hardware workaround by wiring an analog comparator input pin to the battery and setting the comparator reference pin voltage to the desired detection trip level.

**Silicon Revision Affected:**

A2

### 3.2 Performing a system-wide reset also resets the Hibernation module and all of its registers

**Description:**

Performing a system-wide reset by asserting the  $\overline{RST}$  pin, encountering a Brown-Out Reset, or setting the `SYSRESETREQ` bit in the ARM Cortex-M3 Application Interrupt and Reset Control register also incorrectly causes the Hibernation module to be reset. All of the Hibernation module registers are reset, including the battery-backed **Hibernation Data (HIBDATA)** and the **Hibernation RTC Counter (HIBRTCC)** registers.

**Workaround:**

None.

**Silicon Revision Affected:**

A2

### 3.3 Hibernation module may have higher current draw than specified in data sheet under certain conditions

**Description:**

If a battery voltage is applied to the  $V_{BAT}$  power pin prior to power being applied to the  $V_{DD}$  power pins of the device, the current draw from the  $V_{BAT}$  pin is greater than expected. The current may be as high as 1.6 mA instead of the data sheet specified 17  $\mu A$ . The condition exists until power is applied to the  $V_{DD}$  pin. Once the  $V_{DD}$  pin has been powered, the  $V_{BAT}$  current draw functions as expected. The  $V_{DD}$  pin can then be powered up and down as required and the  $V_{BAT}$  pin current specification is maintained.

**Workaround:**

The  $V_{BAT}$  pin higher-than-specified current draw condition can be avoided if the microcontroller's  $V_{DD}$  power pins are powered on prior to the time a battery voltage is initially applied to the  $V_{BAT}$  pin.

**Silicon Revision Affected:**

A2

### 3.4 Hibernation module returns from the Hibernation state to the Wake state regardless of the status of the VDD supply to the microcontroller

#### Description:

When the Hibernation module is in Hibernation mode and receives an event to initiate a wake-up (assertion of the  $\overline{\text{WAKE}}$  pin, RTC match, or low-battery detect), the  $\overline{\text{HIB}}$  signal is de-asserted, enabling the external regulator to provide  $V_{\text{DD}}$  to the device. The device then performs a Power-On Reset (POR) and the software can query the **Hibernation Raw Interrupt Status (HIBRIS)** register to determine if a hibernation wake occurred.

If the regulator does not have a power source, or for some reason  $V_{\text{DD}}$  is not immediately applied to the device when the  $\overline{\text{HIB}}$  signal is de-asserted, the Hibernation module still exits from its Hibernation state to its Wake state, but the device is not able to perform its POR sequence. If power is then restored to the regulator (providing  $V_{\text{DD}}$  to the device), the device executes a POR, however, the state of the Hibernation module is incorrectly reset, and all of the registers within the Hibernation module, including the **Hibernation RTC Counter (HIBRTCC)** and **Hibernation Data (HIBDATA)** registers are set to their reset state.

#### Workaround:

Always ensure that power is available to the regulator controlled by the  $\overline{\text{HIB}}$  signal when the  $\overline{\text{HIB}}$  signal is de-asserted during a wake event.

#### Silicon Revision Affected:

A2

### 3.5 Certain Hibernation module register writes cause RTC Counter register inaccuracy

#### Description:

The Hibernation module contains a **Hibernation RTC Counter (HIBRTCC)** register that keeps an accumulated running one-second count. This register is updated from an internal, 32-KHz counter which is not visible to the user. As this counter value rolls over, it provides a tick count once per second to the **HIBRTCC** register. Register writes to the **Hibernation RTC Match (HIBRTCM0, HIBRTCM1)** registers, the **Hibernation RTC Trim (HIBRTCT)** register, or the **Hibernation Data (HIBDATA)** register cause the 32-KHz counter to reset to its start value. The result is that the **HIBRTCC** register value loses accuracy each time one of these Hibernation registers is written because the 32-KHz counter is reset in the midst of its one-second count window, effectively delaying the **HIBRTCC** register counter value from its ideal value.

#### Workaround:

To minimize the amount of introduced error, the application can write to the affected registers immediately after the RTC rolls over. The RTC rollover can be detected by polling the RTC value in the **HIBRTCC** register and waiting for it to change. If the application writes to the affected registers with a predictable and repeatable pattern, then the **HIBRTCT** register can be used to compensate for introduced error.

#### Silicon Revision Affected:

A2

### 3.6 Hibernation module state retention registers may corrupt after Wake sequence

**Description:**

When transitioning from a Hibernate condition to a Wake-up state, the **Hibernation Control (HIBCTL)** register and **Hibernation Interrupt Mask (HIBIM)** register values may occasionally become corrupted. This situation occurs after a wake-up event caused by an RTC match condition or an external signal asserting the  $\overline{\text{WAKE}}$  pin of the device.

**Workaround:**

Software should mirror the data in the **HIBCTL** and **HIBIM** registers to the **Hibernation Data (HIBDATA)** register before initiating a Hibernation sequence. Immediately upon returning from the Hibernation state to the Wake-up state, software should write the data mirrored from the **HIBDATA** registers back into the **HIBCTL** and **HIBIM** registers.

**Silicon Revision Affected:**

A2

### 3.7 Writes to Hibernation module registers may change the value of the RTC

**Description:**

If the Hibernation module's RTC counter is active, any write to certain Hibernation module registers that occurs while the RTC counter is changing from the current value to the next can cause corruption of the RTC counter stored in the **HIBRTCC** register. Registers affected are: **HIBRTCC**, **HIBRTCM0**, **HIBRTCM1**, **HIBRTCLD**, **HIBRTCT**, and **HIBDATA**.

**Workaround:**

The user application must guarantee that writes to the affected Hibernation module registers cannot occur on the RTC counter boundary. Any initial configuration of the affected Hibernation module registers must be done before enabling the RTC counter.

There are two ways to update affected Hibernation Module registers after initial configuration:

1. Use the Hibernation RTC match interrupt to perform writes to the affected Hibernation module registers. Assuming the interrupt is guaranteed to be serviced within 1 second, this technique provides a mechanism for the application to know that the RTC update event has occurred and that it is safe to write data to the affected Hibernation module registers. This method is useful for applications that don't require many writes to Hibernation module registers.
2. Set up a secondary time-keeping resource to indicate when it is safe to perform writes to the affected Hibernation module registers. For example, use a general purpose timer in combination with the Hibernation RTC match interrupt. In this scenario, the RTC match interrupt is used to both update the match register value and enable the general purpose timer in one-shot mode. The timer must be configured to have a maximum time-out period of less than 1 second. In this configuration, a global variable is used to indicate that it is safe to perform writes to the affected Hibernation module registers. When the one-shot timer times out, the timer interrupt updates the global variable to indicate that writes are no longer safe. This procedure is repeated on every RTC match interrupt.



**Silicon Revision Affected:**

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## 4 GPIO

### 4.1 GPIO input pin latches in the Low state if pad type is open drain

**Description:**

GPIO pins function normally if configured as inputs and the open-drain configuration is disabled. If open drain is enabled while the pin is configured as an input using the **GPIO Alternate Function Select (GPIOAFSEL)**, **GPIO Open Drain Select (GPIOODR)**, and **GPIO Direction (GPIODIR)** registers, then the pin latches Low and excessive current (into pin) results if an attempt is made to drive the pin High. The open-drain device is not controllable.

A GPIO pin is not normally configured as open drain and as an input at the same time. A user may want to do this when driving a signal out of a GPIO open-drain pad while configuring the pad as an input to read data on the same pin being driven by an external device. Bit-banging a bidirectional, open-drain bus (for example, I<sup>2</sup>C) is an example.

**Workaround:**

If a user wants to read the state of a GPIO pin on a bidirectional bus that is configured as an open-drain output, the user must first disable the open-drain configuration and then change the direction of the pin to an input. This precaution ensures that the pin is never configured as an input and open drain at the same time.

A second workaround is to use two GPIO pins connected to the same bus signal. The first GPIO pin is configured as an open-drain output, and the second is configured as a standard input. This way the open-drain output can control the state of the signal and the input pin allows the user to read the state of the signal without causing the latch-up condition.

**Silicon Revision Affected:**

A2

### 4.2 GPIO pins may glitch during power supply ramp up

**Description:**

Upon completing a POR (power on reset) sequence, the GPIO pins default to a tri-stated input condition. However, during the initial ramp up of the external  $V_{DD}$  supply from 0.0 V to 3.3 V, the GPIO pins are momentarily configured as output drivers during the time the internal LDO circuit is also ramping up. As a result, a signal glitch may occur on GPIO pins before both the external  $V_{DD}$  supply and internal LDO voltages reach their normal operating conditions. This situation can occur when the  $V_{DD}$  and LDO voltages ramp up at significantly different rates. The LDO voltage ramp-up time is affected by the load capacitance on the LDO pin, therefore, it is important to keep this load at a nominal 1  $\mu$ F value as recommended in the data sheet. Adding significant more capacitance loading beyond the specification causes the time delay between the two supply ramp-up times to grow, which possibly increases the severity of the glitching behavior.

**Workaround:**

Ensuring that the  $V_{DD}$  power supply ramp up is as fast as possible helps minimize the potential for GPIO glitches. Follow guidelines for LDO pin capacitive loading documented in the electrical section

of the data sheet. System designers must ensure that, during the  $V_{DD}$  supply ramp-up time, possible GPIO pin glitches can cause no adverse effects to their systems.

**Silicon Revision Affected:**

A2

## 5 General-Purpose Timers

### 5.1 General-purpose timer Edge Count mode count error when timer is disabled

**Description:**

When a general-purpose timer is configured for 16-Bit Input Edge Count Mode, the timer (A or B) erroneously decrements by one when the `Timer Enable (TnEN)` bit in the **GPTM Control (GPTMCTL)** register is cleared (the timer is disabled).

**Workaround:**

When the general-purpose timer is configured for Edge Count mode and software needs to “stop” the timer, the timer should be reloaded with the current count + 1 and restarted.

**Silicon Revision Affected:**

A2

### 5.2 General-purpose timer 16-bit Edge Count or Edge Time mode does not load reload value

**Description:**

In Edge Count or Edge Time mode, the input events on the `CCP` pin decrement the counter until the count matches what is in the **GPTM Timern Match (GPTMTnMATCHR)** register. At that point, an interrupt is asserted and then the counter should be reloaded with the original value and counting begins again. However, the reload value is not reloaded into the timer.

**Workaround:**

Rewrite the **GPTM Timern Interval Load (GPTMTnILR)** register before restarting.

**Silicon Revision Affected:**

A2

### 5.3 The General-Purpose Timer match register does not function correctly in 32-bit mode

**Description:**

The **GPTM Timer A Match (GPTMTAMATCHR)** register triggers a match interrupt when the lower 16 bits match, regardless of the value of the upper 16 bits.

**Workaround:**

None.

**Silicon Revision Affected:**

A2

## 6 UART

### 6.1 The RTRIS bit in the UARTRIS register is only set when the interrupt is enabled

**Description:**

The `RTRIS` (UART Receive Time-Out Raw Interrupt Status) bit in the **UART Raw Interrupt Status (UARTRIS)** register should be set when a receive time-out occurs, regardless of the state of the enable `RTIM` bit in the **UART Interrupt Mask (UARTIM)** register. However, currently the `RTIM` bit must be set in order for the `RTRIS` bit to be set when a receive time-out occurs.

**Workaround:**

For applications that require polled operation, the `RTIM` bit can be set while the UART interrupt is disabled in the NVIC using the `IntDisable(n)` function in the StellarisWare Peripheral Driver Library, where `n` is 21, 22, or 49 depending whether UART0, UART1 or UART2 is used. With this configuration, software can poll the `RTRIS` bit, but the interrupt is not reported to the NVIC.

**Silicon Revision Affected:**

A2

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| Interface              | <a href="http://interface.ti.com">interface.ti.com</a>                               |
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