Application Report
SNOA554C–October 2011–Revised May 2013

AN-2090 LM3448 -120VAC, 6W Isolated Flyback LED Driver

ABSTRACT

This application note describes the performance of a LM3448 based Flyback LED driver solution that can be used to power a single LED string consisting of seven to eleven series connected LEDs from a 85 V_{RMS} to 135 V_{RMS}, 60 Hz input power supply.

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1 Introduction

This is a two-layer demonstration board using the bottom and top layer for component placement. The demonstration board can be modified to adjust the LED forward current, the number of series connected LEDs that are driven, and the switching frequency.

Refer to the *LM3448 Phase Dimmable Offline LED Driver with Integrated FET Data Sheet* (SNOSB51) for detailed instructions. A schematic and layout have also been included, along with measured performance characteristics. A bill of materials is also included that describes the parts used on this demonstration board.

2 Key Features

- Drop-in compatibility with TRIAC dimmers
- Line injection circuitry enables PFC values greater than 0.95
- Adjustable LED current and switching frequency
- Flicker free operation

3 Applications

- Retrofit TRIAC Dimming
- Solid State Lighting
- Industrial and Commercial Lighting
- Residential Lighting

4 Performance Specifications

Based on an LED V_f = 3V

Symbol	Parameter	Min	Typ	Max
V_{IN}	Input voltage	85 V_{RMS}	120 V_{RMS}	135 V_{RMS}
V_{OUT}	LED string voltage	21 V	27 V	33 V
I_{LED}	LED string average current	-	228 mA	-
P_{OUT}	Output power	-	6.2 W	-
f_{sw}	Switching frequency	-	73 kHz	-

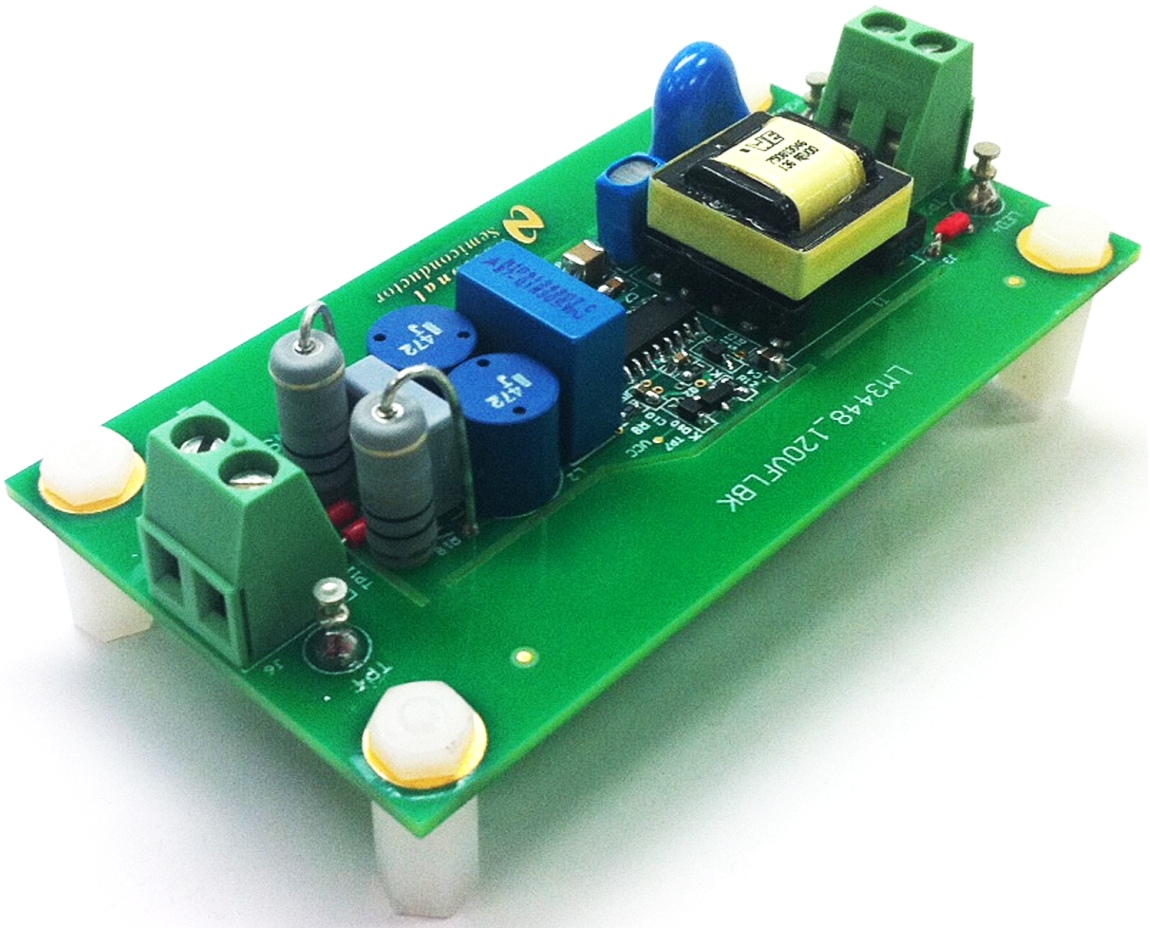


Figure 1. Demo Board

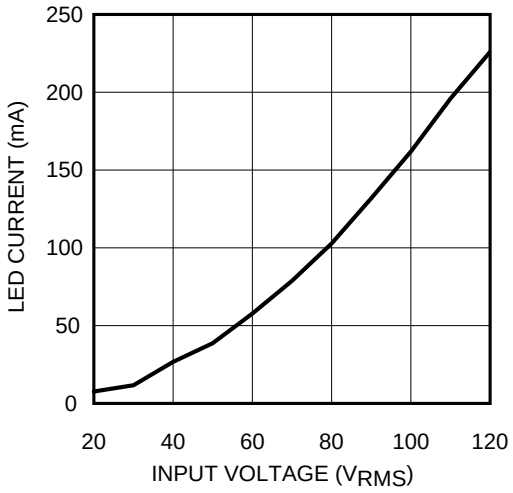


Figure 2. LED Current vs. Line Voltage (using TRIAC Dimmer)

5 Typical Performance Characteristics

T_J=25°C and V_{CC}=12V, unless otherwise specified.

NOTE: Plots of 10 LED performance based on original schematic except that D1 is a 250V TVS and the OVP circuit has been removed.

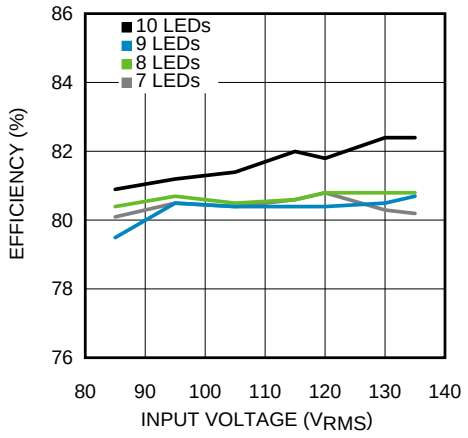


Figure 3. Efficiency vs. Line Voltage

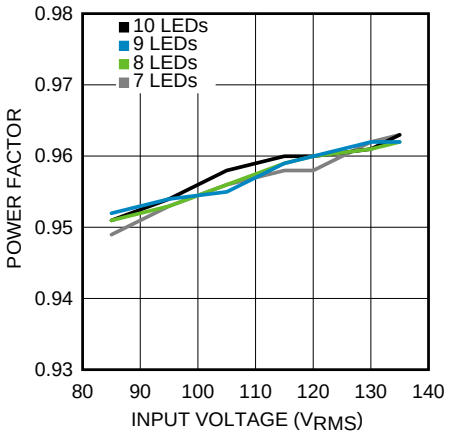


Figure 4. Power Factor vs. Line Voltage

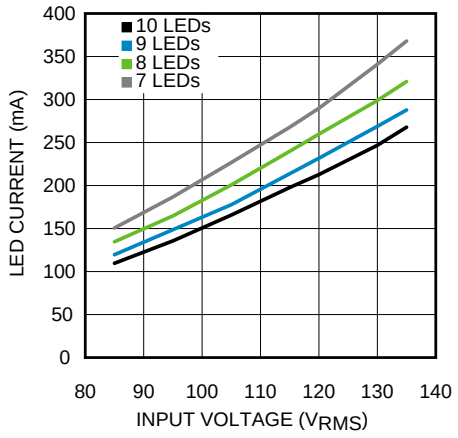


Figure 5. LED Current vs. Line Voltage

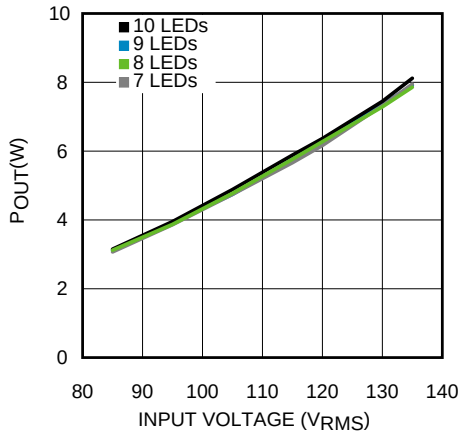


Figure 6. Output Power vs. Line Voltage

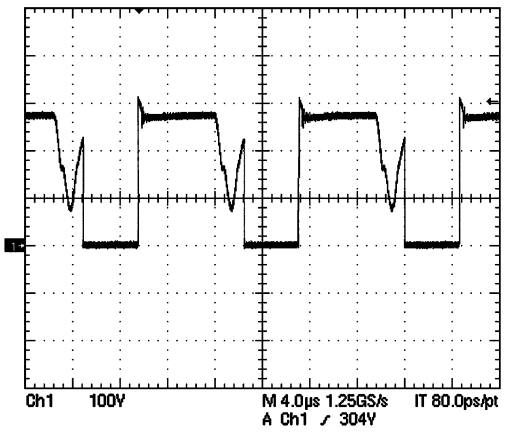


Figure 7. SW FET Drain Voltage Waveform (V_{IN} = 120V_{RMS}, 9 LEDs, I_{LED} = 228mA)

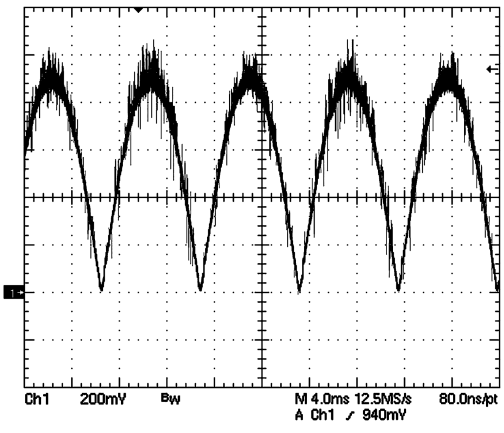


Figure 8. FLTR2 Waveform (V_{IN} = 120V_{RMS}, 9 LEDs, I_{LED} = 228mA)

6 EMI Performance

120V, 6W Conducted EMI Scans

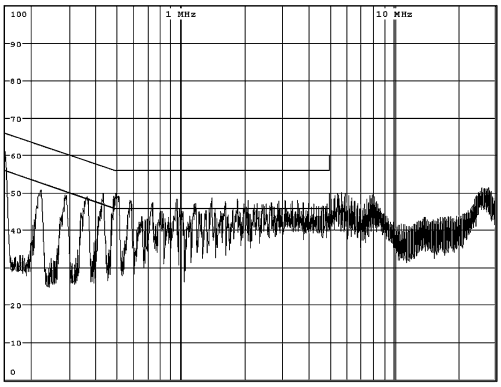


Figure 9. LINE – CISPR/FCC Class B Peak Scan

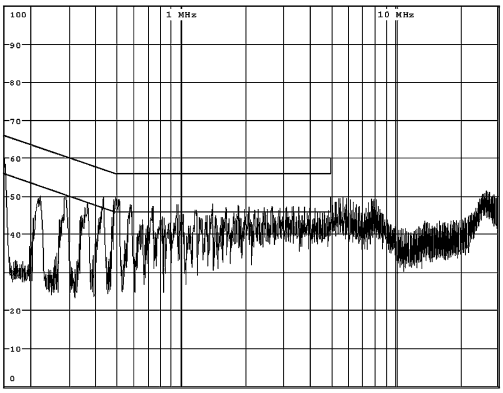


Figure 10. NEUTRAL – CISPR/FCC Class B Peak Scan

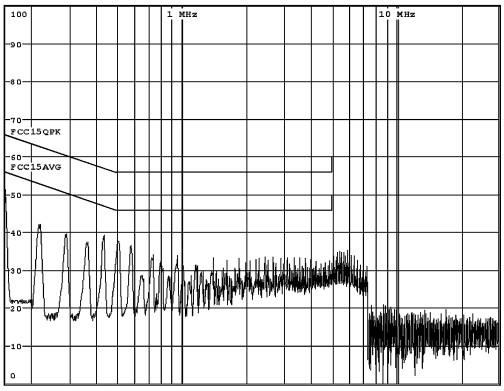


Figure 11. LINE – CISPR/FCC Class B Average Scan

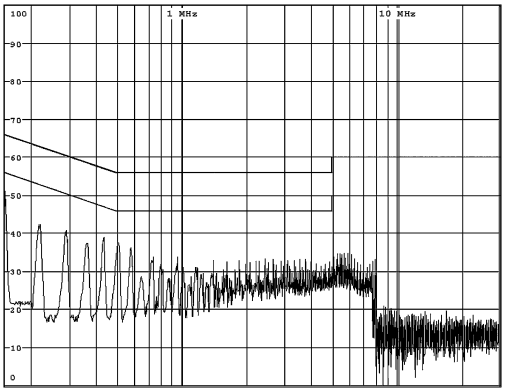


Figure 12. NEUTRAL – CISPR/FCC Class B Average Scan

120V, 6W THD Measurements

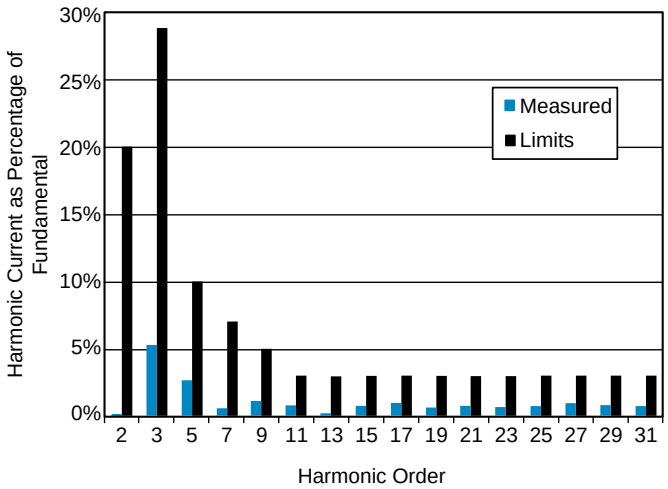


Figure 13. EN-61000-3 Class C Limits

7 Circuit Operation With Forward Phase TRIAC Dimmer

The dimming operation of the circuit was verified using a forward phase TRIAC dimmer. Waveforms captured at different dimmer settings are shown below:

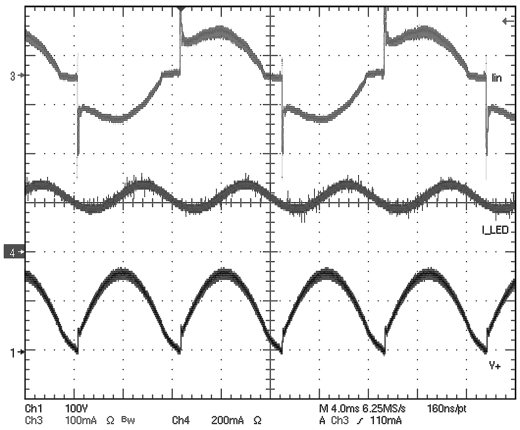


Figure 14. Forward phase circuit at full brightness

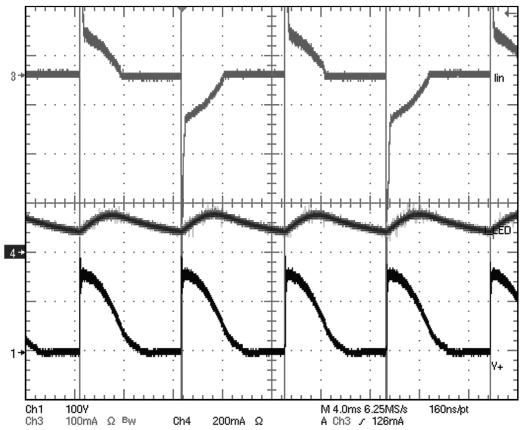


Figure 15. Forward phase circuit at 90° firing angle

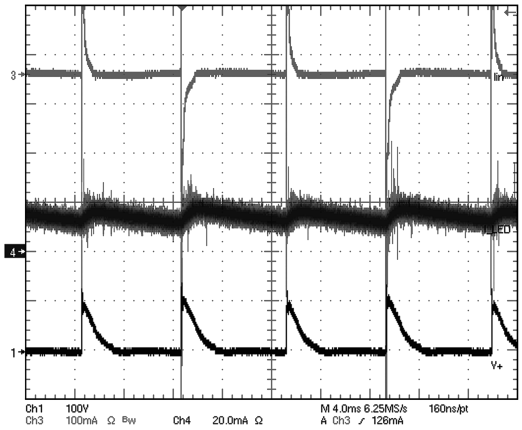


Figure 16. Forward phase circuit at 150° firing angle

8 Circuit Operation With Reverse Phase TRIAC Dimmer

The circuit operation was also verified using a reverse phase dimmer and waveforms captured at different dimmer settings are shown below:

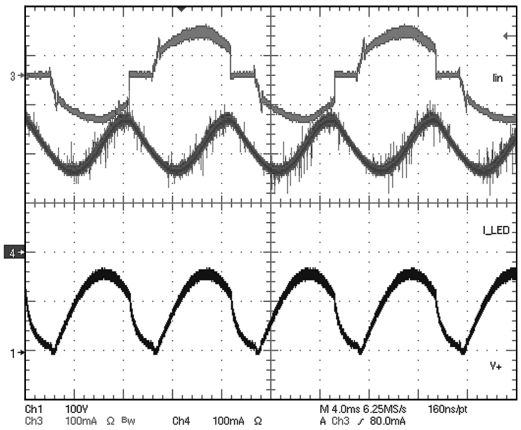


Figure 17. Reverse phase circuit at full brightness

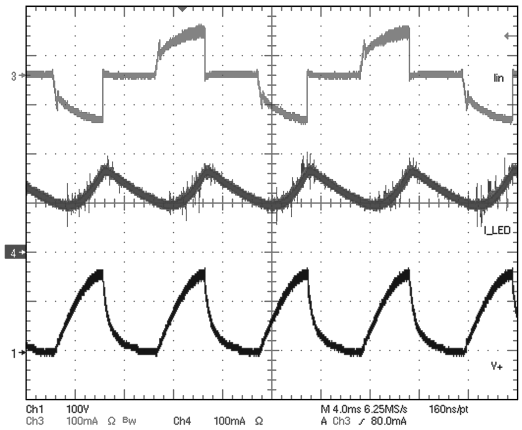


Figure 18. Reverse phase circuit at 90° firing angle

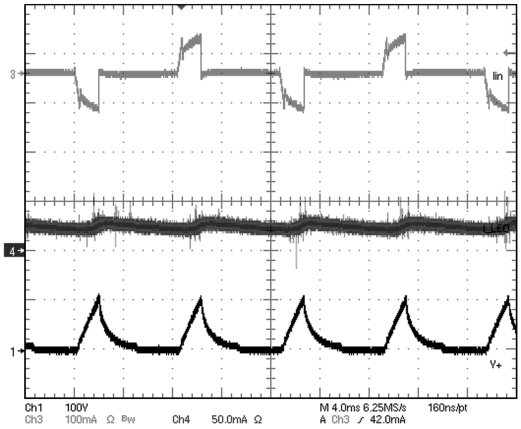
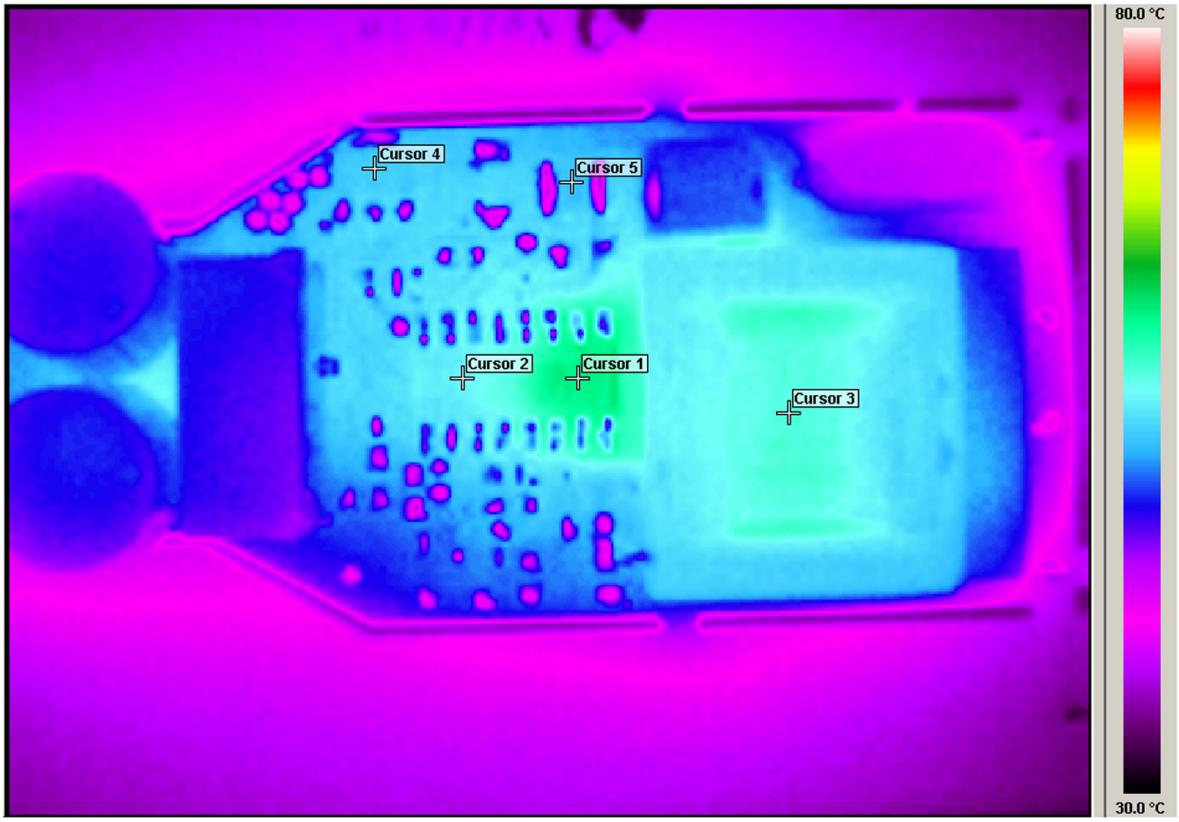


Figure 19. Reverse phase circuit at 150° firing angle

9 Thermal Performance

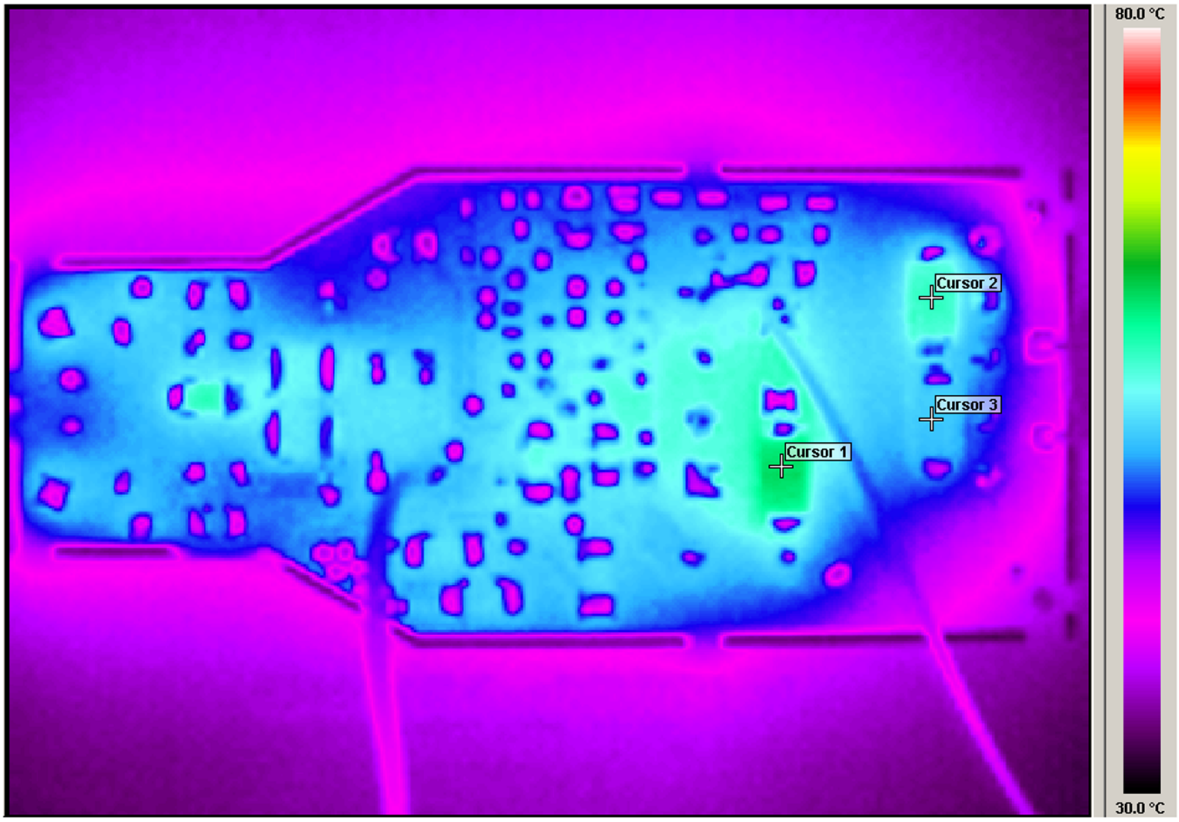
The board temperature was measured using an IR camera (HIS-3000, Wahl) while running under the following conditions: V_{IN} = 120V_{RMS}, I_{LED} = 228mA, # of LEDs = 9, P_{OUT} = 6.2W.

NOTE: Thermal performance is highly dependent on the user's final end-application enclosure, heat-sinking methods, ambient operating temperature, and PCB board layout in addition to the electrical operating conditions. This LM3448 evaluation board is optimized to supply 6W of output power at room temperature without exceeding the thermal limitations of the LM3448. However higher output power levels can be achieved if precautions are taken not to exceed the power dissipation limits of the LM3448 package or die junction temperature. Please see the *LM3448 Phase Dimmable Offline LED Driver with Integrated FET Data Sheet* (SNOSB51) for additional details regarding its thermal specifications.



- Cursor 1: 61.5°C
- Cursor 2: 56.2°C
- Cursor 3: 57.7°C
- Cursor 4: 53.8°C
- Cursor 5: 52.9°C

Figure 20. Top Side - Thermal Scan



- Cursor 1: 62.3°C
- Cursor 2: 58.8°C
- Cursor 3: 53.4°C

Figure 21. Bottom Side - Thermal Scan

10 LM3448 Device Pin-Out

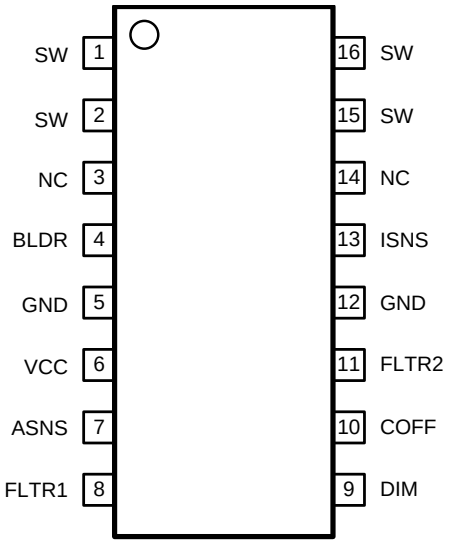


Figure 22. Device Pin-Out

Table 1. Pin Description 16 Pin Narrow SOIC

Pin #	Name	Description
1, 2, 15, 16	SW	Drain connection of internal 600V MOSFET.
3, 14	NC	No connect. Provides clearance between high voltage and low voltage pins. Do not tie to GND.
4	BLDR	Bleeder pin. Provides the input signal to the angle detect circuitry. A 230Ω internal resistor ensures BLDR is pulled down for proper angle sense detection.
5, 12	GND	Circuit ground connection.
6	V_{CC}	Input voltage pin. This pin provides the power for the internal control circuitry and gate driver. Connect a 22µF (minimum) bypass capacitor to ground.
7	ASNS	PWM output of the TRIAC dim decoder circuit. Outputs a 0 to 4V PWM signal with a duty cycle proportional to the TRIAC dimmer on-time.
8	FLTR1	First filter input. The 120Hz PWM signal from ASNS is filtered to a DC signal and compared to a 1 to 3V, 5.85 kHz ramp to generate a higher frequency PWM signal with a duty cycle proportional to the TRIAC dimmer firing angle. Pull above 4.9V (typical) to TRI-STATE® DIM.
9	DIM	Input/output dual function dim pin. This pin can be driven with an external PWM signal to dim the LEDs. It may also be used as an output signal and connected to the DIM pin of other LM3448/LM3445 devices or LED drivers to dim multiple LED circuits simultaneously.
10	COFF	OFF time setting pin. A user set current and capacitor connected from the output to this pin sets the constant OFF time of the switching controller.
11	FLTR2	Second filter input. A capacitor tied to this pin filters the PWM dimming signal to supply a DC voltage to control the LED current. Could also be used as an analog dimming input.
13	ISNS	LED current sense pin (internally connected to MOSFET source). Connect a resistor from ISNS to GND to set the maximum LED current.

11 Demo Board Wiring Overview

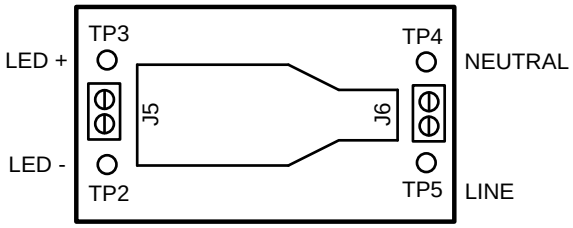


Figure 23. Wiring Connection Diagram

Table 2. Test Points

Test Point	Name	I/O	Description
TP3	LED +	Output	**LED Constant Current Supply** Supplies voltage and constant-current to anode of LED string.
TP2	LED -	Output	**LED Return Connection (not GND)** Connects to cathode of LED string. Do NOT connect to GND.
TP5	LINE	Input	**AC Line Voltage** Connects directly to AC line or output of TRIAC dimmer of a 120VAC system.
TP4	NEUTRAL	Input	**AC Neutral** Connects directly to AC neutral of a 120VAC system.

12 Demo Board Assembly

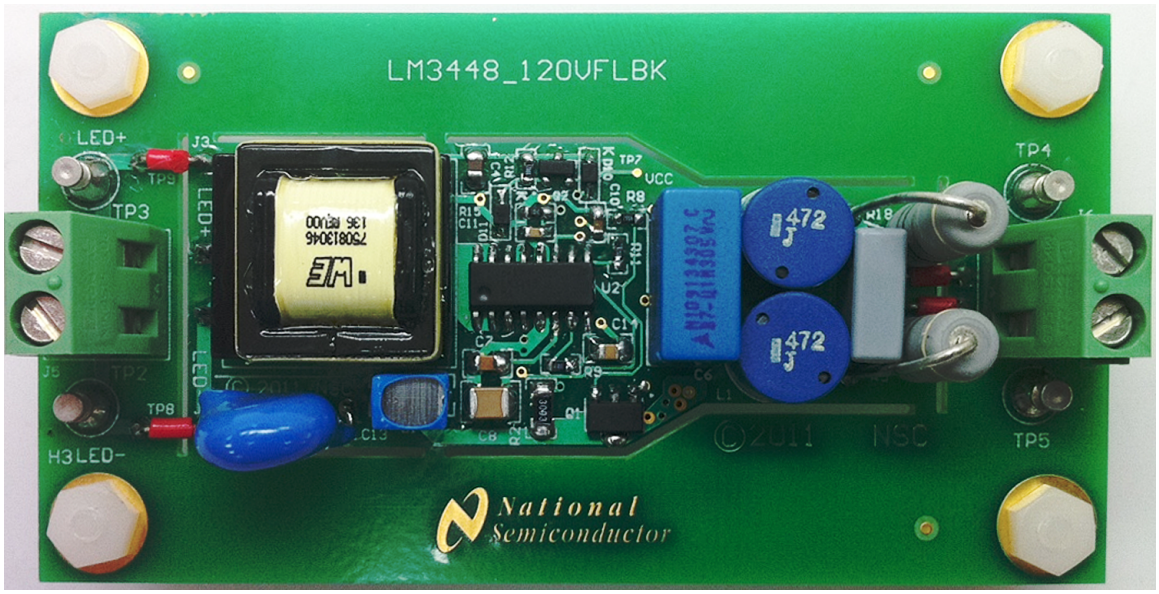


Figure 24. Top View

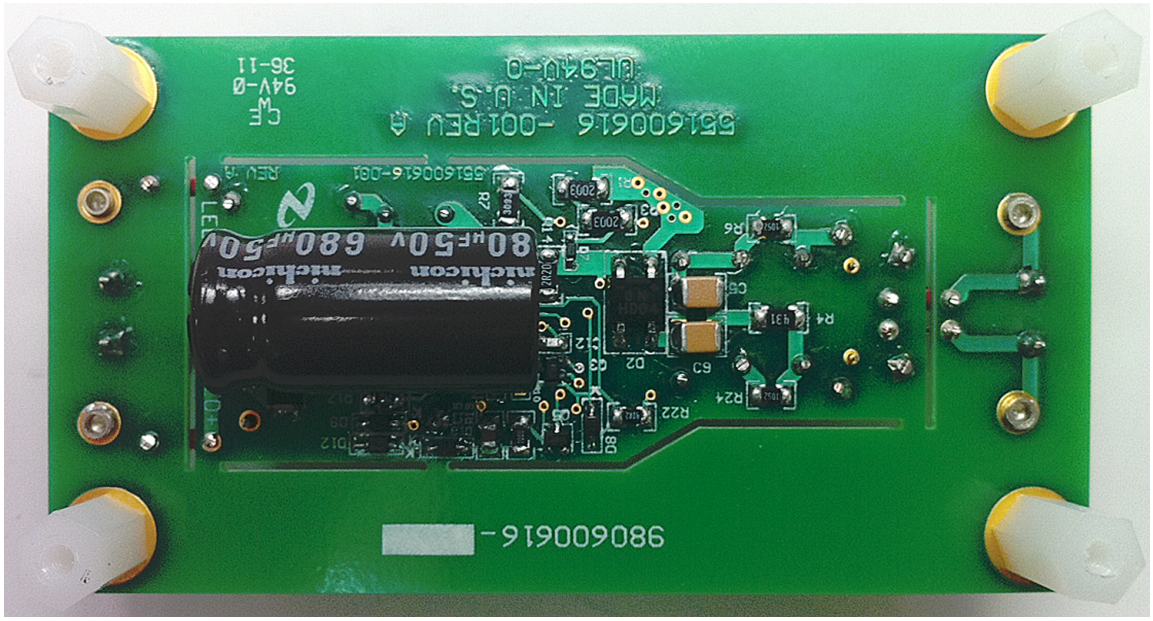


Figure 25. Bottom View

13 Design Guide

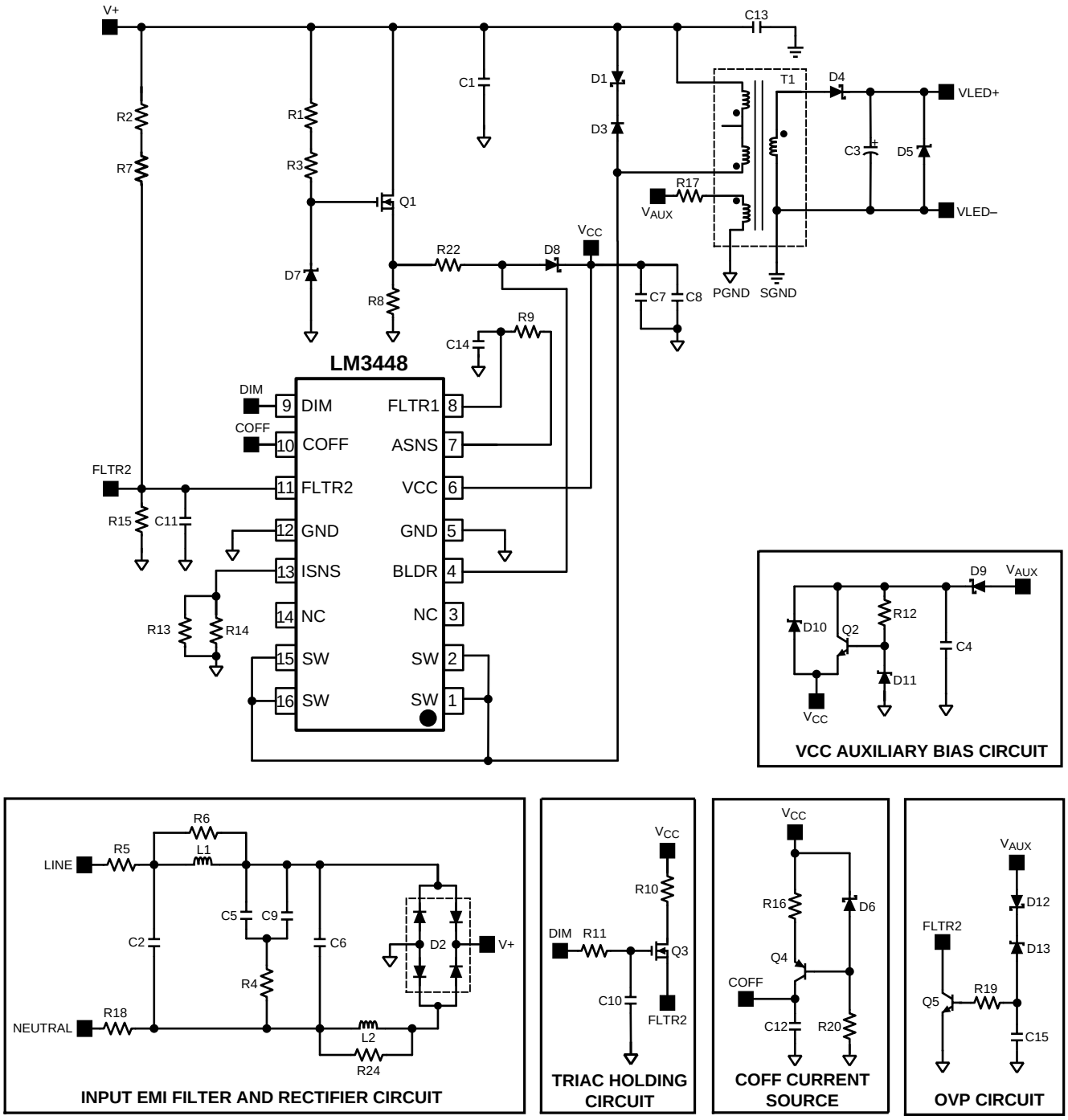


Figure 26. Evaluation Board Schematic

The following section explains how to design an isolated flyback converter using the LM3448. Refer to the *LM3448 Phase Dimmable Offline LED Driver with Integrated FET Data Sheet* (SNOSB51) for specific details regarding the function of the LM3448 device. All reference designators refer to the Evaluation Board Schematic in Figure 26 unless otherwise noted.

13.1 DCM Flyback Converter

This LED driver is designed to accurately emulate an incandescent light bulb and therefore behave as an emulated resistor. The resistor value is determined based on the LED string configuration and the desired output power. The circuit then operates in open-loop, with a fixed duty cycle based on a constant on-time and constant off-time that is set by selecting appropriate circuit components. Like an incandescent lamp, the driver is compatible with both forward and reverse phase dimmers. A key aspect of this design is that the converter operates in discontinuous conduction mode (DCM). DCM is implemented by ensuring that the flyback transformer current reaches zero before the end of the switching period.

By injecting a voltage proportional to the line voltage at the FLTR2 pin (see Figure 27), the LM3448 circuit is essentially turned into a constant power flyback converter operating in discontinuous conduction mode (DCM).

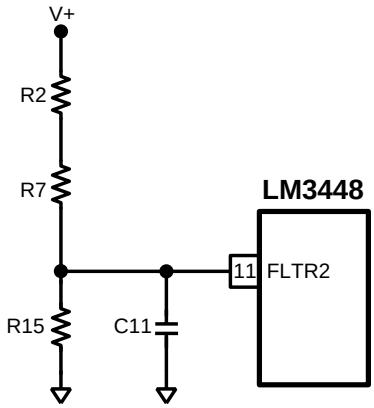


Figure 27. Direct Line-Injection Circuit

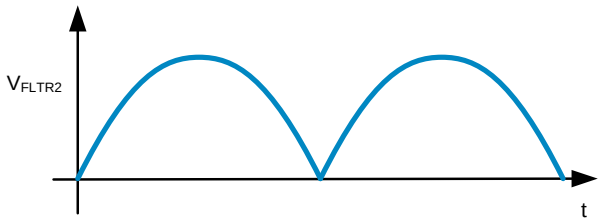


Figure 28. FLTR2 Waveform with No Dimmer

The LM3448 normally works as a constant off-time regulator, but by injecting a $1.0V_{PK}$ rectified AC voltage into the FLTR2 pin, the on-time can be made to be constant. With a DCM flyback converter the primary side current, $i_L(t)$, needs to increase as the rectified input voltage, $V_+(t)$, increases as shown in the following equations,

$$v = L\frac{di}{dt} \tag{1}$$

or,

$$t_{ON} = L\frac{\Delta i_L(t)}{V_+(t)} \tag{2}$$

Therefore a constant on-time (since inductor L is constant) can be obtained.

By using the line voltage injection technique, the FLTR2 pin has the voltage wave shape shown in Figure 28 on it with no TRIAC dimmer in-line. Peak voltage at the FLTR2 pin should be kept below 1.25V otherwise current limit will be tripped. Capacitor C11 in conjunction with resistor R15 acts a filter for noise. Using this technique a power factor greater than 0.95 can be achieved.Figure 29 shows how a constant on-time is maintained.

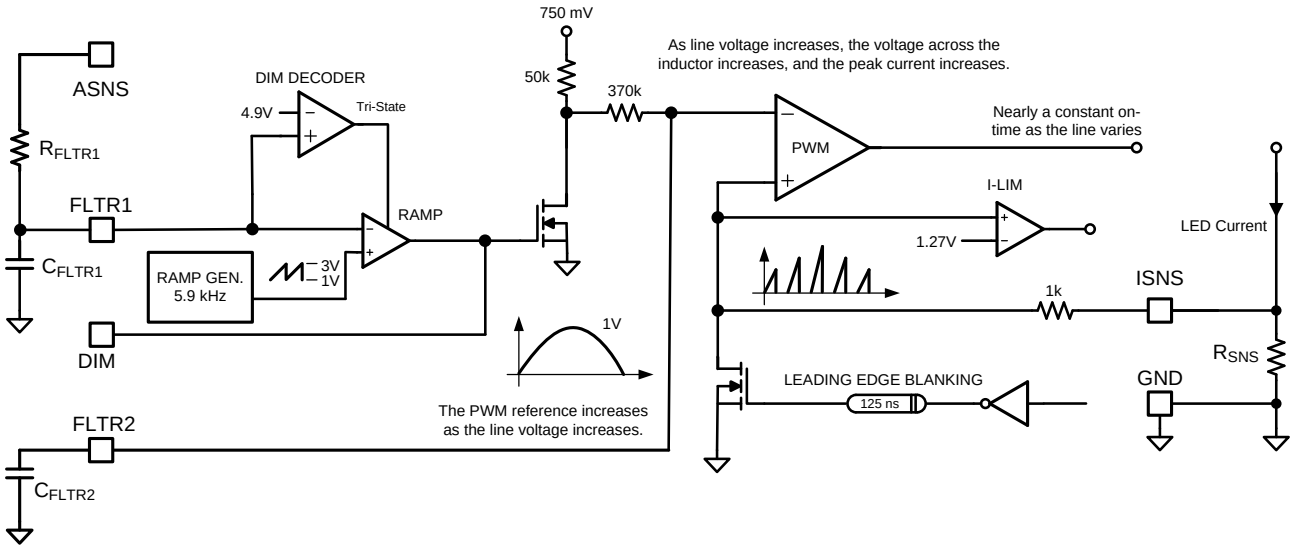


Figure 29. Typical Operation of FLTR2 Pin

Turns Ratio

The first step with an isolated design is to determine the transformer turns ratio. This can be an iterative process that will depend on the specified operating conditions, maximum stresses allowed for the LM3448 SW FET and re-circulating diode as well as transformer core parameters. For many LM3448 flyback designs, an integer turns ratio of 4 or 5 is a good starting point. The next step will be to verify that the chosen turns ratio results in operating conditions that do not violate any other component ratings.

Duty Cycle Calculation

The AC mains voltage at the line frequency f_L is assumed to be perfectly sinusoidal and the diode bridge ideal. This yields a perfect rectified sinusoid at the input to the flyback. The peak nominal input voltage $V_{IN-PK(NOM)}$ is defined in terms of the input voltage $V_{IN(NOM)}$,

$$V_{IN-PK(NOM)} = V_{IN(NOM)} \times \sqrt{2} \tag{3}$$

Duty cycle is calculated at the nominal peak input voltage $V_{IN-PK(NOM)}$. Note that this is the duty cycle for flyback operation at the boundary of continuous conduction mode (CCM) operation. In order to ensure that the converter is operating in DCM, the primary inductance of the transformer will be adjusted lower (refer to "Transformer" section).

$$D = \frac{\left(V_{OUT} \times n\right)}{\left(V_{OUT} \times n\right) + V_{IN-PK(NOM)}} \tag{4}$$

Peak Input Current Calculation

Due to the direct line-injection, the flyback converter operates as a constant power converter. Therefore average input power over one line cycle will approximately equal the output power,

$$< P_{in} > \approx P_{OUT} \tag{5}$$

However since the input power has 120Hz ripple, the “peak” input power P_{IN-PK} will be equal to twice the output power,

$$P_{IN-PK} \approx \left(2 \times P_{OUT}\right) \tag{6}$$

Figure 30 illustrates the input current going into the primary side winding of the flyback transformer over one-half of a rectified input voltage line cycle.

The worst-case average input current is calculated at the minimum peak input voltage and targeted converter efficiency η,

$$I_{IN-AVE} = \frac{2 \times P_{OUT}}{\eta \times V_{IN-PK(MIN)}} \tag{7}$$

where,

$$V_{IN-PK(MIN)} = V_{IN(MIN)} \sqrt{2} \tag{8}$$

Next the worst-case peak input current $i_{IN-PK(MAX)}$ is calculated. From Figure 30, the area of the triangle (highlighted with the dashed oval) is the average input current. Therefore,

$$i_{IN-PK(MAX)} = \frac{2 \times I_{IN-AVE}}{D} \tag{9}$$

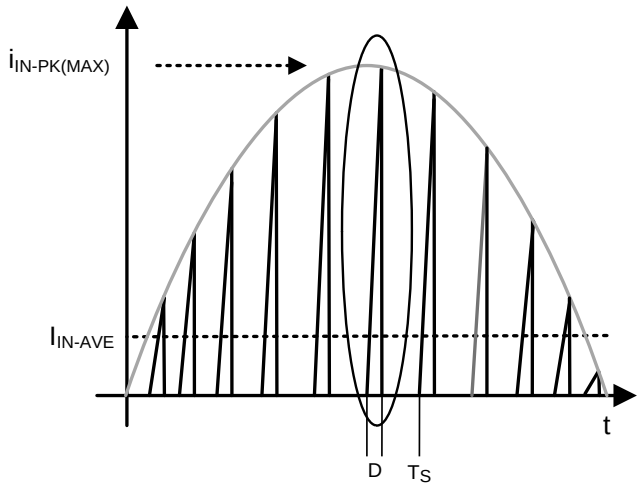


Figure 30. DCM Flyback Current Waveforms

Switching MOSFET (SW FET)

From its datasheet, the LM3448’s SW FET voltage breakdown rating $V_{DS(MAX)}$ is 600V. Due to a transformer’s inherent leakage inductance, some ringing V_{RING} on the drain of the SW FET will be present and must also be taken into consideration when choosing a turns ratio. V_{RING} will depend on the design of the transformer. A good starting point is to design for 50V of ringing while planning for 100V of ringing if additional margin is needed.

The maximum reflected voltage V_{REFL} based on a turns ratio of “n” at the primary also needs to be calculated,

$$V_{REFL} = V_{OUT} \times n \tag{10}$$

The maximum SW FET drain-to-source voltage is then calculated based on the maximum reflected voltage V_{REFL}, ringing on the SW FET drain and the maximum peak input voltage $V_{IN\text{-}PK(MAX)}$,

$$V_{DS(MAX)} = V_{RING} + V_{REFL} + V_{IN\text{-}PK(MAX)} \quad (11)$$

where,

$$V_{IN\text{-}PK(MAX)} = V_{IN(MAX)}\sqrt{2} \quad (12)$$

and the following condition must be met,

$$V_{DS(MAX)} < 600V \quad (13)$$

Peak and RMS SW FET currents are calculated along with maximum SW FET power dissipation based on the SW FET $R_{DS\text{-}ON}$ value,

$$I_{SWFET\text{-}PK(MAX)} = I_{IN\text{-}PK(MAX)} = \frac{2 \times I_{IN\text{-}AVE}}{D} \quad (14)$$

$$I_{SWFET\text{-}RMS(MAX)} = I_{IN\text{-}PK(MAX)} \times \sqrt{\frac{D}{3}} \quad (15)$$

$$P_{SWFET(MAX)} = I_{SWFET\text{-}RMS(MAX)}^{2} \times R_{DS\text{-}ON} \quad (16)$$

Current Limit

The peak current limit I_{LIM} should be at least 25% higher than the maximum peak input current,

$$(R13 \| R14) = \frac{1.27V}{I_{LIM}} = \frac{1.27V}{1.25 \times I_{SWFET\text{-}PK(MAX)}} \quad (17)$$

The parallel sense resistor combination will need to dissipate the maximum power,

$$P_{(R13 \| R14)} = I_{SWFET\text{-}RMS(MAX)}^{2} \times (R13 \| R14) \quad (18)$$

Re-circulating Diode

The main re-circulating diode (D4) should be sized to block the maximum reverse voltage $V_{RD4(MAX)}$, operate at the maximum average current $I_{D4(MAX)}$, and dissipate the maximum power $P_{D4(MAX)}$ as determined by the following equations,

$$V_{RD4(MAX)} = V_{OUT} + \left(\frac{V_{IN\text{-}PK(MAX)}}{n}\right) \quad (19)$$

$$I_{D4(MAX)} = I_{OUT} \quad (20)$$

$$P_{D4(MAX)} = I_{D4(MAX)} \times V_{f(D4)} \quad (21)$$

13.2 Transformer

Primary Inductance

The maximum peak input current $i_{IN\text{-}PK(MAX)}$ occurring at the minimum AC voltage peak $V_{IN\text{-}PK(MIN)}$ determines the worst case scenario that the converter must be designed for in order to stay in DCM. Using the equation for inductor voltage,

$$v = L\frac{di}{dt} \quad (22)$$

and rearranging with the previously calculated parameters,

$$L_{CRIT} = \frac{V_{IN-PK(MIN)} \times D}{f_{SW} \times I_{IN-PK(MAX)}} \quad (23)$$

provides an inductance L_{CRIT} where the flyback converter will operate at the boundary of CCM for a switching frequency f_{SW}. In order to ensure DCM operation, a general rule of thumb is to pick a primary inductance L_P at 85% of the L_{CRIT} value.

Transformer Geometries and Materials

The length of the gap necessary for energy storage in the flyback transformer can be determined numerically; however, this can lead to non-standard designs. Instead, an appropriate A_L core value (a value somewhere between 65nH/turns^2 and 160nH/turns^2 is a good starting point) can be chosen that will imply the gap size. A_L is an industry standard used to define how much inductance, per turns squared, that a given core can provide. With the initial chosen A_L value, the number of turns on the primary and secondary are calculated,

$$N_P = \sqrt{\frac{L_P}{A_L}} \quad (24)$$

$$N_S = \frac{N_P}{n} \quad (25)$$

Given the target operating frequency and the maximum output power, a core size can be chosen using the vendor's specifications and recommendations. This choice can then be validated by calculating the maximum operating flux density given the core cross-sectional area A_e of the chosen core,

$$B_{MAX} = \frac{L_P \times i_{IN-PK(MAX)}}{N_P \times A_e} \quad (26)$$

With most common core materials, the maximum operating flux density should be set somewhere between 250mT and 300mT. If the calculation is below this range, then A_L should be increased to the next standard value and the turns and maximum flux density calculations iterated. If the calculation is above this range, then A_L should be decreased to the next standard value and the turns and maximum flux density calculations iterated. With the flux density appropriately set, the core material for the chosen core size can be determined using the vendor's specifications and recommendations. Note that there are core materials that can tolerate higher flux densities; however, they are usually more expensive and not practical for these designs. The rest of the transformer design can be done with the aid of the manufacturer. There are calculated trade-offs between the different loss mechanisms and safety constraints that determine how well a transformer performs. This is an iterative process and can ultimately result in the choice of a new core or switching frequency range. The previous steps should reduce the number of iterations significantly but a good transformer manufacturer is invaluable for completion of the process.

Clamp

Figure 31 shows a large ringing (V_{RING}) on the SW FET drain due to the leakage inductance of the transformer and output capacitance of SW FET.

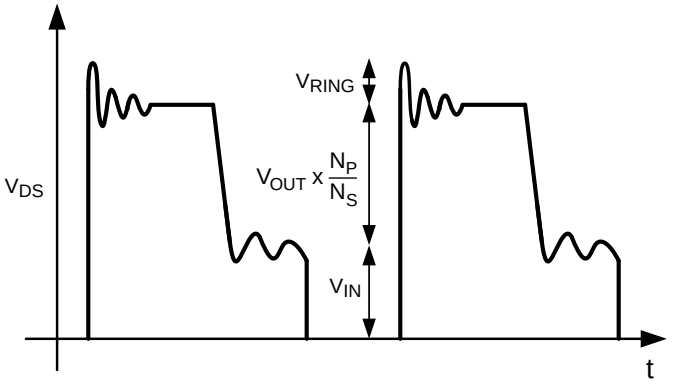


Figure 31. Switch Node Ringing

A clamp circuit is necessary to prevent damage to SW FET from excessive voltage. This evaluation board uses a transient voltage suppression (TVS) clamp D1, shown in Figure 32.

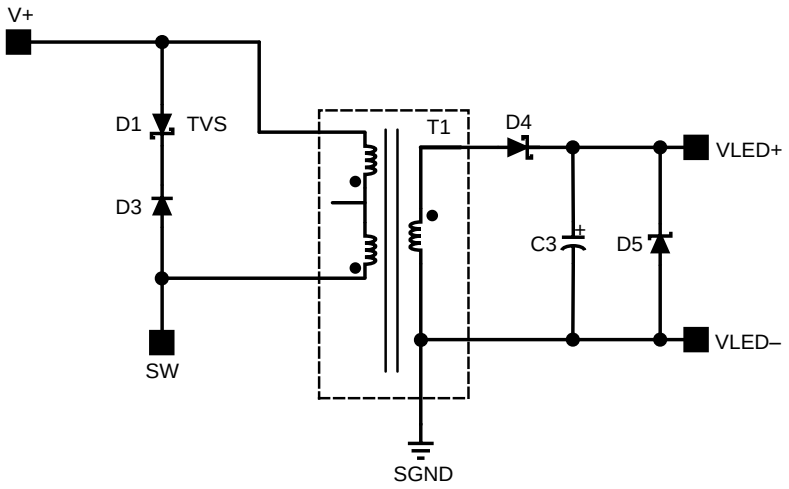


Figure 32. TVS Diode Clamp

When the LM3448's internal SW FET is on and the drain voltage is low, the blocking diode (D3) is reverse biased and the clamp is inactive. When the SW FET is turned off, the drain voltage rises past the nominal voltage (reflected voltage plus the input voltage). If it reaches the TVS clamp voltage plus the input voltage, the clamp prevents any further rise. The TVS diode (D1) voltage is set to prevent the SW FET from exceeding its maximum rating and should be greater than the "output voltage x turns ratio" but less than the expected amount of ringing,

$$V_{TVS-D1} = \frac{3}{2} \times V_{REFL} \quad (27)$$

This clamp method is fairly efficient and very simple compared to other commonly used methods. Note that if the ringing is large enough that the clamp activates, the ringing energy is radiated at higher frequencies. Depending on PCB layout, EMI filtering method, and other application specific items, the clamp can present problems with regards to meeting radiated EMI standards. If the TVS clamp becomes problematic, there are many other clamp options easily found in a basic literature search.

13.3 Bias Supplies and Capacitances

The bias supply circuits shown in Figure 33 and Figure 34 enables instant turn-on through Q1 while providing an auxiliary winding for high efficiency steady state operation. The two bias paths are each connected to VCC through a diode (D8, D9) to ensure the higher of the two is providing V_{CC} current.

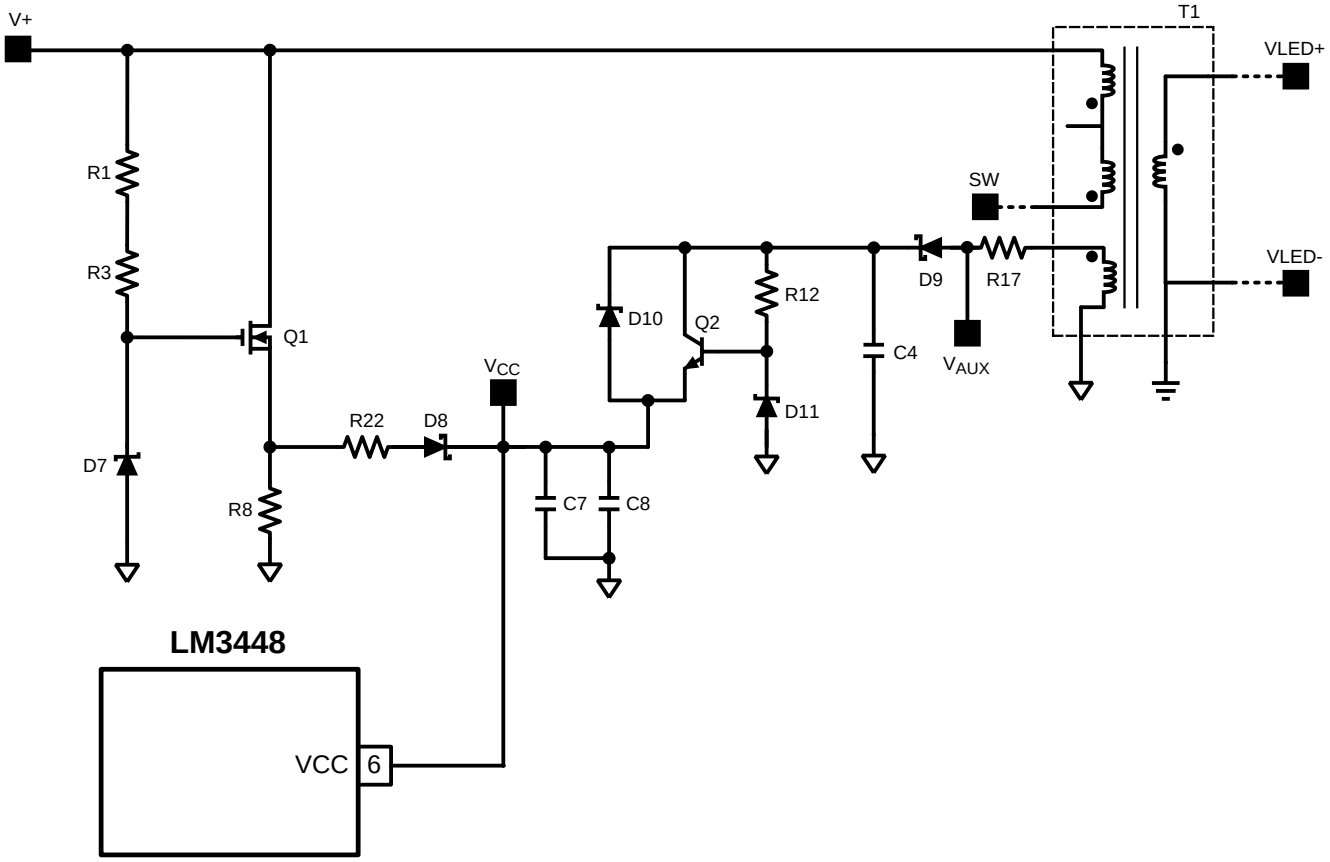


Figure 33. Bias Supply Circuits

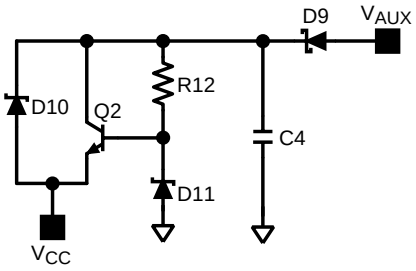


Figure 34. Auxiliary Winding Bias Circuit

PassFET Bias Circuit

The passFET (Q1) is used in its linear region to stand-off the line voltage from the LM3448 regulator. Both the V_{CC} startup current and discharging of the EMI filter capacitance for proper phase angle detection are handled by Q1. Therefore Q1 has to block the maximum peak input voltage and have both sufficient surge and power handling capability with regards to its safe operating area (SOA). The design equations are,

$$V_{Q1} = V_{IN\text{-}PK(MAX)} \quad (28)$$

$$I_{Q1} = \frac{V_{Z(D7)} - V_{GS(Q1)}}{R8} \quad (29)$$

$$P_{Q1} \approx V_{Q1} \times I_{Q1} \quad (30)$$

Note that if additional TRIAC holding current is to be sourced through Q1, then the transistor will need to be sized appropriately to handle the additional current and power dissipation requirements.

Auxiliary Winding Bias Circuit

For high efficiency during steady-state operation, an additional winding is used to establish an auxiliary voltage V_{AUX} used to provide a V_{CC} bias voltage. A minimum value of 13V is recommended for V_{AUX}. An auxiliary transformer turns ratio n_{AUX} and corresponding turns calculation is used to size the primary auxiliary winding N_A,

$$n_{AUX} = \frac{V_{OUT}}{V_{AUX}} \quad (31)$$

$$N_A = \frac{N_S}{n_{AUX}} \quad (32)$$

The minimum primary bias supply capacitance (C7||C8), given a minimum V_{CC} ripple specification at twice the line frequency f_{2L}, is calculated to keep V_{CC} above UVLO at the worst-case current,

$$(C7||C8) = \frac{I_{CC}}{\Delta V_{CC} \times f_{2L}} \quad (33)$$

Input Capacitance

The input capacitor of the flyback (C1) has to be able to provide energy during the worst-case switching period at the peak of the AC voltage input. C1 should be a high frequency, high stability capacitor (usually a metallized film capacitor, either polypropylene or polyester) with an AC voltage rating equal to the maximum input voltage. C1 should also have a DC voltage rating exceeding the maximum peak input voltage + half of the peak to peak input voltage ripple specification. The minimum required input capacitance is calculated given the same ripple specification,

$$C1 = \frac{L_P \times I_{P-PK(MAX)}^2}{\left(V_{IN-PK(MIN)} + \frac{\Delta V_{IN-PK}}{2}\right)^2 - \left(V_{IN-PK(MIN)} - \frac{\Delta V_{IN-PK}}{2}\right)^2} \quad (34)$$

Output Capacitance

C3 should be a high quality electrolytic capacitor with a voltage rating greater than the specified over-voltage protection threshold V_{OVP}. Given the desired voltage ripple, the minimum output capacitance is calculated,

$$C3 = \frac{P_{OUT}}{\left(2\pi \times f_L \times V_{OUT} \times \Delta V_{OUT}\right)} \quad (35)$$

13.4 COFF Current Source

The current source used to establish the constant off-time is shown in Figure 35. Capacitor C12 will be charged with a constant current through resistor R16. A zener diode D6 is placed across R16 which establishes a stable voltage reference for the current source with inherent V_{CC} ripple rejection.

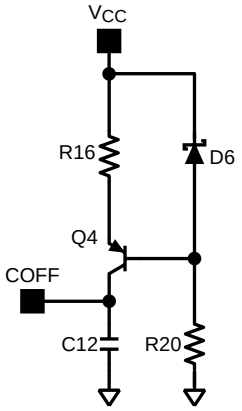


Figure 35. COFF Current Source Circuit

The current that charges up capacitor C12 is set up by the voltage across resistor R16,

$$i_C = \frac{\left(V_{Z(D6)} - V_{BE(Q4)}\right)}{R16} \tag{36}$$

Typically the current through R16 is a value between 40µA and 100µA,

$$R16 = \frac{\left(V_{Z(D6)} - V_{BE(Q4)}\right)}{i_C} \tag{37}$$

For capacitor C12 it is also known that,

$$i_C = C \times \frac{dv}{dt} \tag{38}$$

or,

$$i_C = C12 \times \frac{1.276V}{t_{off}} \tag{39}$$

The off-time t_{OFF} is then calculated where T_s is the switching period,

$$t_{OFF} = T_S - \left(D \times T_S\right) \tag{40}$$

Re-arranging and substituting equations shows,

$$C12 = \frac{t_{OFF} \times \left(V_{Z(D6)} - V_{BE(Q4)}\right)}{R16 \times \left(1.276V\right)} \tag{41}$$

13.5 TRIAC Holding Circuit

An optional TRIAC holding current circuit is also provided on the evaluation board as shown in Figure 36. The DIM pin signal is applied through an RC filter as a varying DC voltage to Q3 such that the voltage on the FLTR2 pin is adjusted and additional holding current can be sinked.

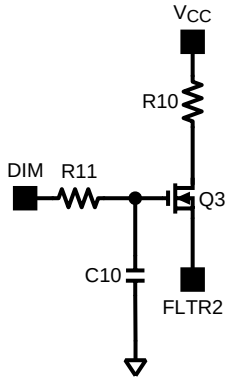


Figure 36. TRIAC Holding Circuit

13.6 Overvoltage Protection

The circuit described in Figure 37 provides over-voltage protection (OVP) in case of LED open circuit failure. The use of this circuit is recommended for stand-alone LED driver designs where it is essential to recover from a momentary open circuit without damaging any part of the circuit. In the case of an integrated LED lamp (where the LED load is permanently connected to the driver output) a simple zener diode or TVS based overvoltage protection is suggested as a cost effective solution. The zener diode/TVS offers protection against a single open circuit event and prevents the output voltage from exceeding the regulatory limits. Depending on the LED driver design specifications, either one or both techniques can be used to meet the target regulatory agency approval

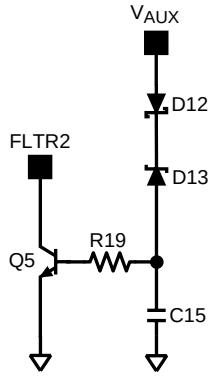


Figure 37. OVP Circuit

The OVP threshold is programmable and is set by selecting appropriate value of zener diode D13. The resistor capacitor (R19, C15) combination across the base of transistor Q5 is used to filter the voltage ripple present on the auxiliary voltage and prevent false OVP tripping due to voltage spikes caused by leakage inductance.

The circuit operation is simple and based on biasing of transistor Q5 during fault conditions such that it pulls down the voltage on the FLTR2 pin to ground. The bias current depends on how much overdrive voltage is generated above the zener diode threshold. For proper circuit operation, it is recommended to design for 4V overdrive in order to adequately bias the transistor. Therefore the zener diode should be selected based on the expression,

$$V_Z = \frac{N_A}{N_S} \times V_{OVP} - 4 \quad (42)$$

where, V_Z is the zener diode threshold, N_A and N_S are the number of transformer auxiliary and secondary turns respectively, and V_{OVP} is the maximum specified output voltage.

13.7 Input Filter

Background

Since the LM3448 is used for AC to DC systems, electromagnetic interference (EMI) filtering is critical to pass the necessary standards for both conducted and radiated EMI. This filter will vary depending on the output power, the switching frequencies, and the layout of the PCB. There are two major components to EMI: differential noise and common-mode noise. Differential noise is typically represented in the EMI spectrum below approximately 500kHz while common-mode noise shows up at higher frequencies.

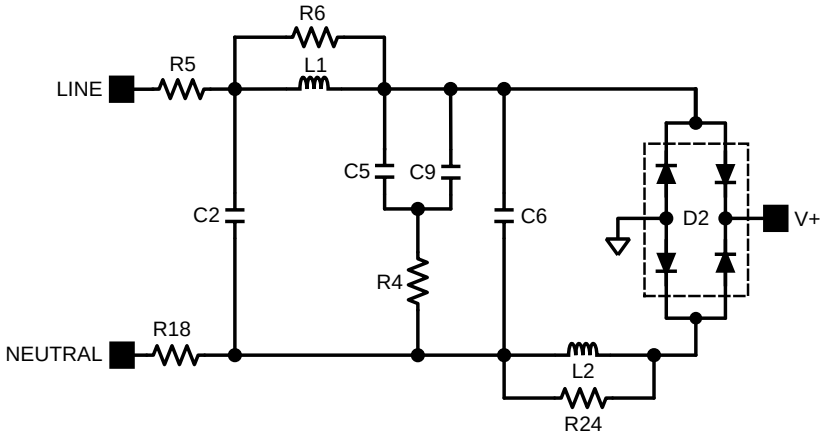


Figure 38. Input EMI Filter

Conducted

Figure 38 shows a typical filter used with this LM3448 flyback design. In order to conform to conducted standards, a fourth order filter is implemented using inductors and "X" rated AC capacitors. If sized properly, this filter design can provide ample attenuation of the switching frequency and lower order harmonics contributing to differential noise. A "Y" rated AC capacitor (C13) from the primary ground to the secondary ground is also critical for reduction of common-mode noise (refer to "Evaluation Board Schematic". This combination of filters along with any necessary damping can easily provide a passing conducted EMI signature.

Radiated

Conforming to radiated EMI standards is much more difficult and is completely dependent on the entire system including the enclosure. C13 will also help reduce radiated EMI; however, reduction of dV/dt on switching edges and PCB layout iterations are frequently necessary as well. Consult available literature and/or an EMI specialist for help with this. Several iterations of component selection and layout changes may be necessary before passing a specific radiated EMI standard.

Interaction with Dimmers

In general input filters and forward phase dimmers do not work well together. The TRIAC needs a minimum amount of holding current to function. The converter itself is demanding a certain amount of current from the input to provide to its output, and the input filter is providing or taking current depending upon the dV/dt of the capacitors. The best way to deal with this problem is to minimize filter capacitance and increase the regulated hold current until there is enough current to satisfy the dimmer and filter simultaneously.

13.8 Inrush Limiting and Damping

Inrush

With a forward phase dimmer, a very steep rising edge causes a large inrush current every cycle as shown in Figure 39. Series resistance (R5, R18) can be placed between the filter and the TRIAC to limit the effect of this current on the converter and to provide some of the necessary holding current at the same time. This will degrade efficiency but some inrush protection is always necessary in any AC system due to startup. The size of R5 and R18 are best found experimentally as they provide attenuation for the whole system.

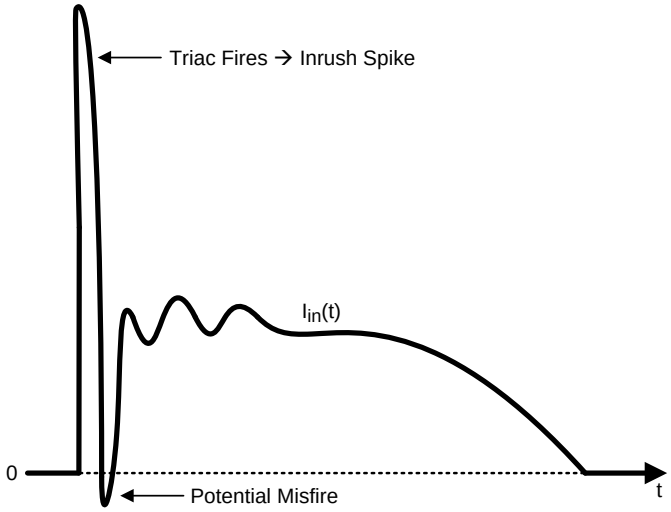


Figure 39. Inrush Current Spike

Damper

The inrush spike can also excite a resonance between the input filter of the TRIAC and the input filter of the converter. The associated interaction can cause the current to ring negative, as shown in Figure 39, thereby shutting off the TRIAC. A TRIAC damper can be placed between the dimmer and the EMI filter to absorb some of the ringing energy and reduce the potential for misfires. The damper is also best sized experimentally due to the large variance in TRIAC input filters. Resistors R5 and R18 can also be increased to help dampen the ringing at the expense of some efficiency and power factor performance.

14 Design Calculations

The following is a step-by-step procedure with calculations for a 120V, 6.5W flyback design.

14.1 Specifications

f_L = 60Hz

$f_{SW(MIN)}$ =72kHz

$V_{IN(NOM)}$ = 120VAC

$V_{IN(MIN)}$ = 85VAC

$V_{IN(MAX)}$ = 135VAC

I_{LED} = 245mA

Δv_{OUT} = 1V

Δv_{IN-PK} = 35V

SW FET $V_{DS(MAX)}$ = 600V

SW FET R_{DS-ON} = 3.5Ω

$V_{f(D4)}$ = 0.8V

V_{RING} = 50V

$P_{OUT(MAX)}$ = 6.5W

V_{OUT} = 26.5V

V_{OVP} = 47V

V_{AUX} = 13V

η = 85%

n = 4

A_L = 80nH/turns^2

A_e = 19.49mm^2

V_{CC} = 12V

$V_{Z(D6)}$ = 5.1V

$V_{BE(Q4)}$ = 0.7V

$V_{Z(D7)}$=12V

R8=49.9kΩ

$V_{GS(Q1)}$=0.7V

14.2 Preliminary Calculations

Nominal peak input voltage:

$$V_{IN-PK(NOM)} = 120V\sqrt{2} = 170V \quad (43)$$

Maximum peak input voltage:

$$V_{IN-PK(MAX)} = 135V\sqrt{2} = 191V \quad (44)$$

Minimum peak input voltage:

$$V_{IN-PK(MIN)} = 85V\sqrt{2} = 120V \quad (45)$$

Maximum average input current:

$$I_{IN-AVE}=\frac{2\times 6.5W}{0.85\times 120V}=0.127A \quad (46)$$

Duty cycle:

$$D=\frac{(26.5V\times 4)}{(26.5V\times 4)+170V}=38.4\% \quad (47)$$

Maximum peak input current:

$$I_{IN-PK(MAX)}=\frac{(2\times 0.127A)}{0.384}=0.662A \quad (48)$$

14.3 SW FET

Maximum reflected voltage:

$$V_{REFL}=26.5V\times 4=106V \quad (49)$$

Maximum drain-to-source voltage:

$$V_{DS(MAX)}=50V+106V+191V=347V \quad (50)$$

Maximum peak MosFET current:

$$I_{SWFET-PK(MAX)}=0.662A \quad (51)$$

Maximum RMS MosFET current:

$$I_{SWFET-RMS(MAX)}=0.662A\times\sqrt{\frac{0.384}{3}}=0.237A \quad (52)$$

Maximum power dissipation:

$$P_{SWFET(MAX)}=(0.237A)^2\times 3.5\Omega=0.196W \quad (53)$$

14.4 Current Sense

Current Limit:

$$I_{LIM}=1.25\times 0.662A=0.827A \quad (54)$$

Sense resistor:

$$R_{SNS}=(R13||R14)=\frac{1.27V}{0.827A}=1.54\Omega \quad (55)$$

Power dissipation:

$$P_{(R13||R14)}=(0.237A)^2\times 1.54\Omega=0.086W \quad (56)$$

Resulting component choice:

$$R13=DNP$$
$$R14=1.54\Omega,0.25W \quad (57)$$

14.5 Recirculating Diode

Maximum reverse blocking voltage:

$$V_{RD4(MAX)} = 26.5V + \frac{191V}{4} = 74.3V \quad (58)$$

Maximum peak diode current:

$$I_{D4\text{-}PK(MAX)} = 0.662V \times 4 = 2.65A \quad (59)$$

Maximum average diode current:

$$I_{D4(MAX)} = 0.245A \quad (60)$$

Maximum power dissipation:

$$P_{D4(MAX)} = 0.245A \times 0.8V = 0.196W \quad (61)$$

Resulting component choice:

$$D4 = 100V, 1A \quad (62)$$

14.6 Transformer

Calculated primary inductance:

$$L_{CRIT} = \frac{120V \times 0.384}{72kHz \times 0.662A} = 970\mu H \quad (63)$$

Chosen primary inductance:

$$L_P = 0.85 \times L_{CRIT} = 824\mu H \quad (64)$$

Number of primary turns:

$$N_P = \sqrt{\frac{824\mu H}{80nH/turns^2 \times (1E\text{-}9)}} = 102turns \quad (65)$$

Number of secondary turns:

$$N_S = \frac{102}{4} = 26turns \quad (66)$$

Number of auxiliary turns:

$$n_{AUX} = \frac{26.5V}{13V} = 2.04 \quad (67)$$

$$N_A = \frac{26}{2.04} = 13turns \quad (68)$$

Maximum flux density:

$$B_{MAX} = \frac{824\mu H \times 0.662A}{102 \times 19.49mm^2} \times 1E6 = 0.276T \quad (69)$$

Resulting component choice:

$$N_P = 102\text{turns}$$
$$N_S = 26\text{turns}$$
$$N_A = 13\text{turns} \quad (70)$$

14.7 COFF Current Source

Calculate off-time,

$$t_{OFF} = 13.9\mu s - (0.384 \times 13.9\mu s) = 8.5\mu s \quad (71)$$

Choose current through resistor R16: 50µA

Calculate R16,

$$R16 = \frac{(5.1V - 0.7V)}{50\mu A} = 88k\Omega \quad (72)$$

Calculate capacitor C12,

$$C12 = \frac{8.5\mu s \times (5.1V - 0.7V)}{88k\Omega \times (1.276V)} = 335pF \quad (73)$$

14.8 PassFET

Calculate maximum peak voltage:

$$V_{Q1} = V_{IN-PK(MAX)} = 191V \quad (74)$$

Calculate current:

$$I_{Q1} = \frac{12V - 0.7V}{49.9k\Omega} = 226\mu A \quad (75)$$

Calculate power dissipation:

$$P_{Q1} \approx 191V \times 226\mu A = 40mW \quad (76)$$

Resulting component choice:

$$Q1 = 260mA, 240V \quad (77)$$

14.9 Input Capacitance

Minimum capacitance:

$$C1 = \frac{(824\mu H \times 0.662A)^2}{\left(120V + \frac{35V}{2}\right)^2 - \left(120V - \frac{35V}{2}\right)^2} = 43nF \quad (78)$$

AC Voltage rating:

$$V_{C2(AC\ Rating)} > 135VAC \quad (79)$$

DC Voltage rating:

$$V_{C2(DC\ Rating)} > 191V + \frac{35V}{2} = 209V \quad (80)$$

Resulting component choice:

$$C1 = 0.047\mu F,\ 200VAC, 400VDC \quad (81)$$

14.10 Output Capacitance

Minimum capacitance:

$$C3 = \frac{6.5W}{(2\pi \times 60Hz \times 26.5V \times 1V)} = 650\mu F \quad (82)$$

Voltage rating:

$$V_{C3} > 47V \quad (83)$$

Resulting component choice:

$$C3 = 680\mu F, 50V \quad (84)$$

14.11 Overvoltage Protection Zener Diode

Calculate Zener diode:

$$V_Z = \left(\frac{13}{26} \times 47V\right) - 4 = 19V \quad (85)$$

Resulting component choice:

$$V_Z = 18V \quad (86)$$

14.12 Transil Clamp

TVS clamp voltage:

$$V_{TVS-D1} = \left(\frac{3}{2}\right) \times 106V = 159V \quad (87)$$

Resulting component choice:

$$D1 = 150V, TVS \quad (88)$$

15 Evaluation Board Schematic

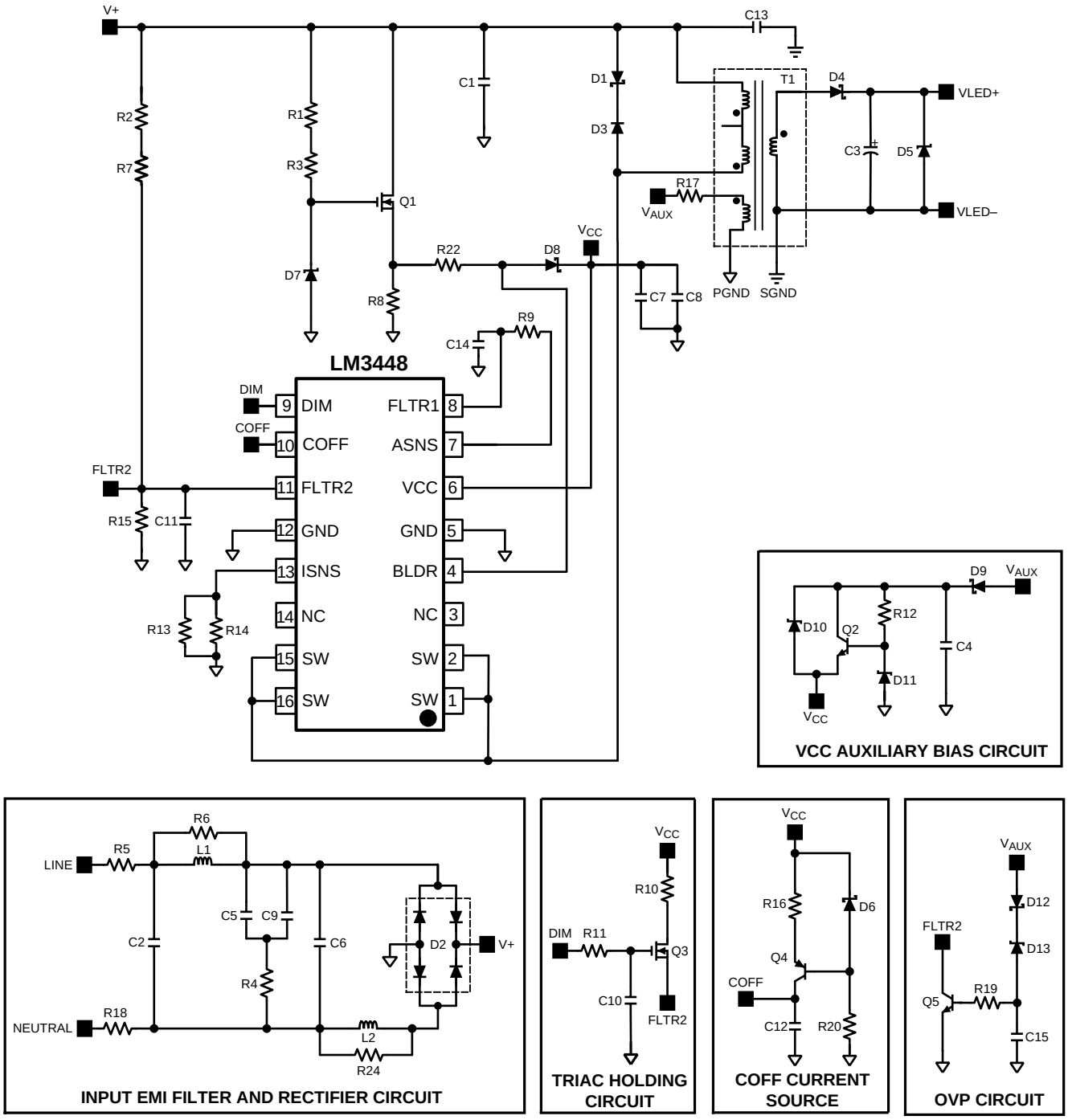


Figure 40. Evaluation Board Schematic

WARNING

The LM3448 evaluation board has exposed high voltage components that present a shock hazard. Caution must be taken when handling the evaluation board. Avoid touching the evaluation board and removing any cables while the evaluation board is operating. Isolating the evaluation board rather than the oscilloscope is highly recommended.

WARNING

The ground connection on the evaluation board is NOT referenced to earth ground. The oscilloscope should be powered via an isolation transformer before an oscilloscope ground lead is connected to the evaluation board.

WARNING

The LM3448 evaluation board should not be powered with an open load. For proper operation, ensure that the desired number of LEDs are connected at the output before applying power to the evaluation board.

Table 3. Bill of Materials

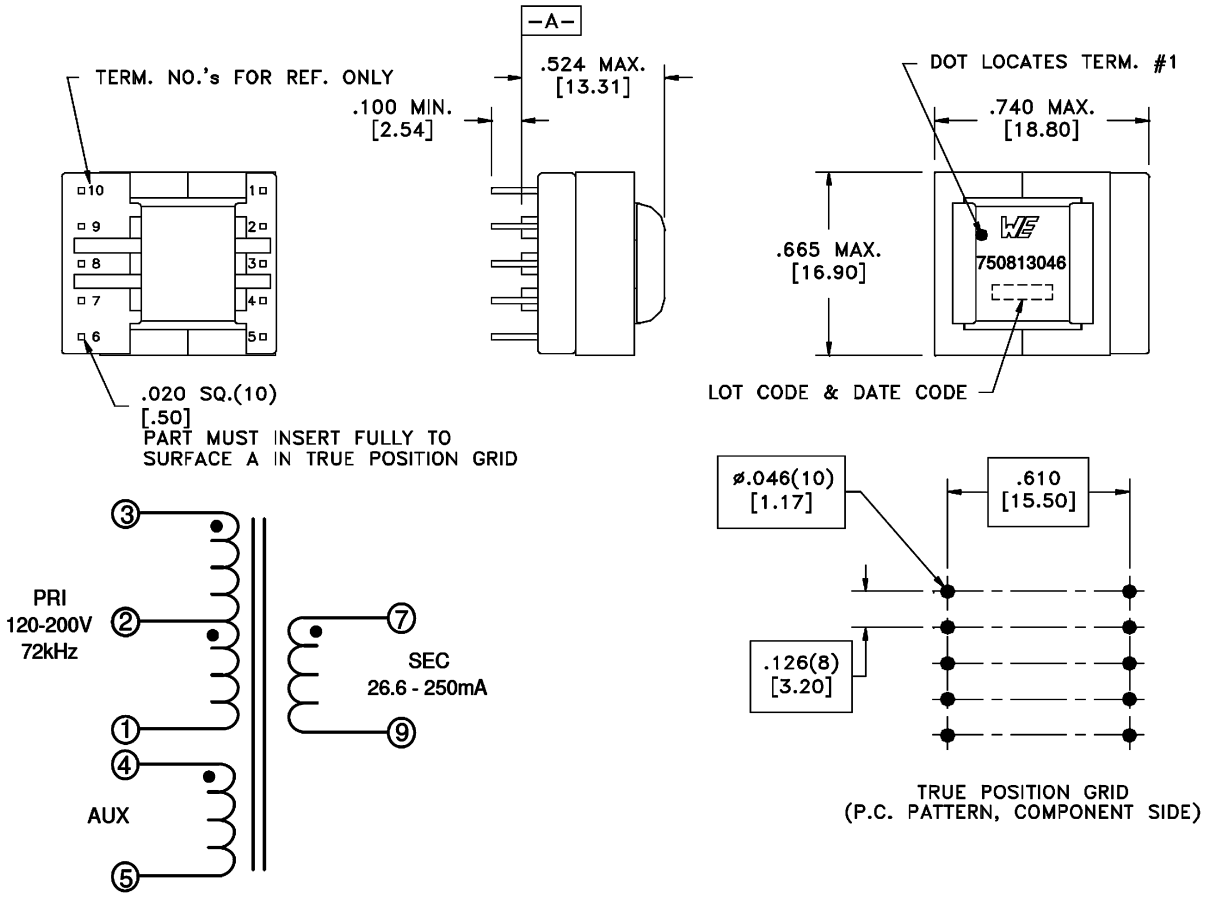
Part ID	Description	Manufacturer	Part Number
C1	CAP .047UF 400V METAL POLYPRO	EPCOS Inc	B32559C6473K000
C2	CAP FILM MKP .015UF 310VAC X2	Vishay/BC Components	BFC233820153
C3	CAP ALUM 680UF 50V 20% RADIAL	Nichicon	UPW1H681MHD
C4, C15	CAP, CERM, 1uF, 35V, +/-10%, X7R, 0805	Taiyo Yuden	GMK212B7105KG-T
C5, C9	CAP CER .15UF 250V X7R 1210	TDK	C3225X7R2E154K
C6	CAP .10UF 305VAC EMI SUPPRESSION	EPCOS	B32921C3104M
C7	CAP, CERM, 0.1µF, 16V, +/-10%, X7R, 0805	Kemet	C0805C104K4RACTU
C8	CAP CER 47UF 16V X5R 1210	MuRata	GRM32ER61C476ME15L
C10	CAP CER .22UF 16V X7R 0603	MuRata	GRM188R71C224KA01D
C11	Ceramic, X7R, 50V, 10%	MuRata	GRM188R71H222KA01D
C12	CAP CER 330PF 50V 5% C0G 0603	MuRata	GRM1885C1H331JA01D
C13	CAP CER 2200PF 250VAC X1Y1 RAD	TDK Corporation	CD12-E2GA222MYNS
C14	CAP CERM .47UF 10% 25V X5R 0805	AVX	08053D474KAT2A
D1	DIODE TVS 120V 400W UNI 5% SMA	Littlefuse	SMAJ120A
D2	Diode, Switching-Bridge, 400V, 0.8A, MiniDIP	Diodes Inc.	HD04-T
D3	DIODE RECT GP 1A 1000V MINI-SMA	Comchip Technology	CGRM4007-G
D4	DIODE SCHOTTKY 100V 1A SMA	ST Microelectronics	STPS1H100A
D5	DIODE ZENER 47V 3W SMB	ON Semi	1SMB5941BT3G
D6	DIODE ZENER 5.1V 200MW SOD-523F	Fairchild Semiconductor	MM5Z5V1
D7	DIODE ZENER 12V 200MW	Fairchild Semiconductor	MM5Z12V
D8	DIODE SWITCH 200V 200MW	Diodes Inc	BAV20WS-7-F

Table 3. Bill of Materials (continued)

D9, D10, D12	IC DIODE SCHOTTKY SS SOD-323	STMicroelectronics	BAT46JFILM
D11	DIODE ZENER 13V 200MW SOD-323	Diodes Inc.	DDZ13BS-7
D13	DIODE ZENER 18V 400MW SOD323	NXP Semi	PDZ18B,115
L1, L2	INDUCTOR 4700UH .13A RADIAL	TDK Corp	TSL0808RA-472JR13-PF
Q1	MOSFET N-CH 240V 260MA SOT-89	Infineon Technologies	BSS87 L6327
Q2	TRANSISTOR NPN 300V SOT23	Diodes Inc	MMBTA42-7-F
Q3	MOSFET, N-CH, 100V, 170A, SOT-323	Diodes Inc.	BSS123W-7-F
Q4	TRANS GP SS PNP 40V SOT323	On Semiconductor	MMBT3906WT1G
Q5	TRANS GP SS NPN 40V SOT323	ON Semi	MMBT3904WT1G
R1, R3	RES, 200k ohm, 1%, 0.25W, 1206	Vishay-Dale	CRCW1206200KFKEA
R2, R7	RES, 309k ohm, 1%, 0.25W, 1206	Vishay-Dale	CRCW1206309KFKEA
R4	RES, 430 ohm, 5%, 0.25W, 1206	Vishay-Dale	CRCW1206430RJNEA
R5, R18	RES 33 OHM 2W 10% AXIAL	TT Electronics/Welwyn	EMC2-33RKI
R6, R24	RES, 10.5k ohm, 1%, 0.125W, 0805	Vishay-Dale	CRCW080510K5FKEA
R8, R11	RES, 49.9k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060349K9FKEA
R9	RES, 100k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW0603100KFKEA
R10	DNP	-	-
R12	RES, 10.0k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060310K0FKEA
R13, R17	RES, 10.0 ohm, 1%, 0.125W, 0805	Vishay-Dale	CRCW080510R0FKEA
R14	RES 2.20 OHM 1/4W 1% 1206 SMD	Vishay/Dale	CRCW12062R20FKEA
R15	RES, 3.48k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW06033K48FKEA
R16	RES, 84.5k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060384K5FKEA
R19	RES, 100 ohm, 1%, 0.125W, 0805	Vishay-Dale	CRCW0805100RFKEA
R20	RES, 30.1k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060330K1FKEA
R22	RES, 40.2 ohm, 1%, 0.125W, 0805	Vishay-Dale	CRCW080540R2FKEA
T1	Transformer	Wurth Electronics Midcom	750813046 Rev. 00
U1	IC LED Driver	Texas Instruments	LM3448

16 Transformer Design

Mfg: Wurth Electronics Midcom, Part #: 750813046 Rev.00



ELECTRICAL SPECIFICATIONS @ 25°C unless otherwise noted:

D.C. RESISTANCE (@20°C):	1-3 , 2.10 Ohms ±10%.
	4-5 , 0.82 Ohms ±10%.
	7-9 , 0.35 Ohms ±10%.
DIELECTRIC RATING:	4500VAC, 1 minute tested by applying 4500VAC for 1 second between pins 3-7 (1+4).
	1000VAC, 1 minute tested by applying 1250VAC for 1 second between pins 3-4.
INDUCTANCE:	1.44 mH ±10%, 10kHz, 100mVAC, 0mADC, 1-3, Ls.
SATURATION CURRENT:	600mA saturating current that causes 20% rolloff from initial inductance.
LEAKAGE INDUCTANCE:	14.0µH typ., 25.0µH max., 100kHz, 100mVAC, 1-3(4+5,7+9), Ls.
TURNS RATIO:	(3-1):(7-9), (3.941):(1.00), ±1%.
	(3-1):(4-5), (8.375):(1.00), ±1%.
	(3-2):(2-1), (1):(1.00), ±1%.

Designed to comply with the following requirements as defined by IEC60950-1, EN60950-1, UL60950-1/CSA60950-1 and AS/NZS60950.1:

- Reinforced insulation for a primary circuit at a working voltage of 400VDC.

17 PCB Layout

NOTE: Spacing between traces and components of this evaluation board are based on high voltage recommendations for designs that will be potted. Users are cautioned to satisfy themselves as to the suitability of this design for the intended end application and take any necessary precautions where high voltage layout and spacing rules must be followed.

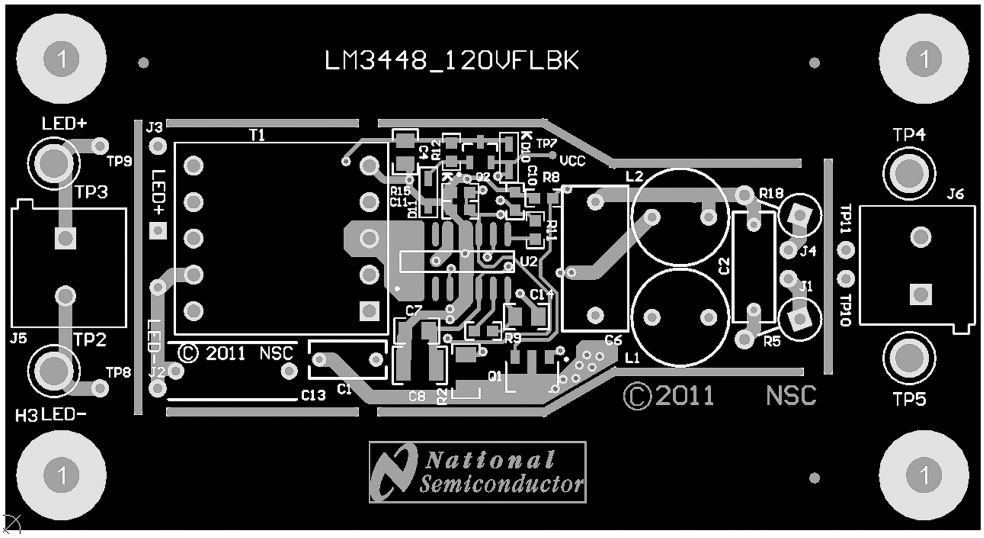


Figure 41. Top Layer

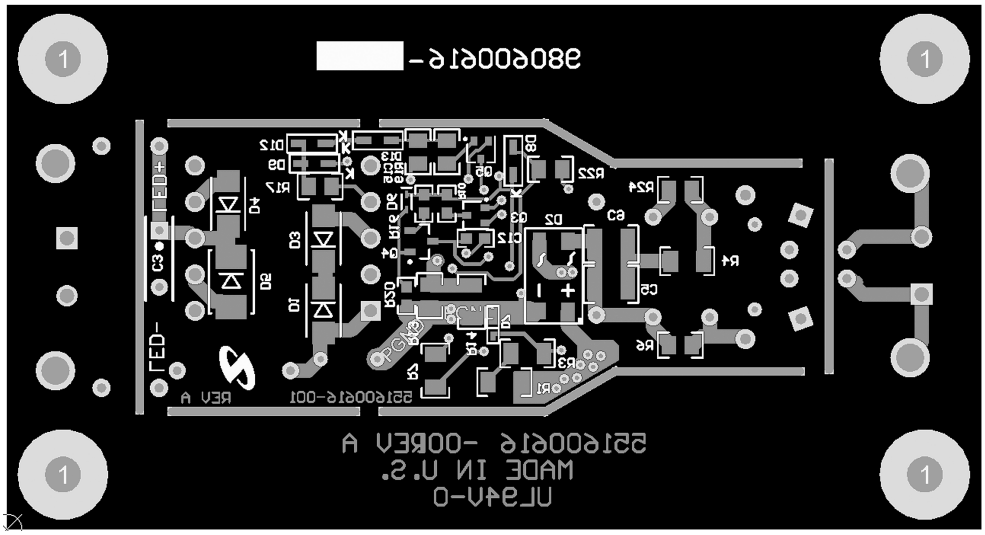


Figure 42. Bottom Layer

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