N a t i o n a l
S e m i c o n d u c t o r ™

FPD-Link Evaluation Kit User's Manual

NSID FLINK3V8BT-85

Rev 3.0

Table of Contents

Introduction:

National Semiconductor - Interface Products Group FPD-Link evaluation kit contains a Transmitter (Tx) board, a Receiver (Rx) board along with interfacing cables. This kit will demonstrate the DS90C385A/DS90CF386 chipsets interfacing from test equipment or a graphics controller using Low Voltage Differential Signaling (LVDS) to a receiver board.

The Transmitter board accepts LVTTL/LVCMOS RGB signals from the graphics controller along with the clock signal. The LVDS Transmitter converts the LVTTL/LVCMOS parallel lines into four serialized LVDS data pairs plus a LVDS clock. The serial data streams toggle at 3.5 times the clock rate.

The Receiver board accepts the LVDS serialized data streams plus clock and converts the data back into parallel LVTTL/LVCMOS RGB signals and clock for the panel timing controller.

The user needs to provide the proper RGB inputs and clock to the Transmitter and also provide a proper interface from the Receiver output to the panel timing controller or test equipment. A cable conversion board or harness scramble may be necessary depending on type of cable/connector interface used. A power down feature is also provided that reduces current draw when the link is not required.

Contents of the Evaluation Kit:

1) One Transmitter board with the DS90C385AMTD - 28 bit Transmitter
2) One Receiver board with the DS90CF386MTD - 28 bit Receiver
3) One 20-pin IDC Flat Ribbon Cable
4) One 60-pin IDC Flat Ribbon Cable
5) Evaluation Kit Documentation (this manual)
6) DS90C385A/DS90CF386 Datasheet
7) LVDS Owner's Manual (2nd Edition)

FPD-Link Typical Application:

FPD-Link Application

Typical FPD-Link Application (24-bit Color)
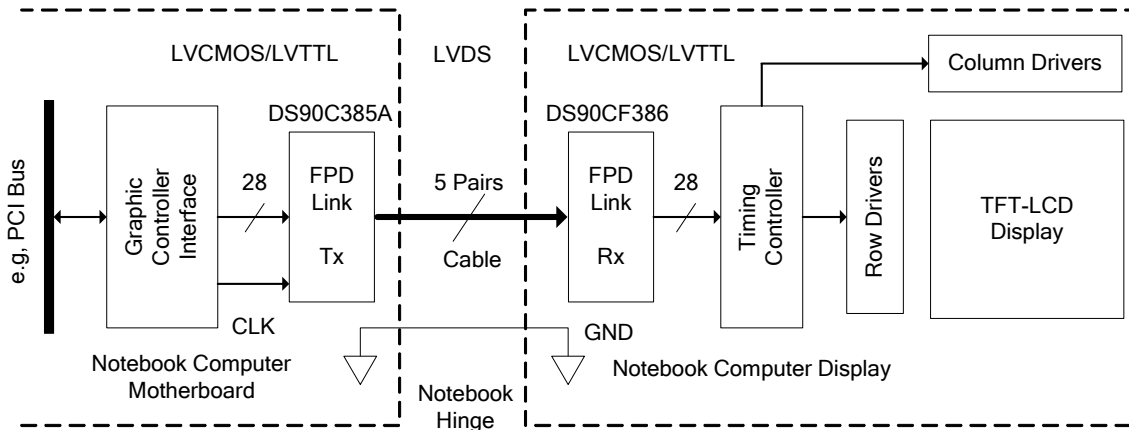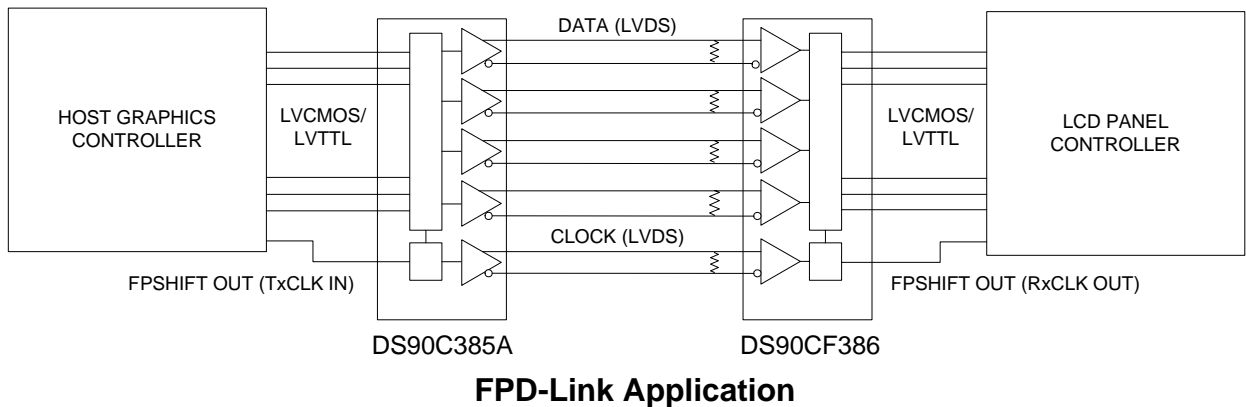
The diagrams above illustrate the use of the Chipset (Tx/Rx) in a Host to LCD Panel Interface.

Chipsets support up to 18-bit or 24-bit AM-TFT LCD Panels for any VGA (640X480), SVGA (800X600), XGA (1024X768), and Single/Dual Pixel SXGA (1280X1024) resolutions.

Because of the non-periodic nature of STN-DD SHFCLK, the Chipset may not work with all D-STN panels. The PLL CLK input of the Transmitter requires a free running periodic SHFCLK. Most Graphics Controller can provide a separate pin with a free running clock. In this case the STN-DD SHFCLK can be sent as Data while the free running clock can be used as SHFCLK for the PLL ref CLK. For example, C&T's 65550's WEC (Pin 102) can be programmed to provide a free running clock using the BMP (Bios Modification Program). Please refer to STN Application using (AN-1056) for more information on STN support.

Refer to the proper datasheet information on Chipsets (Tx/Rx) provided on each board for more detailed information.

How to set up the Evaluation Kit:

The PCB routing for the Tx input pins (TxIN) have been laid out to accept incoming data from a 60-pin IDC connector. The TxOUT/RxIN interface uses a 20-pin IDC connector through a IDC ribbon cable. Please follow these steps to set up the evaluation kit for bench testing and performance measurements:

1) Connect one end of the 20-pin IDC cable to the transmitter board and the other end to the receiver board. Longer lengths can be used.

Note: Previous HSL Tx/Rx 8 Bit boards have different IDC pinouts and must be scrambled in the IDC cable in order to be compatible with this demo kit.

2) Jumpers have been configured at the factory, they should not require any changes for operation of the chipset.   See text on Jumper settings for more details.
3) From the Graphics card, connect a flat (ribbon) cable to the transmitter board and connect the another flat cable from the receiver board to the panel (Note: Refer to AN-1127 for suggested mapping schemes). Note that pin 1 on the connector should be connected to pin 1 of the cable. A scramble cable may be required.
4) Power for the Tx and Rx boards must be supplied externally through TP1 (Vcc). Grounds for both boards are connected through TP2 (GND) (see section below).

Power Connection:

The Transmitter and Receiver boards must be powered by supplying power externally through TP1 (Vcc) and TP2 (GND) on EACH board. The maximum voltage that should ever be applied to the FPD-Link Transmitter (385A) or Receiver (386) Vcc terminal is +4V MAXIMUM.
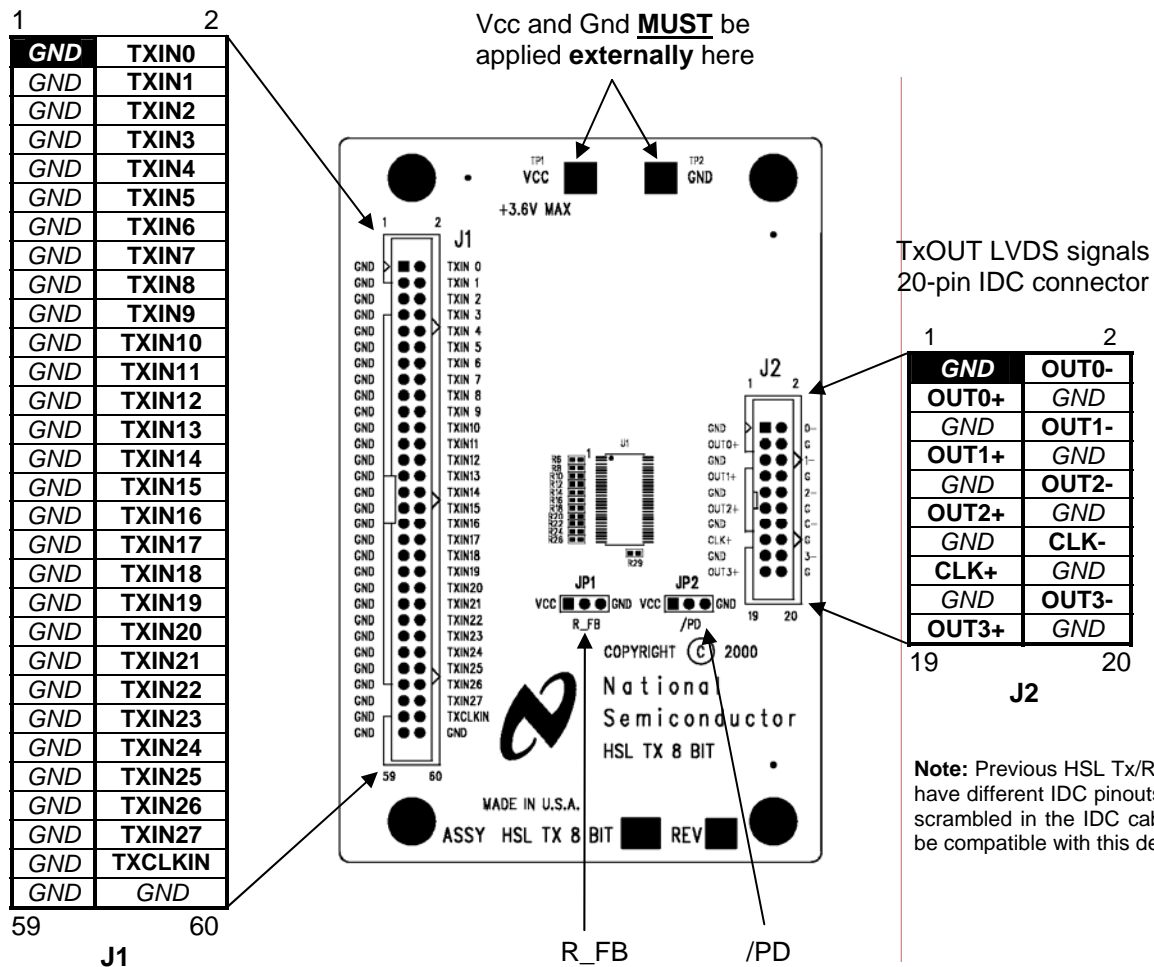
FPD-Link Transmitter Board Description:

J1 (60 position) accepts 28 bit LVTTL/LVCMOS data along with the clock.

The FPD-Link Transmitter board is powered externally. For the transmitter to be operational, the Power Down pin must be set HIGH with a jumper. Rising or falling edge reference clock is selected by JP1 tied to Vcc (rising) or GND (falling).

The 20-pin IDC connector (J2) provides the interface for LVDS signals for the Receiver board.

Note: Previous HSL Tx/Rx 8 Bit boards have different IDC pinouts and must be scrambled in the IDC cable in order to be compatible with this demo kit.

60-pin IDC Connector

Vcc and Gnd **MUST** be applied **externally** here

TxOUT LVDS signals
20-pin IDC connector

1	2
GND	**OUT0-**
OUT0+	*GND*
GND	**OUT1-**
OUT1+	*GND*
GND	**OUT2-**
OUT2+	*GND*
GND	**CLK-**
CLK+	*GND*
GND	**OUT3-**
OUT3+	*GND*

19   20

J2

Note: Previous HSL Tx/Rx 8 Bit boards have different IDC pinouts and must be scrambled in the IDC cable in order to be compatible with this demo kit.

1	2
GND	**TXIN0**
GND	**TXIN1**
GND	**TXIN2**
GND	**TXIN3**
GND	**TXIN4**
GND	**TXIN5**
GND	**TXIN6**
GND	**TXIN7**
GND	**TXIN8**
GND	**TXIN9**
GND	**TXIN10**
GND	**TXIN11**
GND	**TXIN12**
GND	**TXIN13**
GND	**TXIN14**
GND	**TXIN15**
GND	**TXIN16**
GND	**TXIN17**
GND	**TXIN18**
GND	**TXIN19**
GND	**TXIN20**
GND	**TXIN21**
GND	**TXIN22**
GND	**TXIN23**
GND	**TXIN24**
GND	**TXIN25**
GND	**TXIN26**
GND	**TXIN27**
GND	**TXCLKIN**
GND	*GND*

59   60

J1

R_FB   /PD

Jumper Settings for the Tx Board

<u>Jumper</u>	<u>Purpose</u>	<u>Settings</u>

R_FB   **R**ising or **F**alling   [○ ○] ○ = Rising   ○ [○ ○] = Falling
(JP1)   Data Strobe   Vcc   GND   Vcc   GND

Default setting is JP1 set LOW (to GND), falling edge strobe.

/PD   **P**ower**D**own   [○ ○] ○ = ON   ○ [○ ○] = OFF
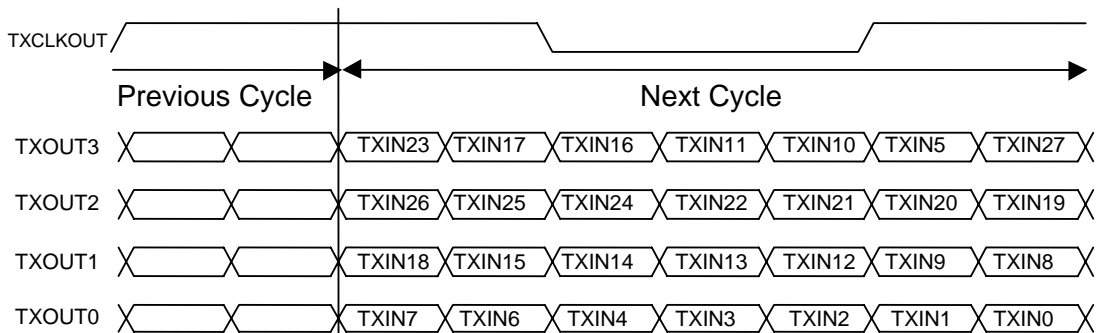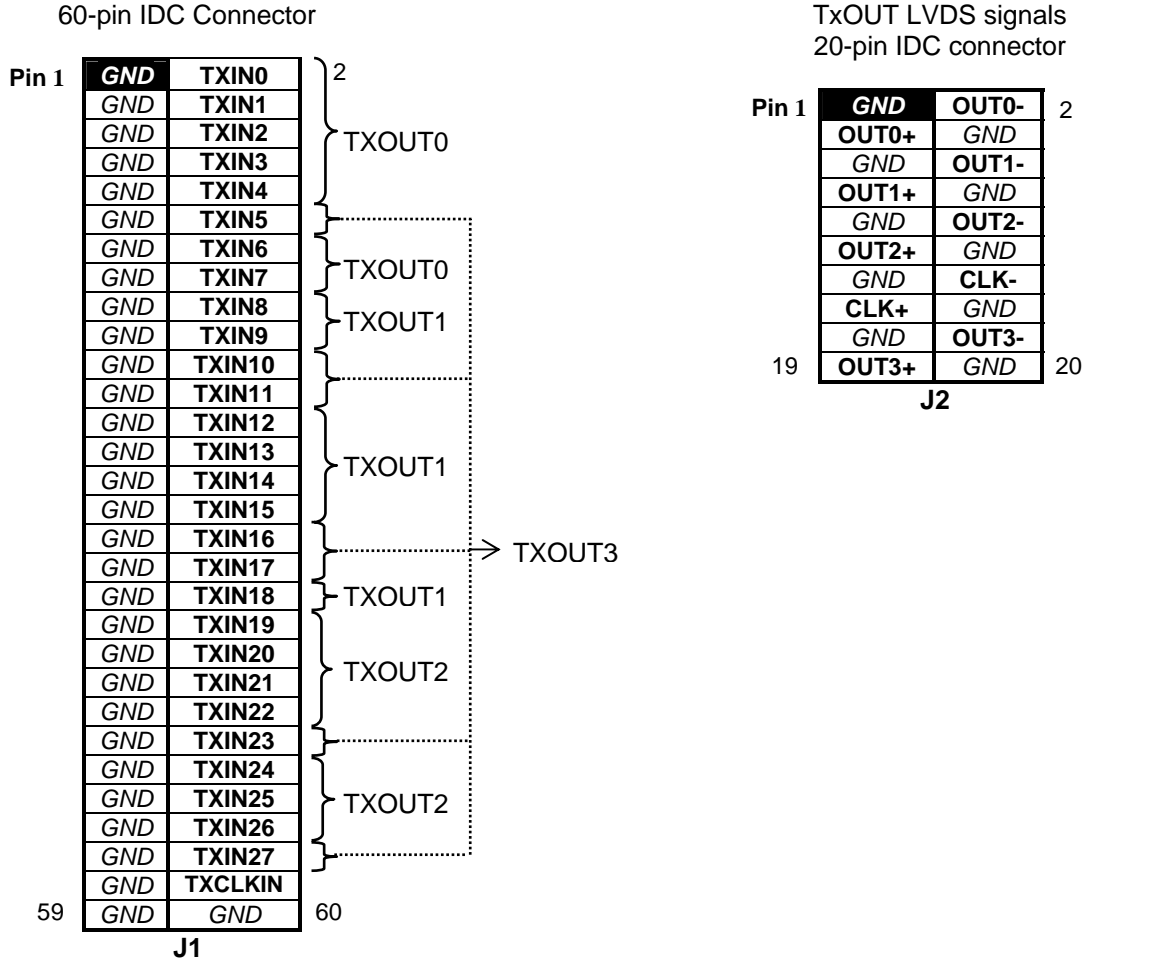(JP2)   Vcc   GND   Vcc   GND
                                         (ON: Tx is operational;   OFF: Tx powers down)

Default setting is JP2 set HIGH (to Vcc), operational mode.

Tx LVDS Mapping by IDC Connector

The following two figures illustrate how the Tx inputs are mapped to the IDC connector (J1) (Note – labels are also printed on the demo boards). The 20-pin IDC (J2) connector pinout is also shown.
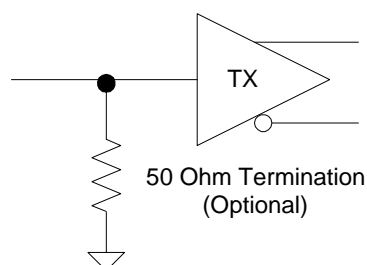
(Transmitter Board)

60-pin IDC Connector

TxOUT LVDS signals
20-pin IDC connector

Pin 1	GND	TXIN0	2
	GND	TXIN1	
	GND	TXIN2	
	GND	TXIN3	
	GND	TXIN4	
	GND	TXIN5	
	GND	TXIN6	
	GND	TXIN7	
	GND	TXIN8	
	GND	TXIN9	
	GND	TXIN10	
	GND	TXIN11	
	GND	TXIN12	
	GND	TXIN13	
	GND	TXIN14	
	GND	TXIN15	
	GND	TXIN16	
	GND	TXIN17	
	GND	TXIN18	
	GND	TXIN19	
	GND	TXIN20	
	GND	TXIN21	
	GND	TXIN22	
	GND	TXIN23	
	GND	TXIN24	
	GND	TXIN25	
	GND	TXIN26	
	GND	TXIN27	
	GND	TXCLKIN	
59	GND	GND	60

J1

TXOUT0
TXOUT0
TXOUT1
TXOUT1
TXOUT1
→ TXOUT3
TXOUT1
TXOUT2
TXOUT2

Pin 1	GND	OUT0-	2
	OUT0+	GND	
	GND	OUT1-	
	OUT1+	GND	
	GND	OUT2-	
	OUT2+	GND	
	GND	CLK-	
	CLK+	GND	
	GND	OUT3-	
19	OUT3+	GND	20

J2

TXCLKOUT

Previous Cycle   Next Cycle

TXOUT3			TXIN23	TXIN17	TXIN16	TXIN11	TXIN10	TXIN5	TXIN27	
TXOUT2			TXIN26	TXIN25	TXIN24	TXIN22	TXIN21	TXIN20	TXIN19	
TXOUT1			TXIN18	TXIN15	TXIN14	TXIN13	TXIN12	TXIN9	TXIN8	
TXOUT0			TXIN7	TXIN6	TXIN4	TXIN3	TXIN2	TXIN1	TXIN0	

Parallel LVTTL/LVCMOS Data Inputs Mapped to LVDS Outputs

Tx Board Options: 50 Ohm Termination for TxIN

On the Tx demo board, the 29 inputs have an option for 50 Ohm terminations. There are 0402 pads for this purpose. One side is connected to the signal line and the other side is tied to ground. These pads are unpopulated from the factory but are provided if the user needs to install a 50 Ohm termination. R1 TO R28 are associated with the Tx data input lines. R29 is associated with CLKIN. Some test equipment may require a 50 Ohm load.

Mapping of Transmitter Inputs for the Optional Termination Resistors is shown below:

Tx Pin Names	Tx Pin Number	Termination Resistor
TxIN0	51	R1
TxIN1	52	R2
TxIN2	54	R3
TxIN3	55	R4
TxIN4	56	R5
TxIN5	2	R6
TxIN6	3	R7
TxIN7	4	R8
TxIN8	6	R9
TxIN9	7	R10
TxIN10	8	R11
TxIN11	10	R12
TxIN12	11	R13
TxIN13	12	R14
TxIN14	14	R15
TxIN15	15	R16
TxIN16	16	R17
TxIN17	18	R18
TxIN18	19	R19
TxIN19	20	R20
TxIN20	22	R21
TxIN21	23	R22
TxIN22	24	R23
TxIN23	25	R24
TxIN24	27	R25
TxIN25	28	R26
TxIN26	30	R27
TxIN27	50	R28
TxCLKIN	31	R29

TX

50 Ohm Termination (Optional)

BOM (Bill of Materials) Transmitter PCB:

HSL Demo Board Schematic REV3
HSL8TXR3   Revision: 3   FPD-Link

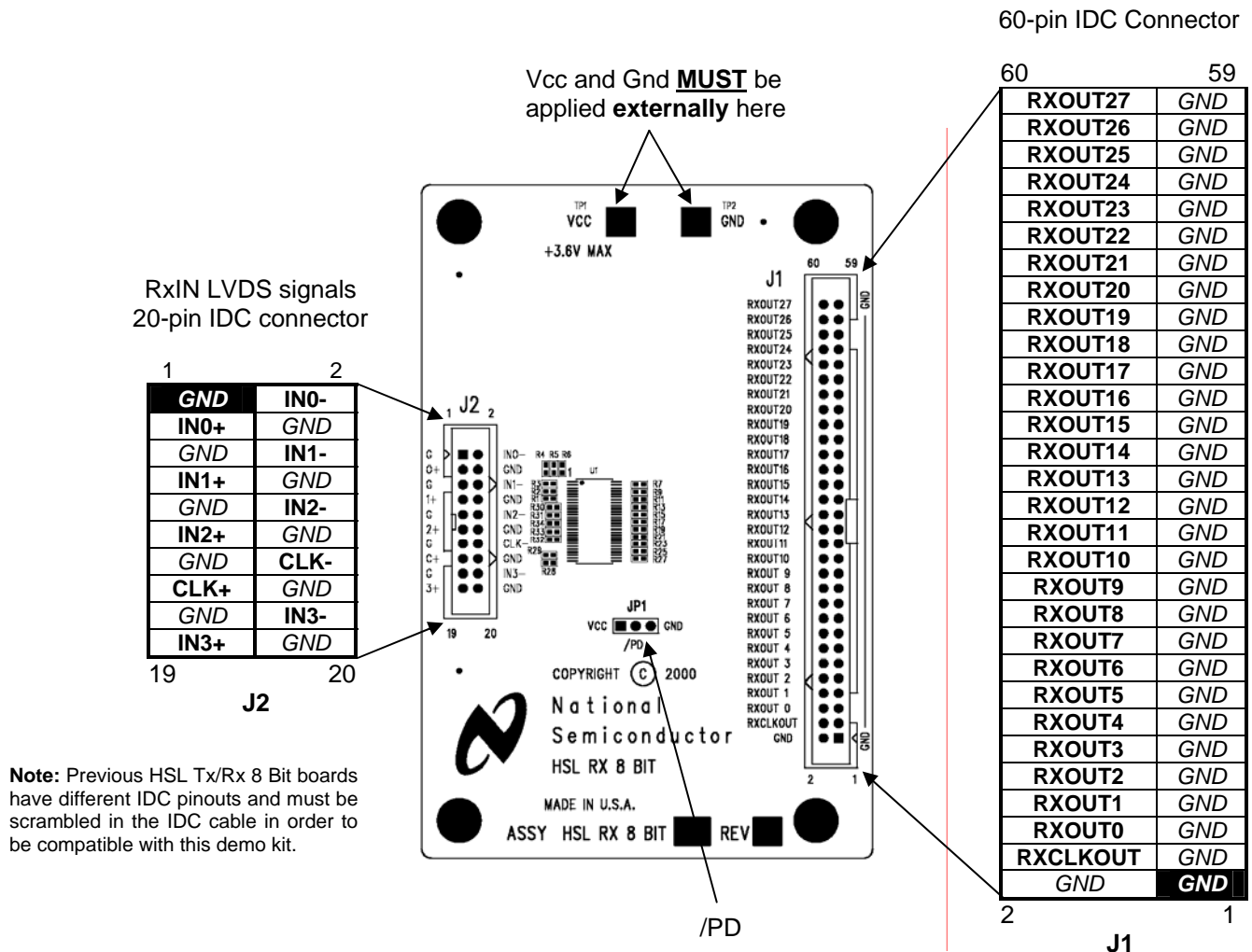| Item	Qty	Reference	Part	Pkg Size
1	1	C1	10 μF	CASE D
2	4	C2,C6,C10,C14	0.1 μF	1206 (3216)
3	4	C3,C7,C11,C15	22 μF	7343 (D)
4	3	C4,C8,C12	0.001 μF	0805 (2012)
5	3	C5,C9,C13	0.01 μF	0805 (2012)
6	2	JP2,JP1	3_PIN_HEADER	0.1" spacing
7	1	J1	IDC30X2	IDC60
8	1	J2	IDC10X2	IDC20
9	29	R1,R2,R3,R4,R5,R6,R7,R8, R9,R10,R11,R12,R13,R14, R15,R16,R17,R18,R19,R20, R21,R22,R23,R24,R25,R26, R27,R28,R29	Optional (See previous page)	0402
10	8	R30,R31,R32,R33,R34,R35, R36,R37	0 Ohm	0402
11	2	TP1,TP2	N/A	TP_.2"X.2"
12	1	U1	DS90C385AMTD	56-pin TSSOP

Rx FPD-Link Receiver Board:

J1 (60 position) provides access to the 28 bit LVTTL/LVCMOS and clock outputs.

The FPD-Link Receiver board is powered from the pads show below. For the receiver to be operational, the Power Down pin must be set HIGH with the jumper.

The 20-pin IDC connector (J2) provides the interface for LVDS signals for the Receiver board.

Note: Previous HSL Tx/Rx 8 Bit boards have different IDC pinouts and must be scrambled in the IDC cable in order to be compatible with this demo kit.

60-pin IDC Connector

Vcc and Gnd **MUST** be applied **externally** here

60	59
RXOUT27	*GND*
RXOUT26	*GND*
RXOUT25	*GND*
RXOUT24	*GND*
RXOUT23	*GND*
RXOUT22	*GND*
RXOUT21	*GND*
RXOUT20	*GND*
RXOUT19	*GND*
RXOUT18	*GND*
RXOUT17	*GND*
RXOUT16	*GND*
RXOUT15	*GND*
RXOUT14	*GND*
RXOUT13	*GND*
RXOUT12	*GND*
RXOUT11	*GND*
RXOUT10	*GND*
RXOUT9	*GND*
RXOUT8	*GND*
RXOUT7	*GND*
RXOUT6	*GND*
RXOUT5	*GND*
RXOUT4	*GND*
RXOUT3	*GND*
RXOUT2	*GND*
RXOUT1	*GND*
RXOUT0	*GND*
RXCLKOUT	*GND*
GND	**GND**
2	1

J1

RxIN LVDS signals
20-pin IDC connector

1	2
GND	**IN0-**
IN0+	*GND*
GND	**IN1-**
IN1+	*GND*
GND	**IN2-**
IN2+	*GND*
GND	**CLK-**
CLK+	*GND*
GND	**IN3-**
IN3+	*GND*
19	20

J2

Note: Previous HSL Tx/Rx 8 Bit boards have different IDC pinouts and must be scrambled in the IDC cable in order to be compatible with this demo kit.

/PD

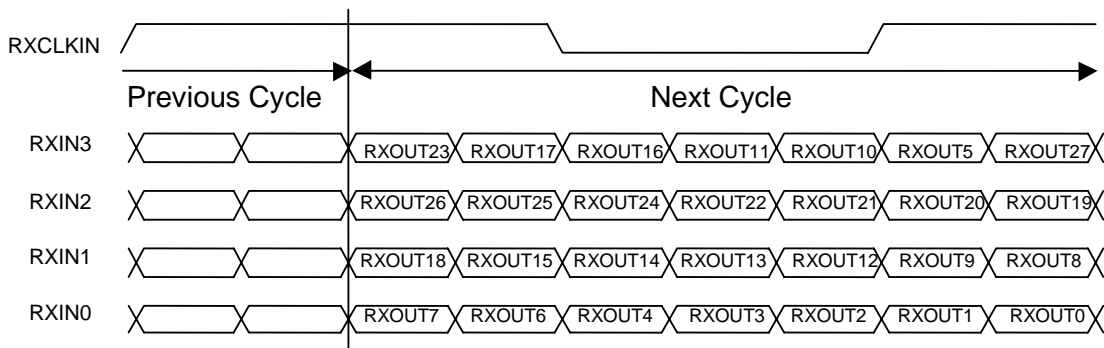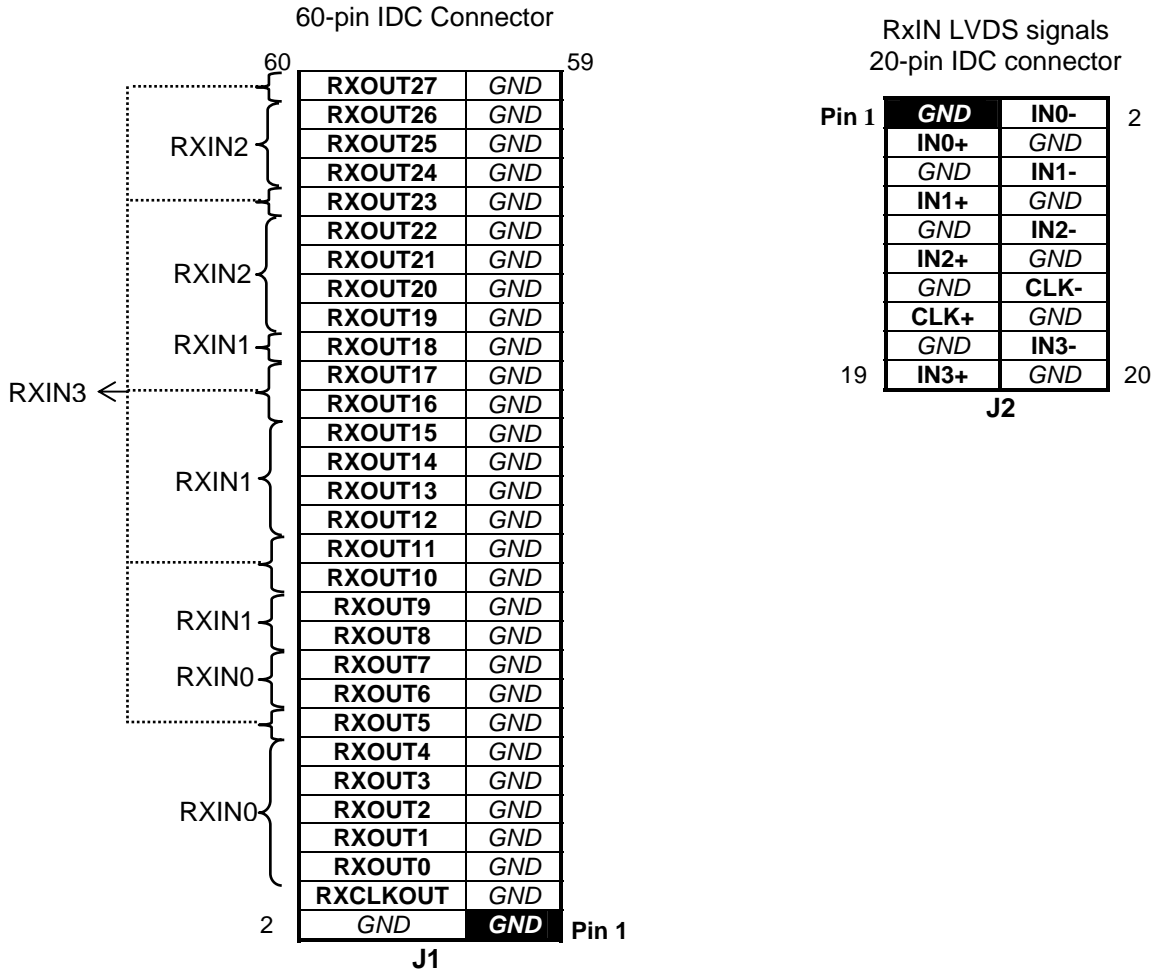# Selectable Jumper Settings for the Rx Board

Jumper	Purpose	Settings

/PD   **P**ower**D**own

(JP1)

$\boxed{\circ \quad \circ}\ \circ$ = ON $\circ\ \boxed{\circ \quad \circ}$ = OFF

Vcc   GND   Vcc   GND

(ON: Rx is operational;   OFF: Rx powers down)

Default setting is JP1 set HIGH (to Vcc), operational mode.

LVDS Mapping by IDC Connector

The following two figures illustrate how the Rx outputs are mapped to the IDC connector (J1) (Note – labels are also printed on the demo boards). The 20-pin IDC connector (J2) pinout is also shown.

(Receiver Board)

60-pin IDC Connector

60		59
RXIN2	RXOUT27	GND
	RXOUT26	GND
	RXOUT25	GND
	RXOUT24	GND
RXIN2	RXOUT23	GND
	RXOUT22	GND
	RXOUT21	GND
	RXOUT20	GND
RXIN1	RXOUT19	GND
	RXOUT18	GND
RXIN3	RXOUT17	GND
	RXOUT16	GND
	RXOUT15	GND
RXIN1	RXOUT14	GND
	RXOUT13	GND
	RXOUT12	GND
	RXOUT11	GND
	RXOUT10	GND
RXIN1	RXOUT9	GND
	RXOUT8	GND
RXIN0	RXOUT7	GND
	RXOUT6	GND
	RXOUT5	GND
	RXOUT4	GND
RXIN0	RXOUT3	GND
	RXOUT2	GND
	RXOUT1	GND
	RXOUT0	GND
	RXCLKOUT	GND
2	GND	GND	Pin 1

J1

RxIN LVDS signals
20-pin IDC connector

Pin 1	GND	IN0-	2
	IN0+	GND
	GND	IN1-
	IN1+	GND
	GND	IN2-
	IN2+	GND
	GND	CLK-
	CLK+	GND
	GND	IN3-
19	IN3+	GND	20

J2

RXCLKIN

Previous Cycle | Next Cycle

RXIN3: RXOUT23 RXOUT17 RXOUT16 RXOUT11 RXOUT10 RXOUT5 RXOUT27

RXIN2: RXOUT26 RXOUT25 RXOUT24 RXOUT22 RXOUT21 RXOUT20 RXOUT19

RXIN1: RXOUT18 RXOUT15 RXOUT14 RXOUT13 RXOUT12 RXOUT9 RXOUT8

RXIN0: RXOUT7 RXOUT6 RXOUT4 RXOUT3 RXOUT2 RXOUT1 RXOUT0

LVDS Data Inputs Mapped to LVTTL/LVCMOS Outputs

Rx Optional: Series Termination for RxOut

On the Rx demo board, there are 29 outputs that have an 0402 pad in series (which are shorted out). These pads are unpopulated from the factory but are provided if the user needs to install a 450 Ohm series resistors. This is required if directly connecting to 50 Ohm inputs on a scope. To use this option the user must cut the signal line between the pads before installing the 450 Ohm series resistors. R1 to R28 are associated with the DATA output lines. R29 is associated with CLKOUT. The total load presented to the receiver output is 500 Ohms (450 + 50). The waveform on the scope is 1/10 of the signal due to the resulting voltage divider (50 / (450 + 50)).

Optional Series Termination Resistor mapping is shown below:

Rx Pin Names	Rx Pin Number	Series Termination Resistor
RxOUT0	27	R28
RxOUT1	29	R27
RxOUT2	30	R26
RxOUT3	32	R25
RxOUT4	33	R24
RxOUT5	34	R23
RxOUT6	35	R22
RxOUT7	37	R21
RxOUT8	38	R20
RxOUT9	39	R19
RxOUT10	41	R18
RxOUT11	42	R17
RxOUT12	43	R16
RxOUT13	45	R15
RxOUT14	46	R14
RxOUT15	47	R13
RxOUT16	49	R12
RxOUT17	50	R11
RxOUT18	51	R10
RxOUT19	53	R9
RxOUT20	54	R8
RxOUT21	55	R7
RxOUT22	1	R6
RxOUT23	2	R5
RxOUT24	3	R4
RxOUT25	5	R3
RxOUT26	6	R2
RxOUT27	7	R1
RxCLKOUT	26	R29

RX — Series Termination (Optional)
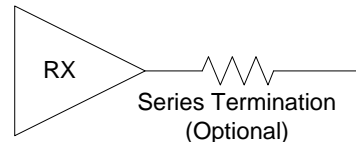
BOM (Bill of Materials) Receiver PCB:

HSL Demo Board Schematic REV3
HSL8RXR3   Revision: 3   FPD-Link

Item	Qty	Reference	Part	Pkg Size
1	1	C1	10 μF	CASE D
2	4	C2,C6,C10,C14	0.1 μF	1206 (3216)
3	4	C3,C7,C11,C15	22 μF	7343 (D)
4	3	C4,C8,C12	0.001 μF	0805 (2012)
5	3	C5,C9,C13	0.01 μF	0805 (2012)
6	1	JP1	3_PIN_HEADER	0.1" spacing
7	1	J1	IDC30X2	IDC60
8	1	J2	IDC10X2	IDC20
9	29	R1,R2,R3,R4,R5,R6,R7,R8, R9,R10,R11,R12,R13,R14, R15,R16,R17,R18,R19,R20, R21,R22,R23,R24,R25,R26, R27,R28,R29	Optional (See previous page)	0402
10	6	R35,R36,R37,R38,R39,R40	0 Ohm	0402
11	5	R30,R31,R32,R33,R34	100 Ohm	0402
12	2	TP1,TP2	N/A	TP_.2"X.2"
13	1	U1	DS90CF386MTD	56-pin TSSOP

Typical Connection / Test Equipment

The following is a list of typical test equipment that may be used to generate signals for the TX inputs:

1) Graphics card or GUI controller with digital RGB (LVTTL) output.
2) TEK HFS9009 - This pattern generator along with 9DG2 Cards may be used to generate input signals and also the clock signal.
3) TEK DG2020 - This generator may also be used to generate data and clock signals.
4) TEK MB100 BERT - This bit error rate tester may be used for both signal source and receiver.
5) Any other signal / pattern generator that generates the correct input levels as specified in the datasheet.

The following is a list of typically test equipment that may be used to monitor the output signals from the RX:

1) LCD Display Panel which supports digital RGB (LVTTL) inputs.
2) TEK MB100 BERT - Receiver.
3) Any SCOPE with 50 Ohm inputs or high impedance probes.

LVDS signals may be easily measured with high impedance / high bandwidth differential probes such as the TEK P6247 or P6248 differential probes.

The picture below shows a typical test set up using a Graphics Card and LCD Panel.
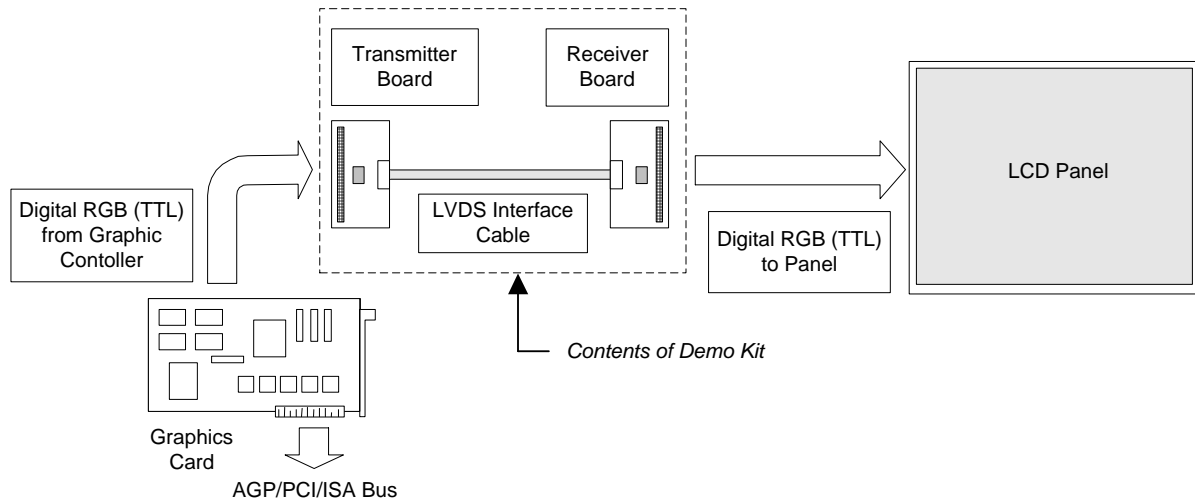
Typical FPD-Link Setup / PC Panel Application

The picture below shows a typical test set up using a generator and scope.
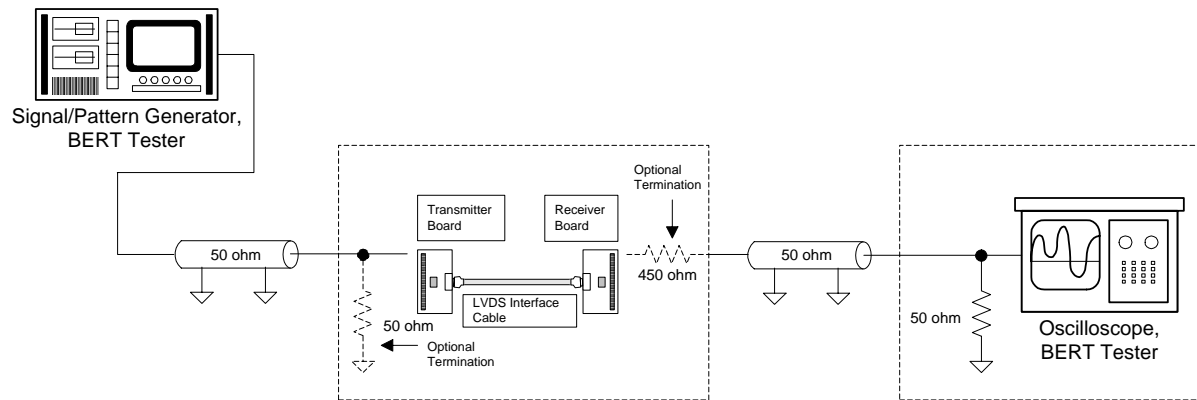
Typical Connection / Test Equipment Setup

Typical Waveshapes

LVDS
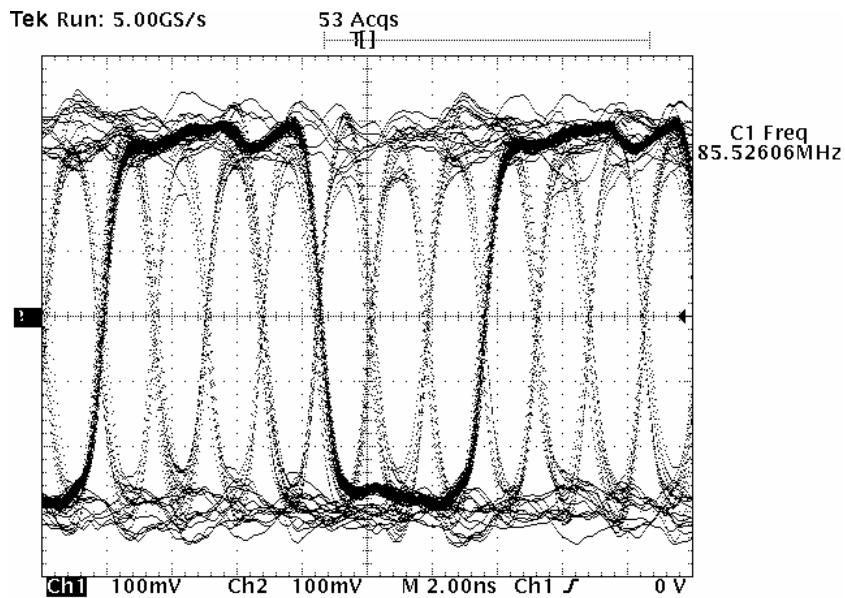
The plot above shows both the LVDS Data channel with PRBS data and also the LVDS Clock over laid. Note that the clock pattern is 4 bit times HIGH and 3 bit times LOW. The differential signal should be typically +/-300mV. These waveforms were acquired using the TEK P6248 Probes. Clock rate is 85MHz.

RxOUT
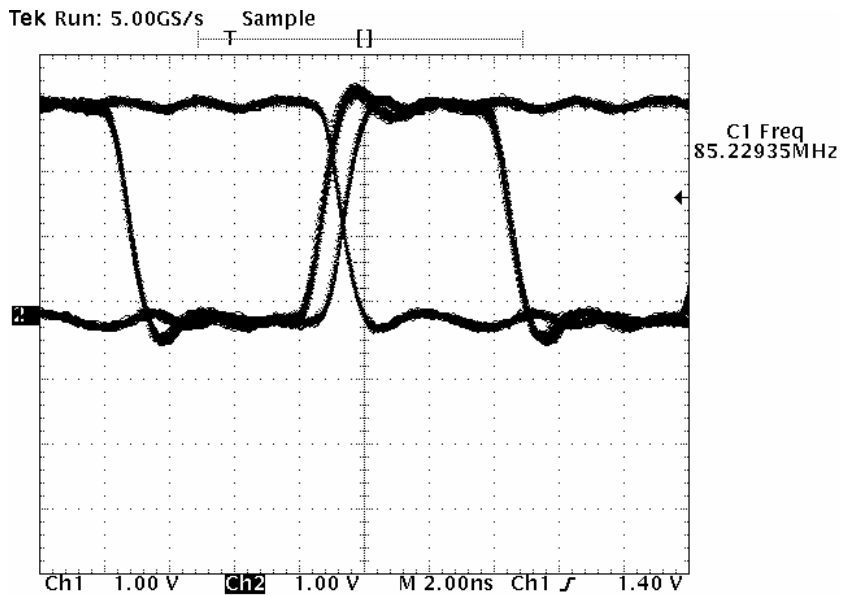
The plot above shows both the recovered PRBS data and also the regenerated Clock overlaid. Note that the clock transitions slightly before the data transition and strobes the data on the falling edge of the clock. The data and clock signals are low drive 3V CMOS outputs. The plot above is at 85MHz.

Troubleshooting

If the demo boards are not performing properly, use the following as a guide for quick solutions to potential problems.

QUICK CHECKS:
1. Check that Power and Ground are connected to both Tx AND Rx boards.
2. Check the supply voltage (typical 3.3V) and also current draw with both Tx and Rx boards (should be about 200mA with clock and one data bit at 66MHz).
3. Verify input clock and input data signals meet requirements (VIL, VIH, tset, thold), Also verify that data is strobed on the selected rising/falling (R_FB pin) edge of the clock.
4. Check that the Jumpers are set correctly.
5. Check that the cable is properly connected.

TROUBLESHOOTING CHART

Problem…	Solution…
There is only the output clock. There is no output data.	Make sure the data is applied to the correct input pin. Make sure data is valid at the input.
No output data and clock.	Make sure Power is on. Input data and clock are active and connected correctly. Make sure that the cable is secured to both demo boards.
Power, ground, input data and input clock are connected correctly, but no outputs.	Check the Power Down pins of both boards and make sure that the devices are enabled (/PD=Vcc) for operation.
The devices are pulling more than 1A of current.	Check for shorts in the cables connecting the TX and RX boards.
After powering up the demo boards, the power supply reads less than 3V when it is set to 3.3V.	Use a larger power supply that will provide enough current for the demo boards, a 500mA power supply is recommended.

Additional Information

For more information on FPD-Link Transmitters/Receivers, refer to the National's LVDS website at:

www.national.com/appinfo/fpd

Application Notes

- AN-1032 An Introduction to FPD-Link
- AN-1056 STN Application using FPD-Link
- AN-1059 High Speed Transmission with LVDS Devices
- AN-1084 Parallel Application of Link Chips
- AN-1085 FPD-Link PCB and Interconnect Design-In Guidelines
- AN-1127 LVDS Display Interface (LDI) TFT Data Mapping for Interoperability with FPD-Link
- AN-1163 TFT Data Mapping for Dual Pixel LDI Application - Alternate A - Color Map

Appendix

Tx PCB Schematic

Transmitter Board: HSL Demo Board Schematic
Document Number: HSL8TXR3
Rev: 3.0

Rx PCB Schematic

Receiver Board: HSL Demo Board Schematic
Document Number: HSL8RXR3
Rev: 3.0

J1 — IDC30X2

Pins 1–60 with signals: TXIN0, TXIN1, TXIN2, TXIN3, TXIN4, TXIN5, TXIN6, TXIN7, TXIN8, TXIN9, TXIN10, TXIN11, TXIN12, TXIN13, TXIN14, TXIN15, TXIN16, TXIN17, TXIN18, TXIN19, TXIN20, TXIN21, TXIN22, TXIN23, TXIN24, TXIN25, TXIN26, TXIN27, TXCLKIN

+3.6V MAX
VCC

U1 — DS90C385A

Pin	Signal		Signal	Pin
1	VCC	TXIN4	56
2	TXIN5	TXIN3	55
3	TXIN6	TXIN2	54
4	TXIN7	GND	53
5	GND	TXIN1	52
6	TXIN8	TXIN0	51
7	TXIN9	TXIN27	50
8	TXIN10	LVDS GND	49
9	VCC	TXOUT0-	48
10	TXIN11	TXOUT0+	47
11	TXIN12	TXOUT1-	46
12	TXIN13	TXOUT1+	45
13	GND	LVDS VCC	44
14	TXIN14	LVDS GND	43
15	TXIN15	TXOUT2-	42
16	TXIN16	TXOUT2+	41
17	R_FB	TXCLK OUT-	40
18	TXIN17	TXCLK OUT+	39
19	TXIN18	TXOUT3-	38
20	TXIN19	TXOUT3+	37
21	GND	LVDS GND	36
22	TXIN20	PLL GND	35
23	TXIN21	PLL VCC	34
24	TXIN22	PLL GND	33
25	TXIN23	/PWR DWN	32
26	VCC	TXCLK IN	31
27	TXIN24	TXIN26	30
28	TXIN25	GND	29

Resistors R1–R29 on TXIN0–TXIN27 and TXCLKIN

J2 — IDC10X2

Pin	Signal		Signal	Pin
1	LVDS_GND	TXOUT0-	2
3	TXOUT0+		4
5		TXOUT1-	6
7	TXOUT1+		8
9		TXOUT2-	10
11	TXOUT2+		12
13		TXCLKOUT-	14
15	TXCLKOUT+		16
17		TXOUT3-	18
19	TXOUT3+		20

TXOUT0-, TXOUT0+, TXOUT1-, TXOUT1+, LVDS_VCC, LVDS_GND, TXOUT2-, TXOUT2+, TXCLKOUT-, TXCLKOUT+, TXOUT3-, TXOUT3+, PLL_GND, PLL_VCC

VCC
R32 VCC
R33 LVDS_VCC
R34 PLL_VCC
VCC1

GND1
R35 PLL_GND
R36 LVDS_GND
R37 GND

VCC
JP1
R_FB   R31
3_PIN_HEADER

VCC
JP2
/PD
3_PIN_HEADER

VCC
C3 C4 C5 C6 C7
GND 22uF 0.001uF 0.01uF 0.1uF 22uF

LVDS_VCC
C8 C9 C10 C11
LVDS_GND 0.001uF 0.01uF 0.1uF 22uF

PLL_VCC
C12 C13 C14 C15
PLL_GND 0.001uF 0.01uF 0.1uF 22uF

TP1
TP_.2"X.2"
TP2
TP_.2"X.2"

+3.6V MAX
VCC1
C1 10uF   C2 0.1uF
GND1

National *Semiconductor*

Title: HSL DEMO BOARD SCHEMATIC

Size | Document Number: HSL8TXR3 | Rev: 3

Date: Friday, March 5, 2004 | Sheet 1 of 1

+3.6V MAX
VCC

J2

LVDS_GND	1	2	RXIN0-
RXIN0+	3	4	RXIN1-
RXIN1+	5	6	
	7	8	RXIN2-
RXIN2+	9	10	
	11	12	RXCLKIN-
RXCLKIN+	13	14	
	15	16	RXIN3-
RXIN3+	17	18	
	19	20	

IDC10X2

U1

1	RXOUT22	VCC	56
2	RXOUT23	RXOUT21	55
3	RXOUT24	RXOUT20	54
4	GND	RXOUT19	53
5	RXOUT25	GND	52
6	RXOUT26	RXOUT18	51
7	RXOUT27	RXOUT17	50
8	LVDS GND	RXOUT16	49
9	RXIN0-	VCC	48
10	RXIN0+	RXOUT15	47
11	RXIN1-	RXOUT14	46
12	RXIN1+	RXOUT13	45
13	LVDS VCC	GND	44
14	LVDS GND	RXOUT12	43
15	RXIN2-	RXOUT11	42
16	RXIN2+	RXOUT10	41
17	RXCLK IN-	VCC	40
18	RXCLK IN+	RXOUT9	39
19	RXIN3-	RXOUT8	38
20	RXIN3+	RXOUT7	37
21	LVDS GND	GND	36
22	PLL GND	RXOUT6	35
23	PLL VCC	RXOUT5	34
24	PLL GND	RXOUT4	33
25	/PWR DWN	RXOUT3	32
26	RXCLK OUT	VCC	31
27	RXOUT0	RXOUT2	30
28	GND	RXOUT1	29

DS90CF386

R1 RXOUT27
R2 RXOUT26
R3 RXOUT25
R4 RXOUT24
R5 RXOUT23
R6 RXOUT22
R7 RXOUT21
R8 RXOUT20
R9 RXOUT19
R10 RXOUT18
R11 RXOUT17
R12 RXOUT16
R13 RXOUT15
R14 RXOUT14
R15 RXOUT13
R16 RXOUT12
R17 RXOUT11
R18 RXOUT10
R19 RXOUT9
R20 RXOUT8
R21 RXOUT7
R22 RXOUT6
R23 RXOUT5
R24 RXOUT4
R25 RXOUT3
R26 RXOUT2
R27 RXOUT1
R28 RXOUT0
R29 RXCLKOUT

RXIN0-
RXIN0+ R30 100
RXIN1- R31 100
RXIN1+
LVDS_VCC
LVDS_GND
RXIN2-
RXIN2+ R34 100
RXCLKIN-
RXCLKIN+ R33 100
RXIN3- R32 100
RXIN3+
PLL_VCC
PLL_GND

VCC
JP1
/PD
3_PIN_HEADER

J1

RXOUT27			
RXOUT26	60	59	
RXOUT25	58	57	
RXOUT24	56	55	
RXOUT23	54	53	
RXOUT22	52	51	
RXOUT21	50	49	
RXOUT20	48	47	
RXOUT19	46	45	
RXOUT18	44	43	
RXOUT17	42	41	
RXOUT16	40	39	
RXOUT15	38	37	
RXOUT14	36	35	
RXOUT13	34	33	
RXOUT12	32	31	
RXOUT11	30	29	
RXOUT10	28	27	
RXOUT9	26	25	
RXOUT8	24	23	
RXOUT7	22	21	
RXOUT6	20	19	
RXOUT5	18	17	
RXOUT4	16	15	
RXOUT3	14	13	
RXOUT2	12	11	
RXOUT1	10	9	
RXOUT0	8	7	
RXCLKOUT	6	5	
	4	3	
	2	1	

IDC30X2

VCC1 R35 VCC
R36 LVDS_VCC
R37 PLL_VCC
VCC

GND1 R38 PLL_GND
R39 LVDS_GND
R40 GND

VCC
| C3 | C4 | C5 | C6 | C7 |
GND 22uF 0.001uF 0.01uF 0.1uF 22uF

LVDS_VCC
| C8 | C9 | C10 | C11 |
LVDS_GND 0.001uF 0.01uF 0.1uF 22uF

PLL_VCC
| C12 | C13 | C14 | C15 |
PLL_GND 0.001uF 0.01uF 0.1uF 22uF

TP1
TP_.2"X.2"
TP2
TP_.2"X.2"

+3.6V MAX
VCC1
+ C1 10uF
+ C2 0.1uF
GND1

National *Semiconductor*

Title
HSL DEMO BOARD SCHEMATIC

Size
Document Number
HSL8RXR3
Rev 3

Date: Friday, October 27, 2000   Sheet 1 of 1

IMPORTANT NOTICE