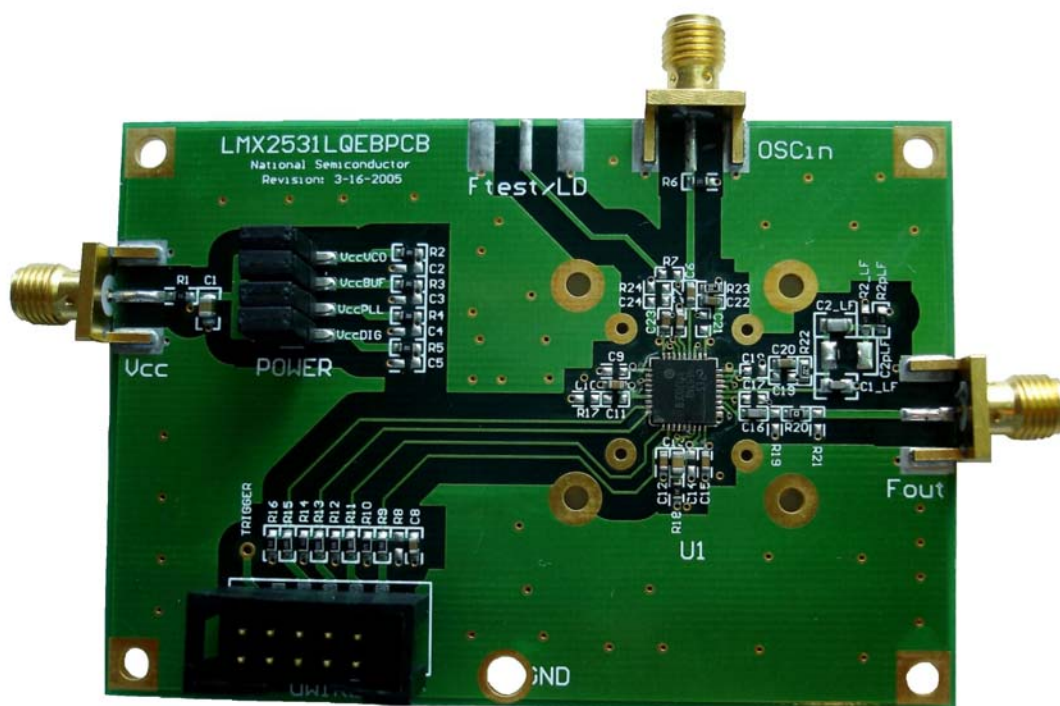




LMX2531LQ2265E

Evaluation Board Operating Instructions



National Semiconductor Corporation
Wireless Communications, RF Products Group

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MS A2-600
Santa Clara, CA, 95052-8090

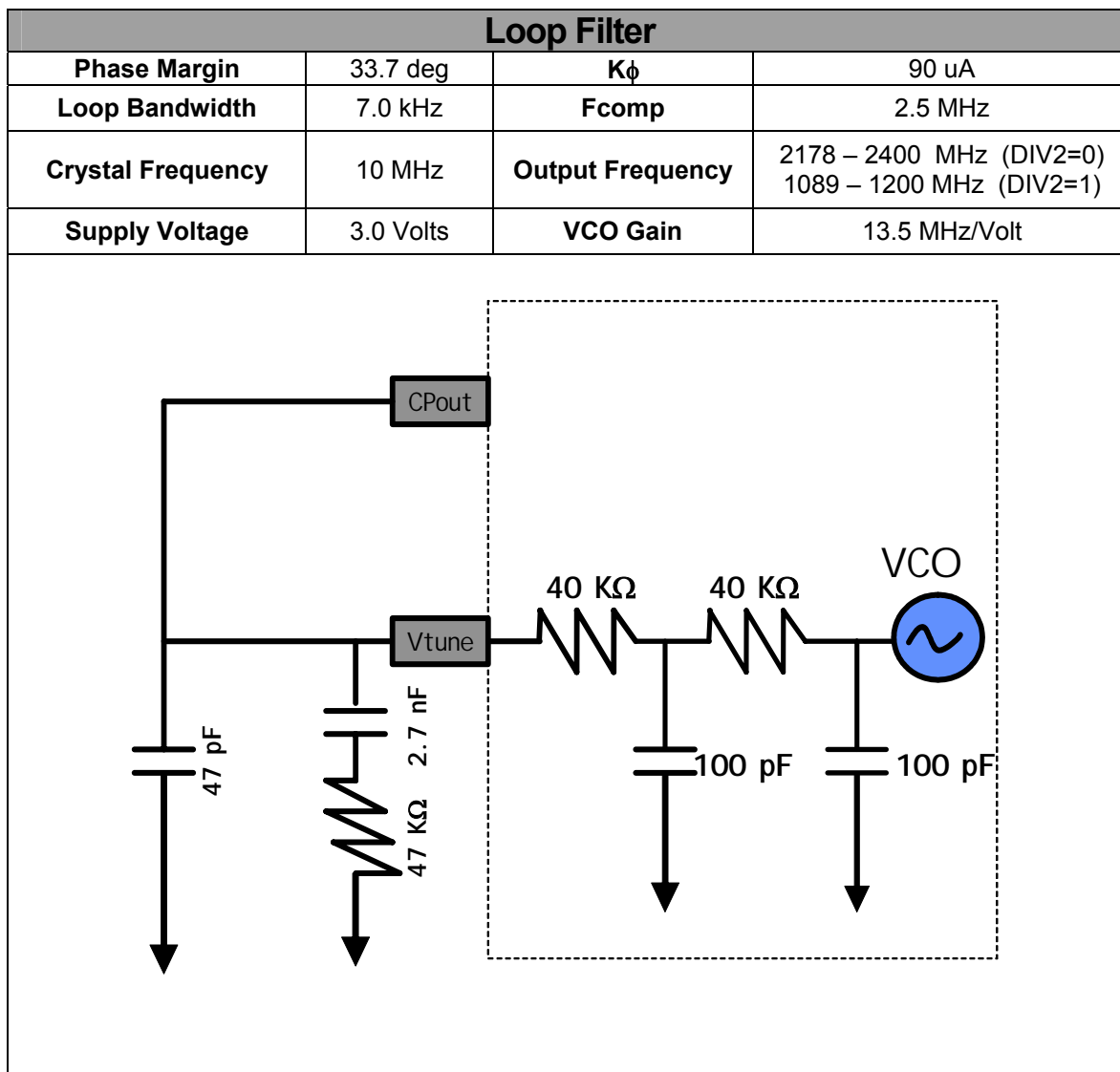
LMX2531LQ2265EFPEB Rev 1.19.2006

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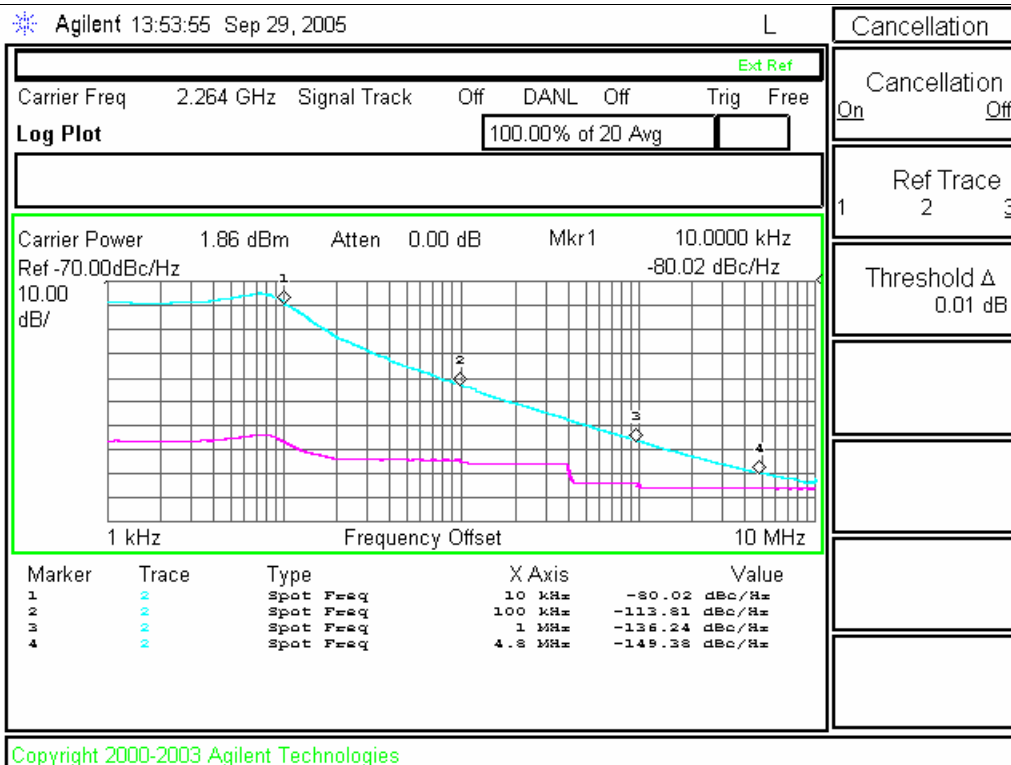
General Description

The LMX2531LQ2265E Evaluation Board simplifies evaluation of the LMX2531LQ2265E PLL/VCO synthesizer system. The board enables all performance measurements with no additional support circuitry. The evaluation board consists of a LMX2531LQ2265E device, and a cable assembly. The cable assembly is bundled with the evaluation board for connecting to a PC through the parallel printer port. By means of **MICROWIRE™** serial port emulation, the *CodeLoader* software included can be run on a PC to facilitate the LMX2531LQ2265E internal register programming for the evaluation and measurement. In addition to this cable assembly, there is a microwire buffer board that ensures that the proper voltage levels are provided to the microwire inputs and also this reduces digital noise from computers through the parallel port.

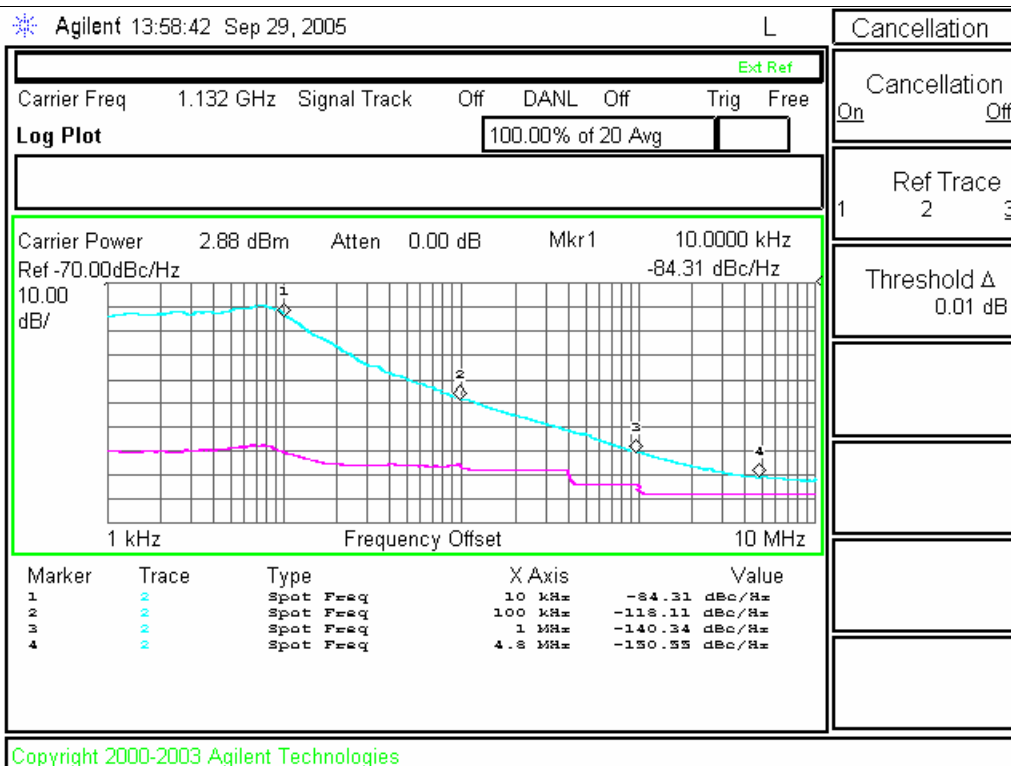


Phase Noise

Output Frequency = 2264 MHz
Internal Divide by 2 Disabled (DIV2=0)



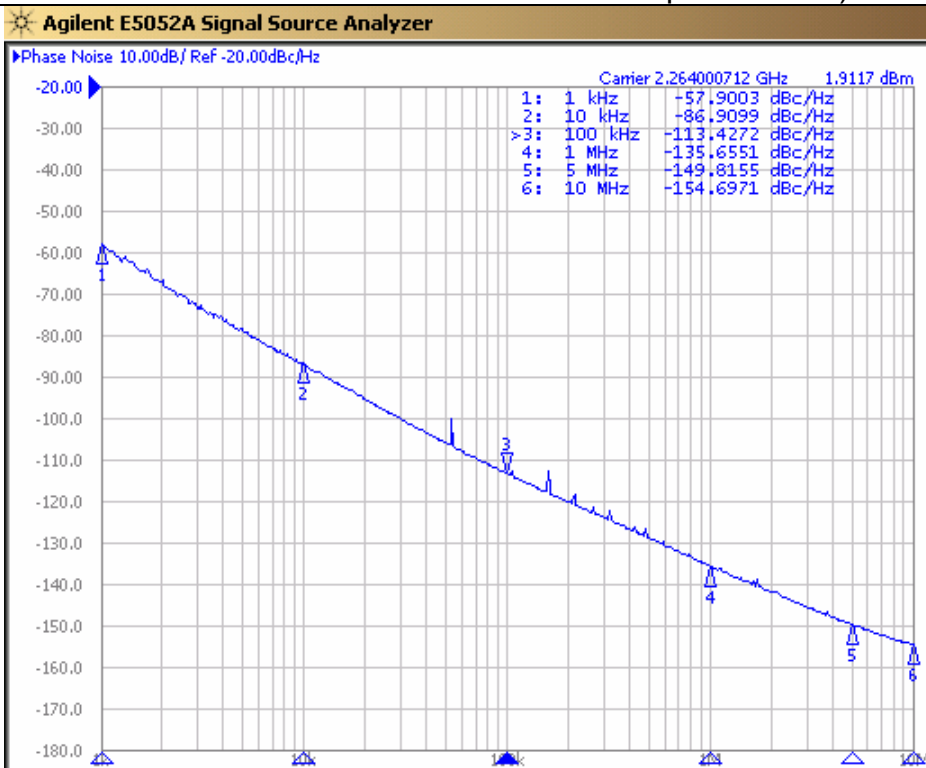
Output Frequency = 1132 MHz
Internal Divide by 2 Enabled (DIV2=1)



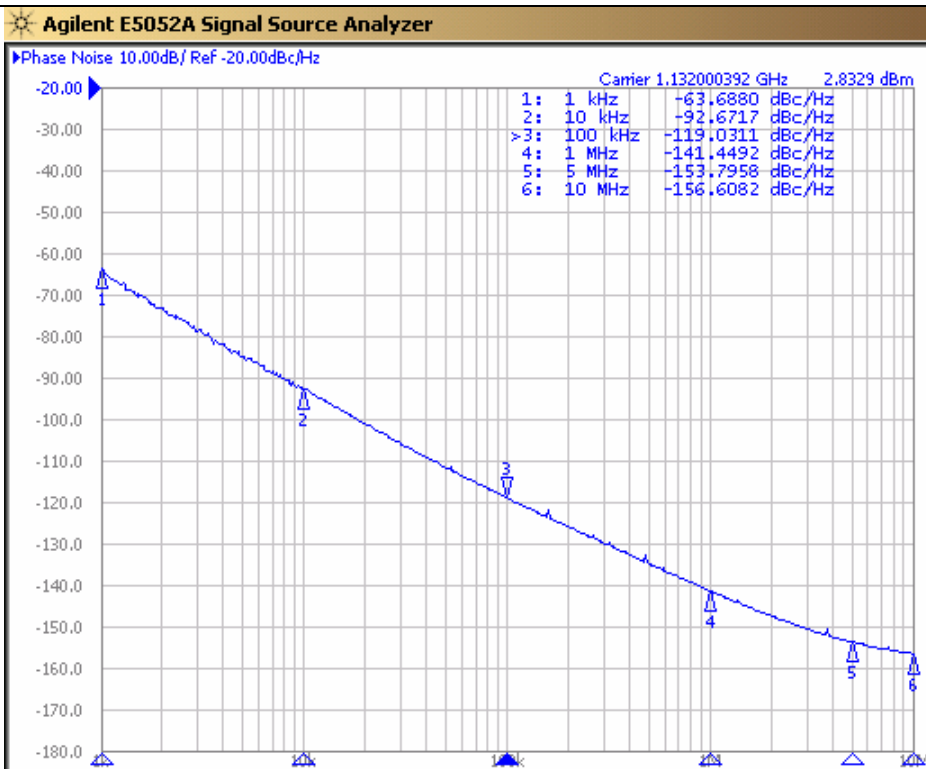
Phase Noise with Narrow Loop Filter

(This is the most accurate measurement of the VCO phase noise)

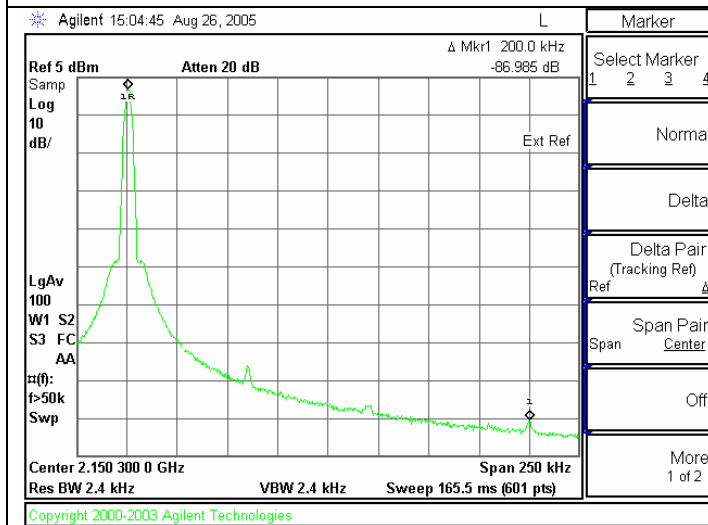
Output Frequency = 2264 MHz
Internal Divide by 2 Disabled (DIV2=0)



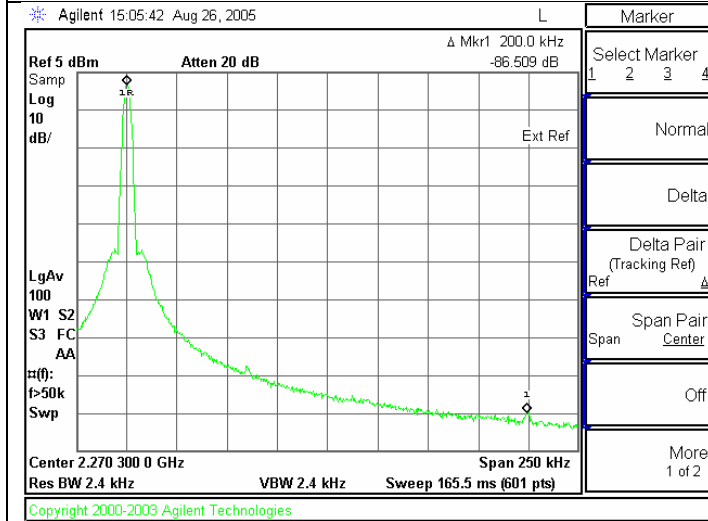
Output Frequency = 1132 MHz
Internal Divide by 2 Enabled (DIV2=1)



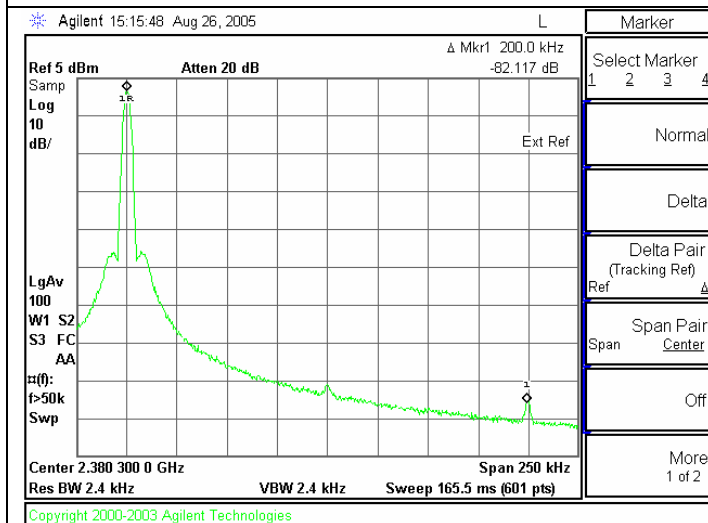
Spurs (Internal Divide by 2 Disabled)



Spur at 200 kHz offset at a worst case frequency of 2150.2 MHz is -86.9 dBc. Worst case channels occur at exactly one channel spacing above or below a multiple of the crystal frequency (10 MHz).

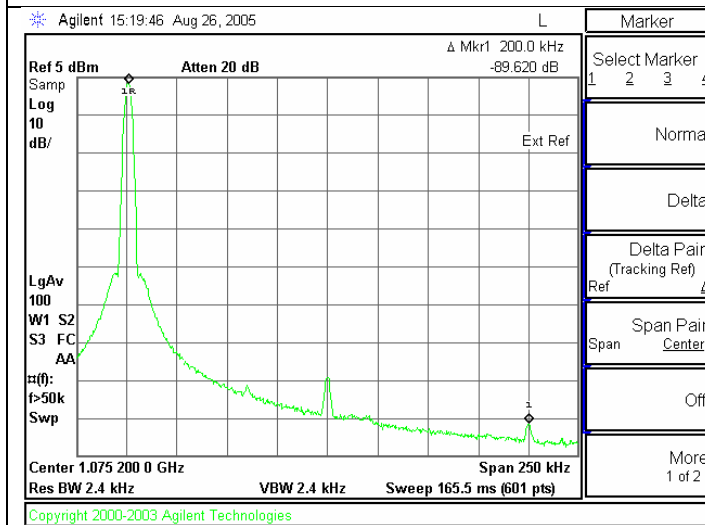


Spur at 200 kHz offset at a worst case frequency of 2270.2 MHz is -86.5 dBc.

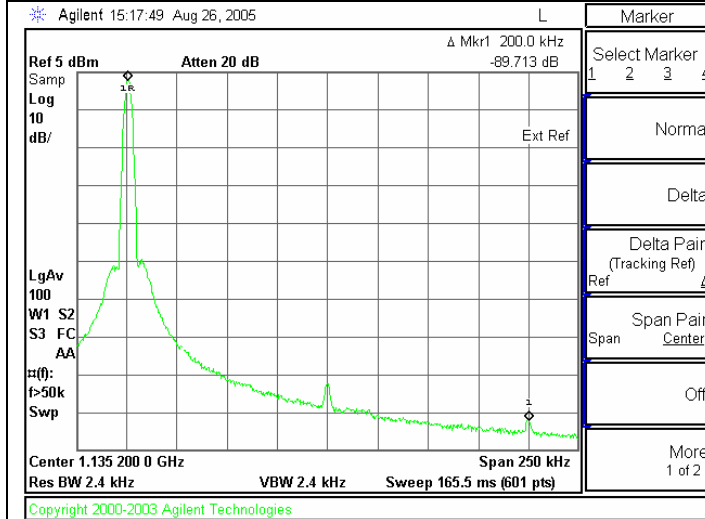


Spur at 200 kHz offset at a worst case frequency of 2380.2 MHz is -82.1 dBc.

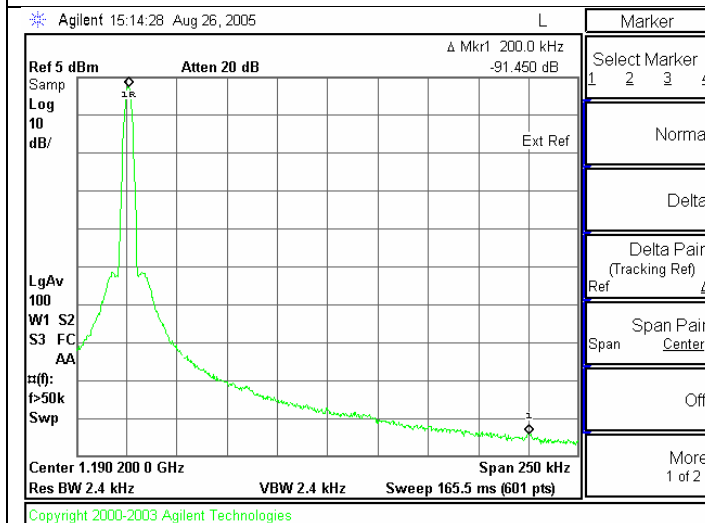
Spurs (Internal Divide by 2 Enabled)



Spur at 200 kHz offset at a frequency of 1075.1 MHz is -89.6 dBc. Since this mode uses the divide by 2 mode, the channel spacing here is actually 100 kHz. The spur at 100 kHz could be eliminated by doubling the channel spacing before the divider. The reason that the spur at 200 kHz is shown is to illustrate theoretical 6 dB impact of the divider.

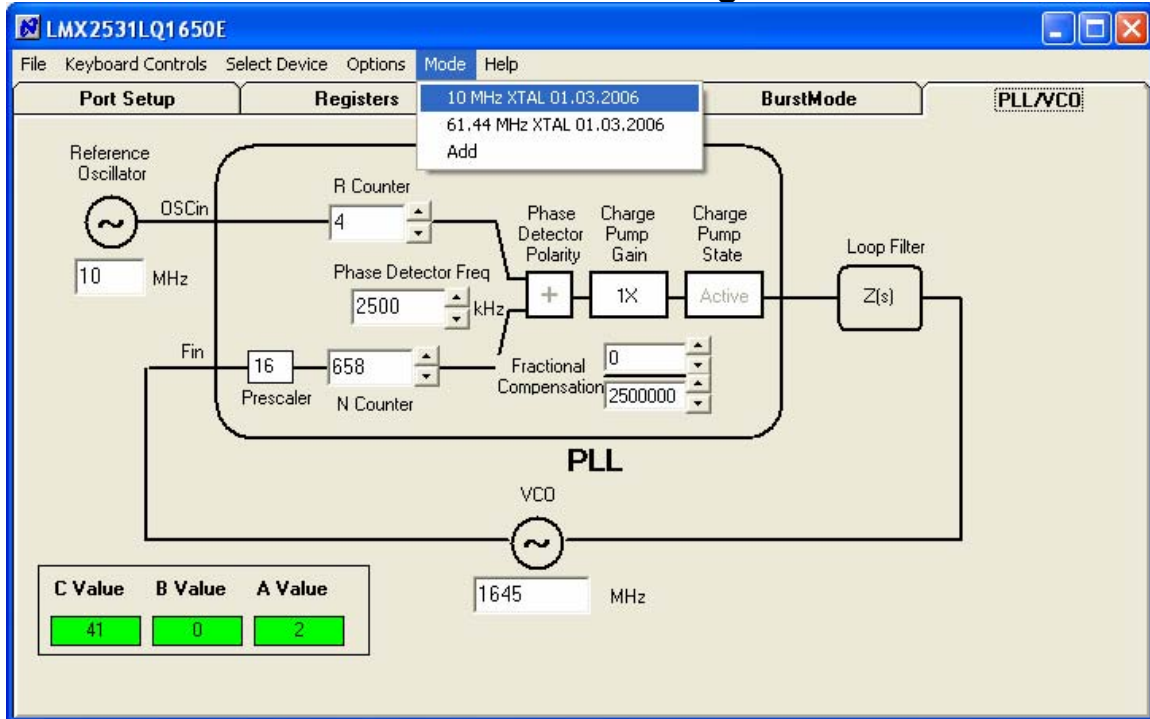


Spur at 200 kHz offset for a frequency of 1135.1 MHz is -89.7 dBc.



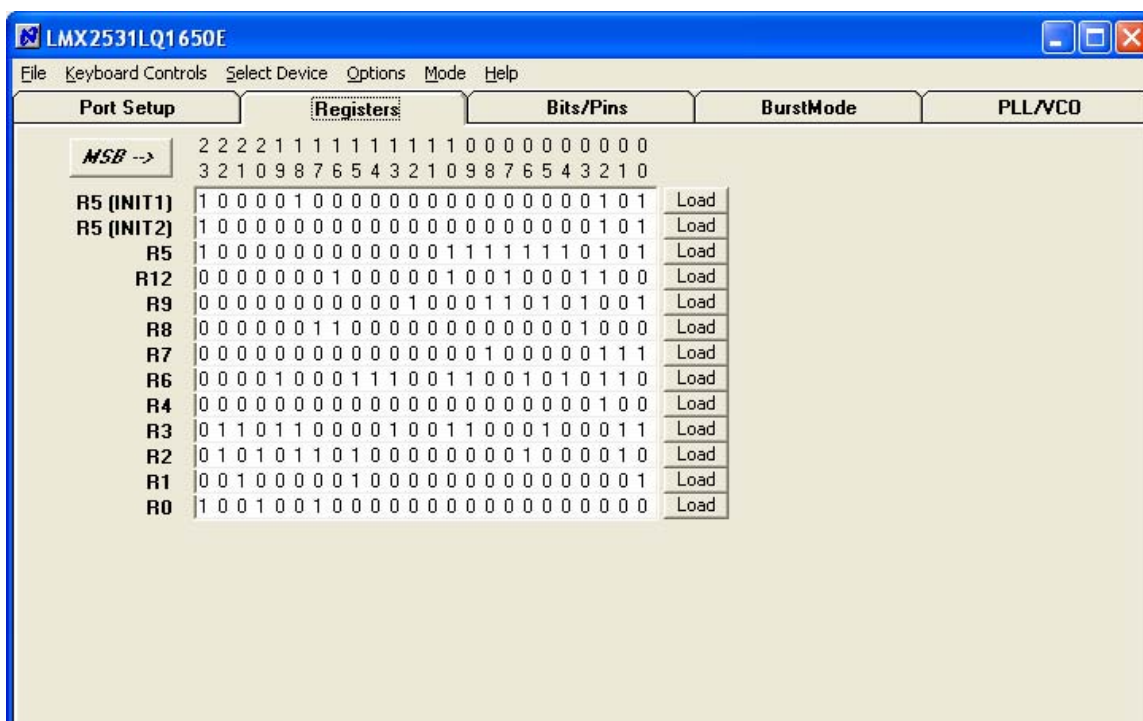
Spur at 200 kHz offset for a frequency of 1190.1 MHz is -91.4 dBc.

CodeLoader Settings

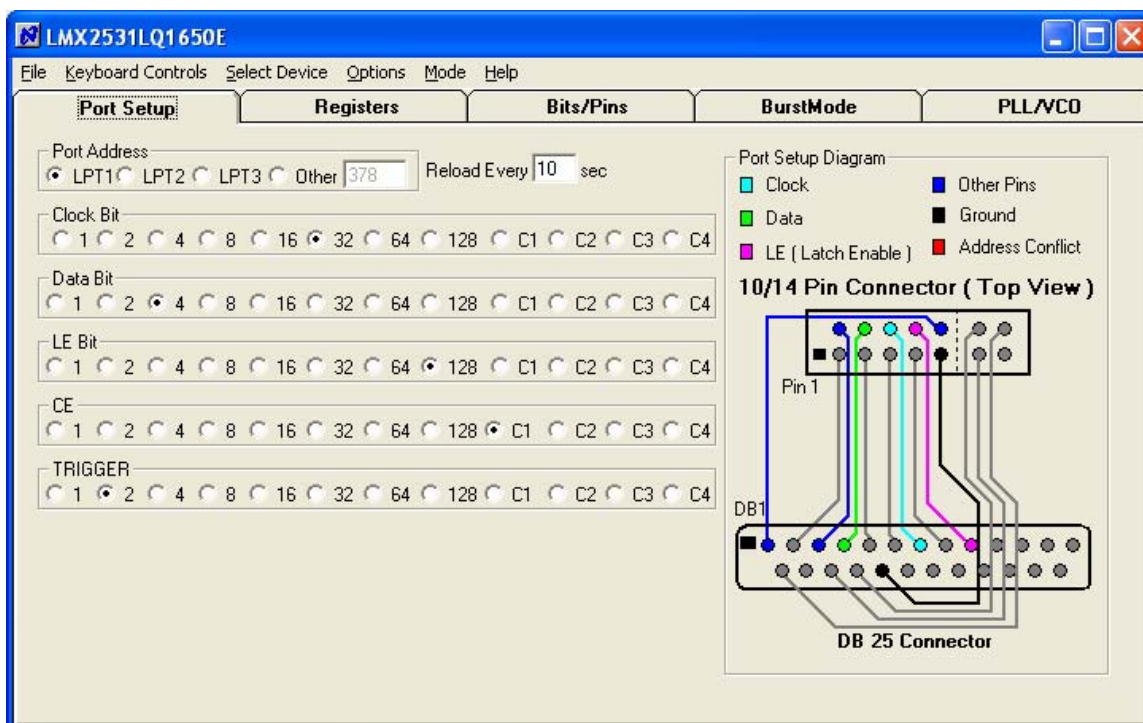


For the CodeLoader program, the default reference oscillator used for these instructions was 10 MHz, but there is a mode for a 61.44 MHz oscillator as well. If the bits become scrambled, their original state may be recalled by choosing the appropriate mode. Note that if the internal divide by 2 is enabled, the VCO frequency still reflects the VCO frequency before the divide by 2.

The screenshot shows the LMX2531LQ1650E CodeLoader Settings window with the 'Bits/Pins' tab selected. The 'INITIALIZATION' section has 'REG_RST' unchecked. The 'VCO OUTPUT' section has 'DIV2' unchecked. The 'POWER CONTROLS' section has 'EN_PLL', 'EN_PLLLD01', 'EN_PLLLD02', 'EN_DIGLDO', 'EN_VCO', 'EN_VCOLDO', and 'EN_OSC' all checked. The 'VCO PN OPTIMIZATION' section has 'VCO_ACISEL' set to 8. The 'VCO FREQUENCY CAL' section has 'XTLDIV' set to 'Divide by 2', 'XTLSEL' set to '<20 MHz', and 'XTLMAN' set to 0. The 'INTERNAL LOOP FILTER' section has 'EN_LPFILTER' checked, 'C3_4_ADJ' set to 'C3=100pF, C4=100pF', 'R3_ADJ' set to '40 Kohm', and 'R4_ADJ' set to '40 Kohm'. The 'FASTLOCK CONTROLS' section has 'TOC' set to 0, 'ICPFL' set to '1X', 'R3_ADJ_FL' set to '0 Ohm', and 'R4_ADJ_FL' set to '0 Ohm'. The 'LOCK DETECT' section has 'LDDIV4' set to 'Disabled'. The 'Program Pins' section has 'CE' checked and 'TRIGGER' unchecked.

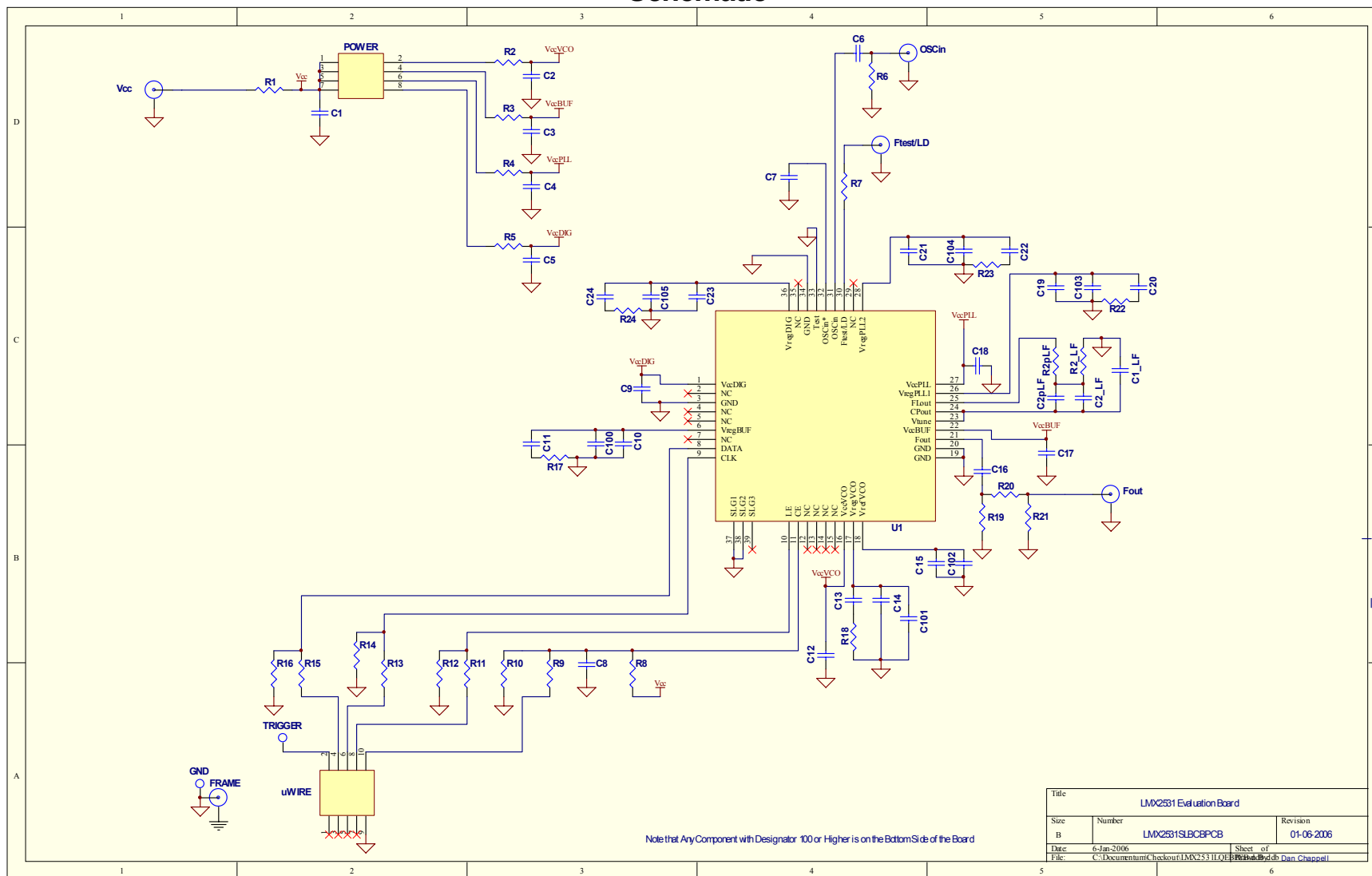


CodeLoader is set up to load the registers and initialize the part in the correct way. R5 (INIT1) and R5 (INIT 2) are just the R5 register being used to properly initialize the part. So a single CNT+L should load the part.



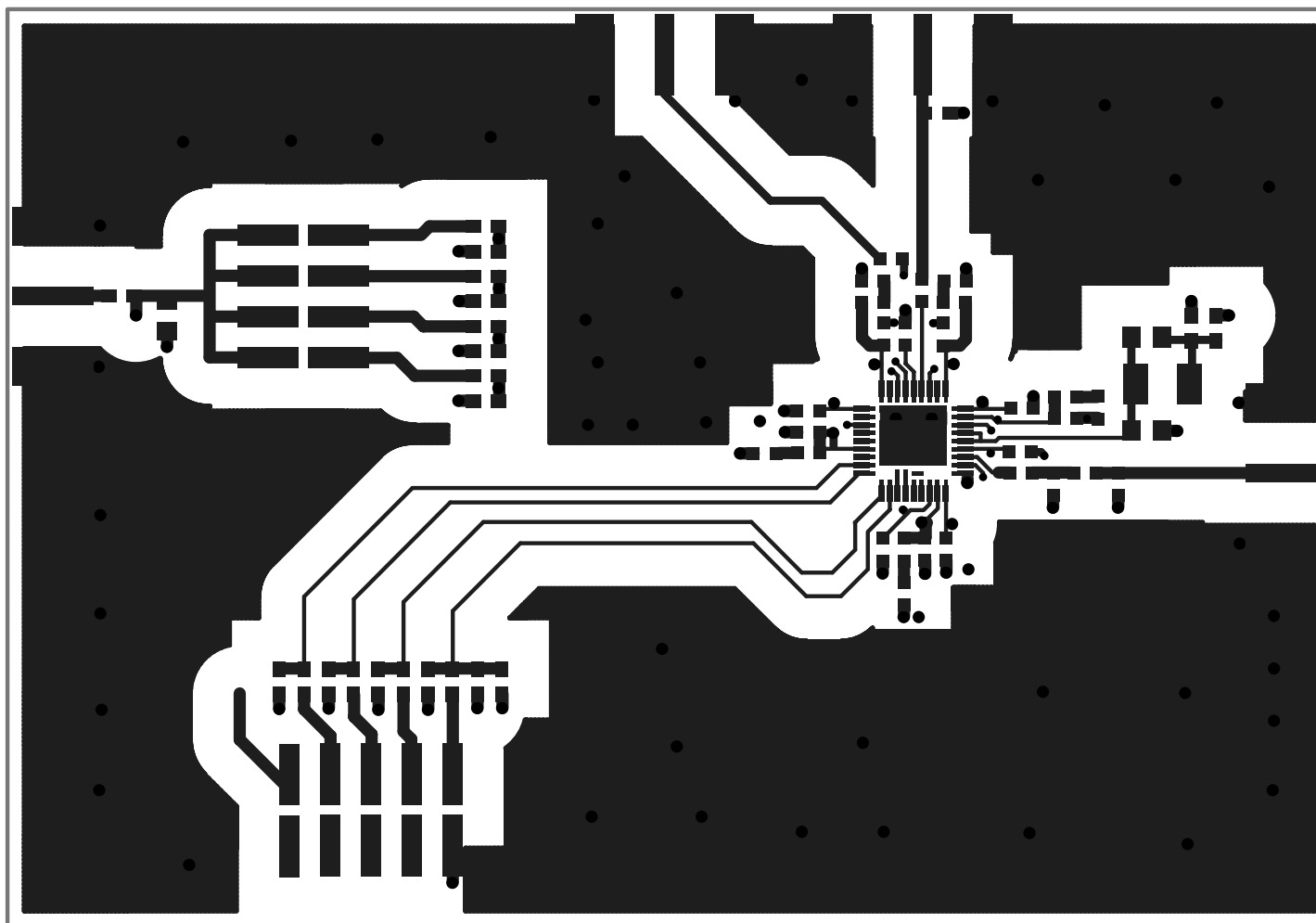
The port setup tells CodeLoader what information goes where. If this is wrong, the part will not program. Although LPT1 is usually correct, CodeLoader does not autodetect the correct port. On some laptops, it may be LPT3.

Schematic

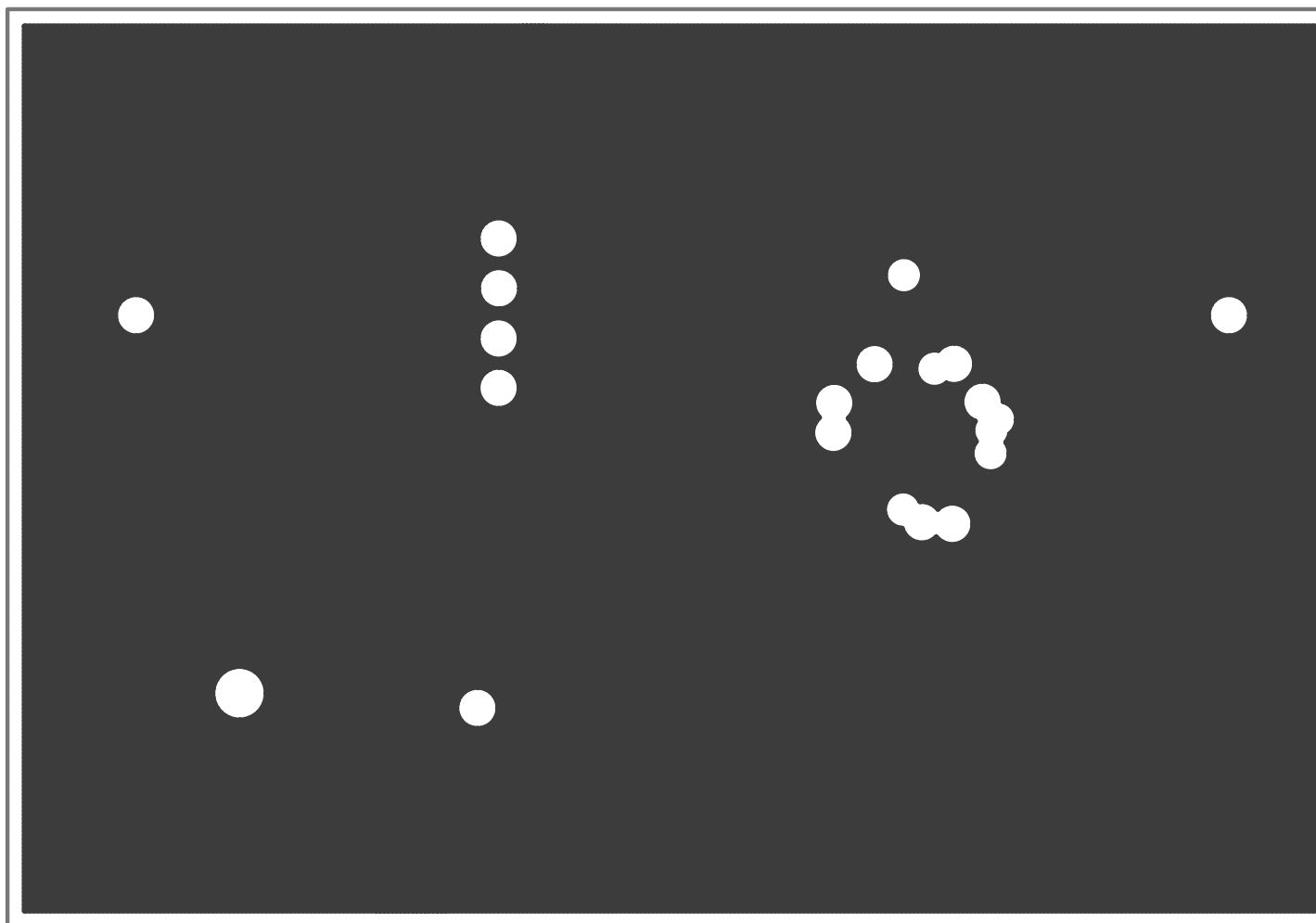


Bill of Materials				LMX2531EB					Revision 1/3/2006
Item	QTY	Manufacturer	Part #	Size	Tol	Voltage	Material	Value	Designators
0	19	n/a						Open Capacitors	C2pLF, C2, C3, C4, C5, C9, C11, C14, C17, C18, C19, C21, C24, C100, C101, C102, C103, C104, C105
	6							Open Resistors	R7, R8, R17, R19, R21, R24
	1							Open Miscellaneous	Ftest/LD
1	1	Kemet	C0603C470J5GAC	603	5%	50V	C0G	47pF	C1_LF
2	1	Kemet	C0603C101J5GAC	603	5%	50V	C0G	100pF	C16
3	1	Kemet	C0805C272J3GAC	805	5%	25V	C0G	2.7nF	C2_LF
4	2	Kemet	C0603C103J5RAC	603	5%	50V	X7R	10nF	C10, C23
5	4	Kemet	C0603C104J3RAC	603	5%	25V	X7R	100nF	C6, C7, C12, C15
6	2	Kemet	C0603C474K4RAC	603	10%	16V	X7R	470nF	C20, C22
7	1	Kemet	C0603C105K4RAC	603	10%	16V	X5R	1uF	C8
8	1	Kemet	C0603C475K9PAC	603	10%	6.3V	X5R	4.7uF	C13
9	1	Kemet	C0805C106K8PAC	805	10%	10V	X5R	10uF	C1
10	1	Vishay	CRCW0603000ZRT1	603	5%	0.1W	Thick Film	0Ω	R20
11	2	Panasonic	P.22AHCT-ND	603	10%	0.1W	Thick Film	0.22Ω	R22, R23
12	2	Vishay	CRCW06033R3JRT1	603	5%	0.1W	Thick Film	3.3Ω	R1, R18
13	4	Vishay	CRCW0603100JRT1	603	5%	0.1W	Thick Film	10Ω	R2, R3, R4, R5
14	1	Vishay	CRCW0603510JRT1	603	5%	0.1W	Thick Film	51Ω	R6
15	4	Vishay	CRCW0603103JRT1	603	5%	0.1W	Thick Film	10KΩ	R9, R11, R13, R15
16	5	Vishay	CRCW0603123JRT1	603	5%	0.1W	Thick Film	12KΩ	R2pLF, R10, R12, R14, R16
17	1	Vishay	CRCW0603473JRT1	603	5%	0.1W	Thick Film	47KΩ	R2_LF
18	1	Comm Con Connectors	HTSM3203-8G2	2X4	n/a	n/a	Metal/Plastic	Header	POWER
19	1	FCI Electronics	52601-S10-8	2X5	n/a	n/a	Metal/Plastic	Header	uWire
20	3	Johnson Components	142-0701-851	SMA	n/a	n/a	Metal	SMA	Fout, OSCin, Vcc
21	1	National Semiconductor	LMX2531LQEBPCB	n/a	n/a	n/a	FR4 62 mil Thick	PCB Board 1st Layer 10 mils	n/a
22	1	National Semiconductor	LMX2531	LLP36	n/a	2.7	Silicon	LMX2531	U1
23	4	Com Con Connectors	CCIJ255G	2-Pin	n/a	n/a	Metal/Plastic	Shunt	Place Across: POWER: 1-2, 3-4, 5-6, 7-8
24	4	SPC Technology	SPCS-8	0.156"	n/a	n/a	Nylon	Nylon Standoffs	Place in 4 Holes in Corners of Board

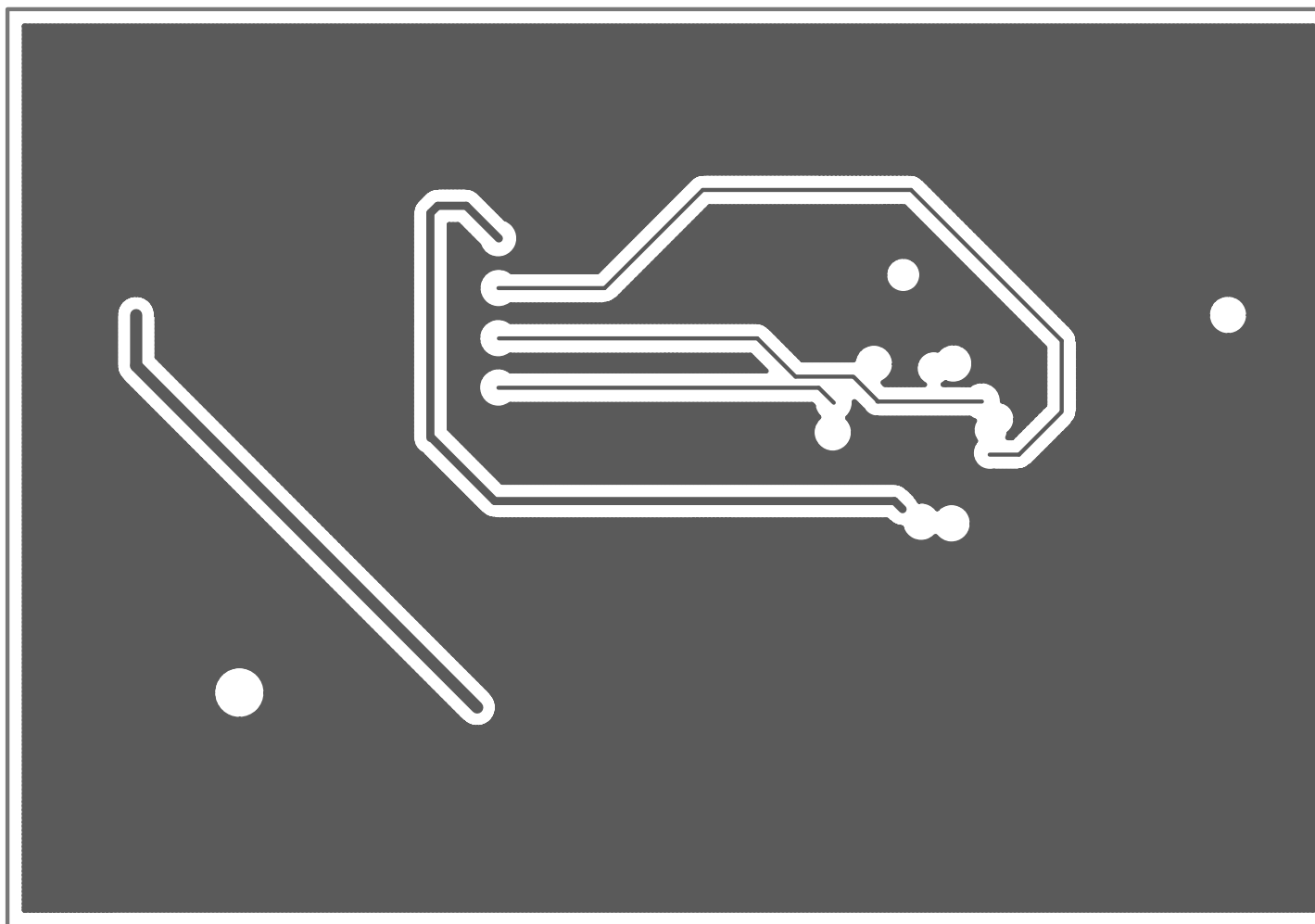
Top Layer



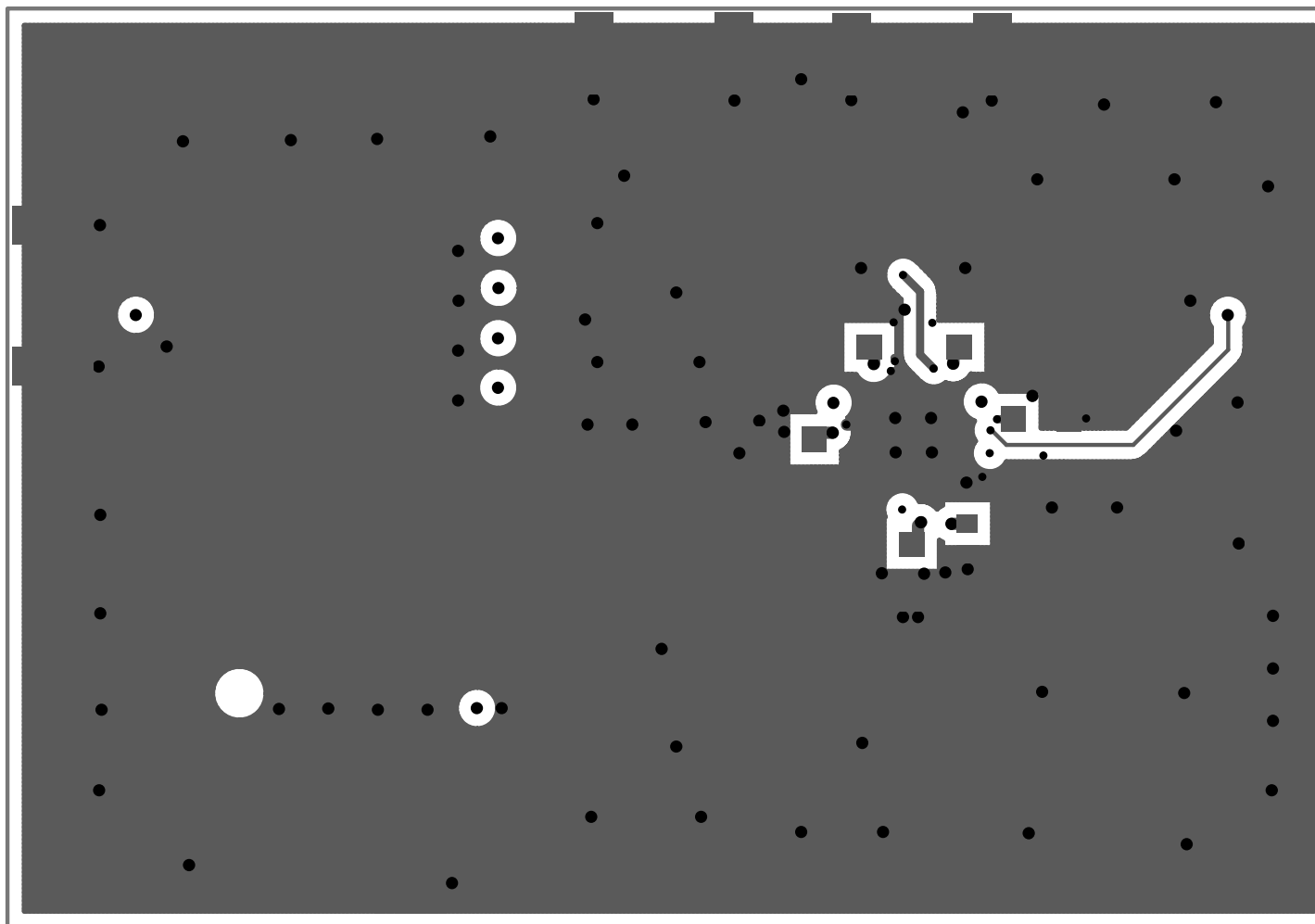
Mid Layer 1 "Ground Plane" (15 Mils Down FR4)



Mid Layer 2 "Power"

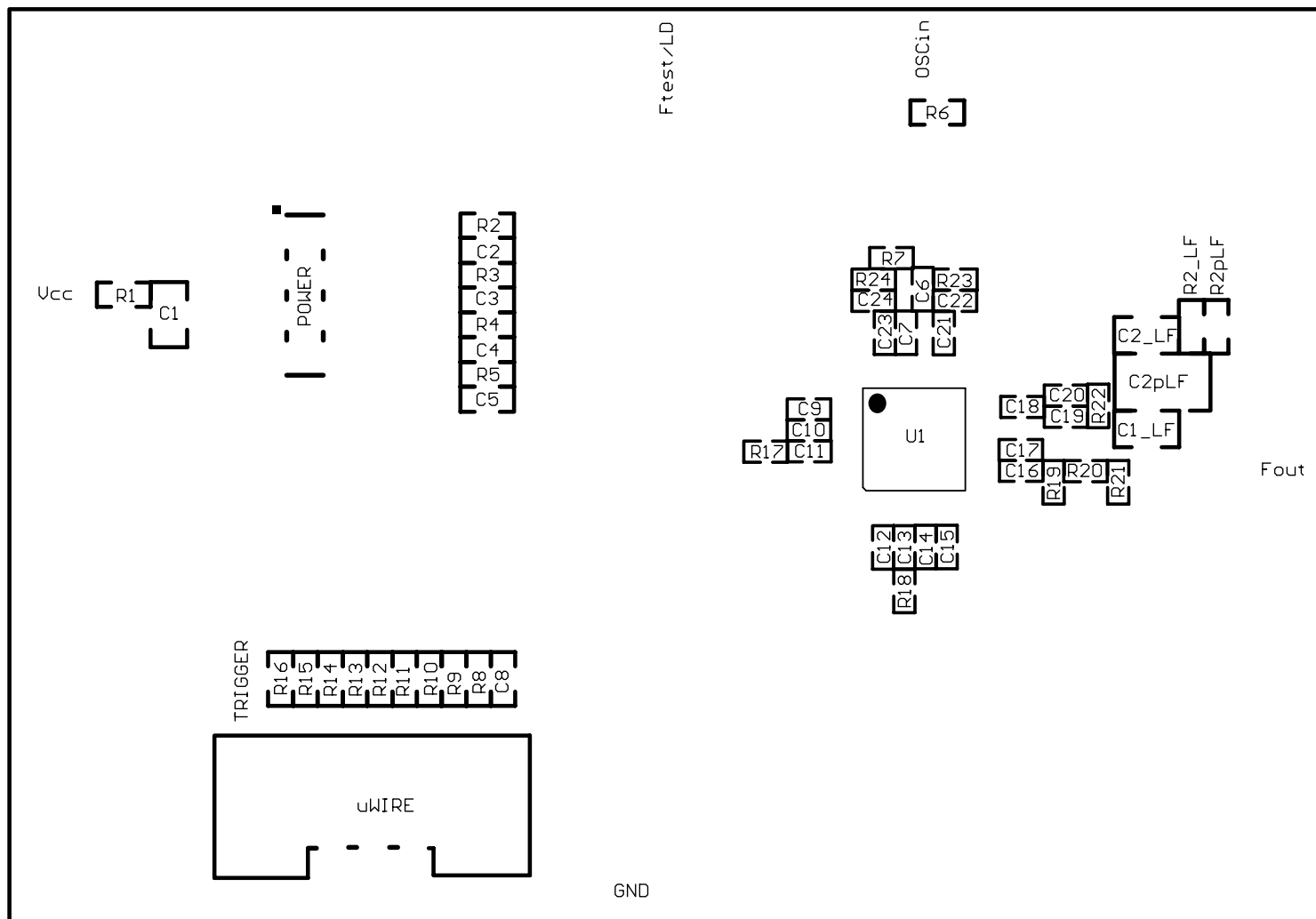


Bottom Layer "Signal"



Note: Total Board Thickness = 61 mils

Top Build Diagram



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