DisplayPort 1:2 Switch With Integrated TMDS Translator

FEATURES

- One Input Port to One of Two Output Ports
- Integrated TMDS Level Translator with Receiver Equalization
- DP Port Supports Data Rates up to 2.7 Gbps
- DP Port Supports Dual-Mode DisplayPort
- DP Port Output Waveform Mimics Input Waveform Characteristics
- TMDS Port Supports Data Rates up to 2.5 Gbps
- Integrated I^2C Logic Block for DVI/HDMI Connector Recognition
- Enhanced ESD:
  - 12 kV on all High Speed Pins
  - 8 kV on all Auxiliary and I^2C Pins
- Enhanced Commercial Temperature Range: 0°C to 85°C
- 56 Pin 8 × 8 QFN Package

APPLICATIONS

- Personal Computer Market
  - Desktop PC
  - Notebook PC
  - Docking Station
  - Standalone Video Card

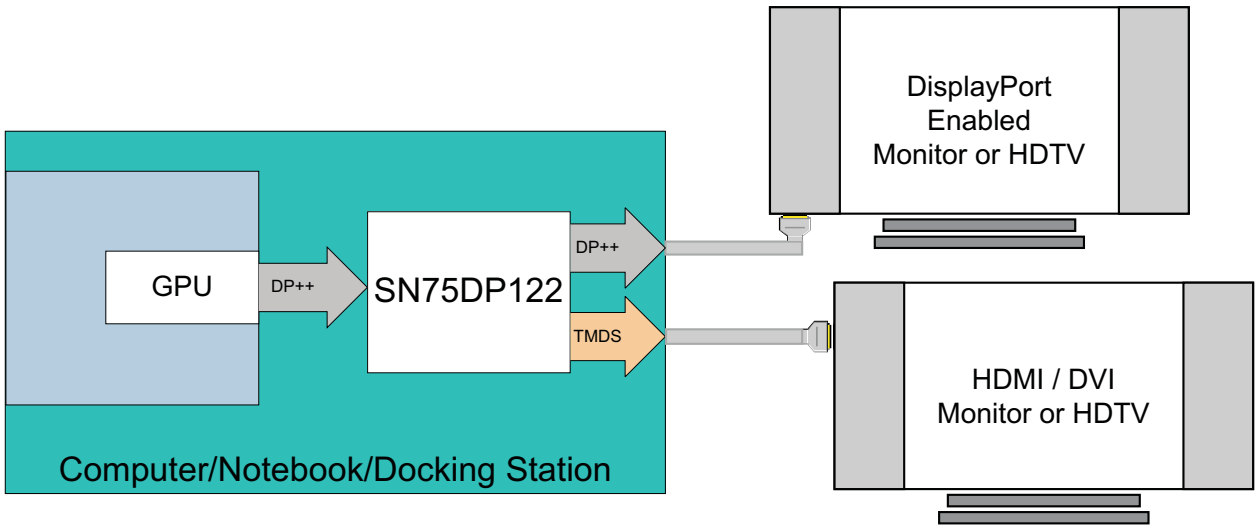
DESCRIPTION

The SN75DP122 is a one Dual-Mode DisplayPort input to one Dual-Mode DisplayPort output or one TMDS output. The TMDS output has a built in level translator compliant with Digital Video Interface (DVI) 1.0 and High Definition Multimedia Interface (HDMI) 1.3b. The DisplayPort output follows the input signal in a manner that provides the highest level of signal integrity while supporting the EMI benefits of spread spectrum clocking. Through the SN75DP122 data rates of up to 2.7 Gbps through each link for a total throughput of up to 10.8 Gbps can be realized.

In addition to the switching of the DisplayPort high speed signal lines, the SN75DP122 also supports the switching of the bidirectional auxiliary (AUX), Hot Plug Detect (HPD), and Cable Adapter Detect (CAD) channels. The Auxiliary differential pair supports Dual-Mode DisplayPort operation through the DisplayPort port. Through the TMDS port the auxiliary port is configured as an I^2C port with an integrated I^2C repeater.

The SN75DP122 is characterized for operation over ambient air temperature of 0°C to 85°C.

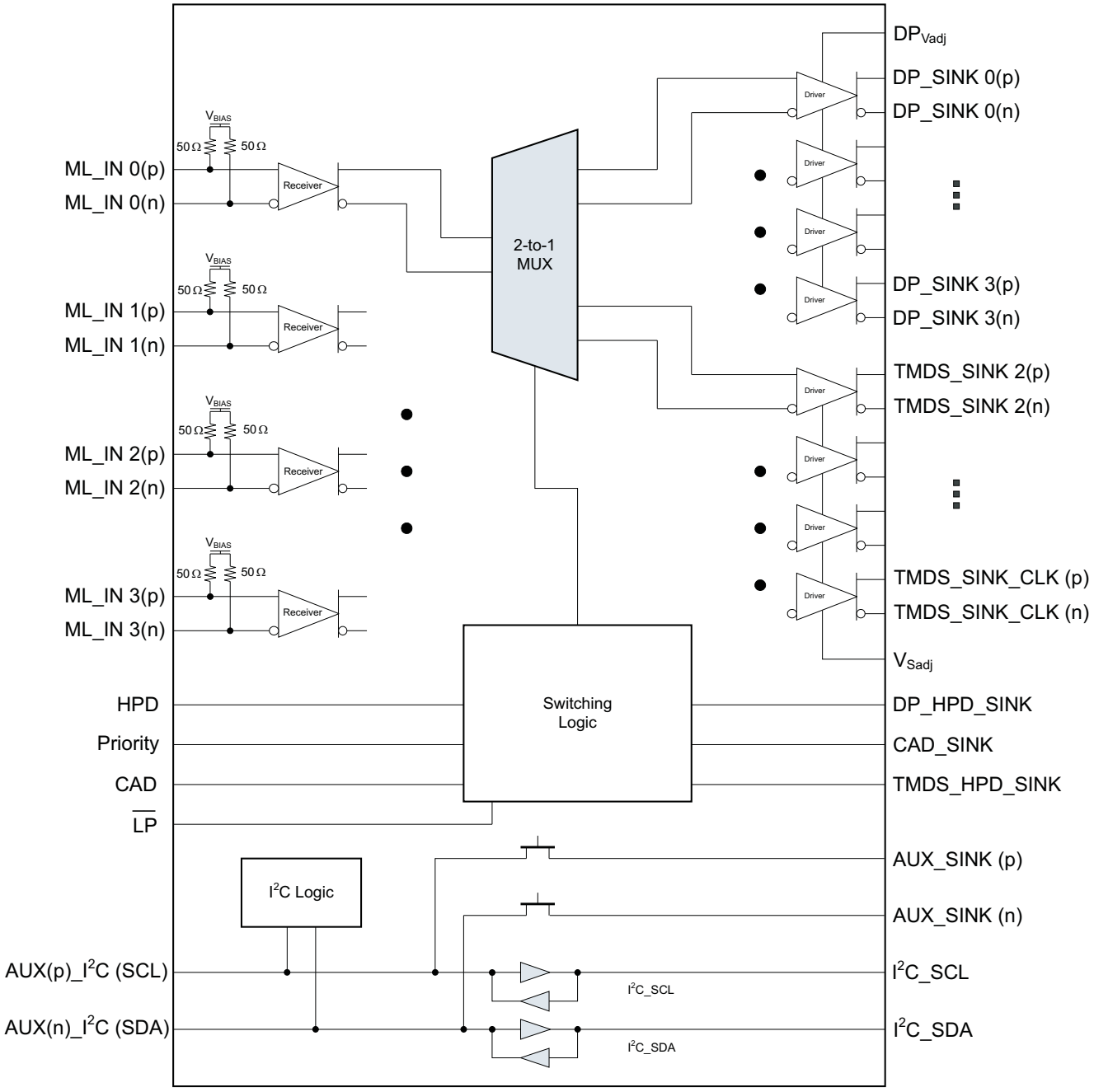
TYPICAL APPLICATION

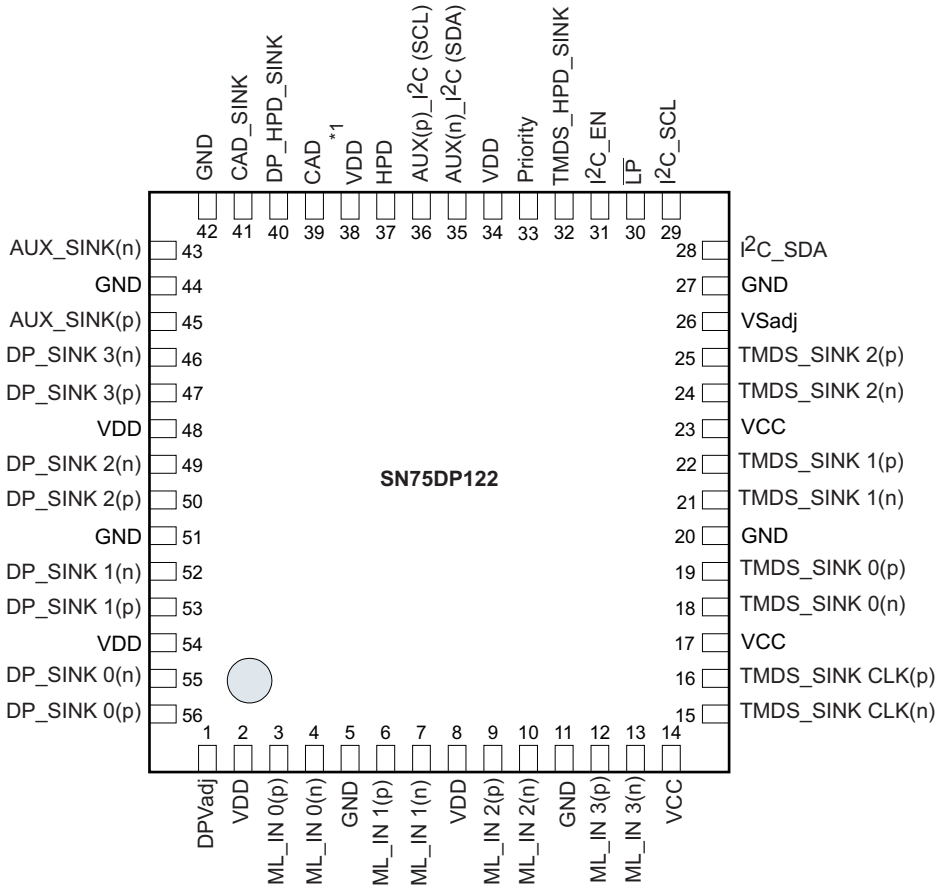


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DATA FLOW BLOCK DIAGRAM




SN75DP122
GND 42
CAD_SINK 41
DP_HPD_SINK 40
CAD *1 39
VDD 38
HPD 37
AUX(p)_I2C (SCL) 36
AUX(n)_I2C (SDA) 35
VDD 34
Priority 33
TMDS_HPD_SINK 32
I2C_EN 31
LP 30
I2C_SCL 29
AUX_SINK(n) 43
GND 44
AUX_SINK(p) 45
DP_SINK 3(n) 46
DP_SINK 3(p) 47
VDD 48
DP_SINK 2(n) 49
DP_SINK 2(p) 50
GND 51
DP_SINK 1(n) 52
DP_SINK 1(p) 53
VDD 54
DP_SINK 0(n) 55
DP_SINK 0(p) 56
28 I2C_SDA
27 GND
26 VSadj
25 TMDS_SINK 2(p)
24 TMDS_SINK 2(n)
23 VCC
22 TMDS_SINK 1(p)
21 TMDS_SINK 1(n)
20 GND
19 TMDS_SINK 0(p)
18 TMDS_SINK 0(n)
17 VCC
16 TMDS_SINK CLK(p)
15 TMDS_SINK CLK(n)
1 DPVadj
2 VDD
3 ML_IN 0(p)
4 ML_IN 0(n)
5 GND
6 ML_IN 1(p)
7 ML_IN 1(n)
8 VDD
9 ML_IN 2(p)
10 ML_IN 2(n)
11 GND
12 ML_IN 3(p)
13 ML_IN 3(n)
14 VCC

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
MAIN LINK INPUT PINS			
ML_IN 0	3, 4	I	DisplayPort main link channel 0 differential input
ML_IN 1	6, 7	I	DisplayPort main link channel 1 differential input
ML_IN 2	9, 10	I	DisplayPort main link channel 2 differential input
ML_IN 3	12, 13	I	DisplayPort main link channel 3 differential input
MAIN LINK PORT A OUTPUT PINS			
DP_SINK 0	56, 55	O	DisplayPort main link port a channel 0 differential output
DP_SINK 1	53, 52	O	DisplayPort main link port a channel 1 differential output
DP_SINK 2	50, 49	O	DisplayPort main link port a channel 2 differential output
DP_SINK 3	47, 46	O	DisplayPort main link port a channel 3 differential output
MAIN LINK PORT B OUTPUT PINS			
TMDS_SINK 2	25, 24	O	TMDS data 2 differential output
TMDS_SINK 1	22, 21	O	TMDS data 1 differential output
TMDS_SINK 0	19, 18	O	TMDS data 0 differential output
TMDS_SINK CLK	16, 15	O	TMDS data clock differential output
HOT PLUG DETECT PINS			
HPD	37	O	Hot plug detect output to the displayport source
DP_HPD_SINK	40	I	DisplayPort port hot plug detect input
TMDS_HPD_SINK	32	I	TMDS port hot plug detect input
AUXILIARY DATA PINS			
AUX_I^2C	36, 35	I/O	Source side bidirectional displayport auxiliary data line
AUX_SINK	45, 43	I/O	DisplayPort port bidirectional displayport auxiliary data line
I^2C_SCL I^2C_SDA	29, 28	I/O	TMDS port bidirectional ddc data lines
CABLE ADAPTER DETECT PINS			
CAD	39	O	Cable adapter detect output to the displayport source
CAD_SINK	41	I	DisplayPort cable adapter detect input
CONTROL PINS			
$\overline{LP}$	30	I	Low power select bar
Priority	33	I	Output port priority selection
DPVadj	1	I	DisplayPort main link output gain adjustment
VSadj	26	I	TMDS compliant voltage swing control
I^2C_EN	31	I	Internal I^2C register enable, used for HDMI / DVI connector differentiation
SUPPLY and GROUND PINS			
VDD	2, 8, 34, 48, 54		5-V supply
VDD[*1]	38		HPD/CAD supply
VCC	14, 17, 23		3.3-V supply
GND	5, 11, 20, 27, 42, 44, 51		Ground

Table 1. Control Pin Lookup Table

SIGNAL	LEVEL(1)	STATE	DESCRIPTION
$\overline{LP}$	H	Normal Mode	Normal operational mode for device
	L	Low Power Mode	Device is forced into a low power state causing the outputs to go to a high impedance state. All other inputs are ignored
Priority	H	TMDS Port has Priority	If both DP_HPD_SINK and TMDS_HPD_SINK are high, the TMDS port is selected
	L	DP Port has Priority	If both DP_HPD_SINK and TMDS_HPD_SINK are high, the DP port is selected
I^2C_EN	H	HDMI	The Internal I^2C register is active and readable when the TMDS port is selected indicating that the connector being used is HDMI
	L	DVI	The Internal I^2C register is disabled and not readable when the TMDS port is selected indicating that the connector being used is DVI
DP_{Vadj}	4.53 kΩ	Increased Gain	Main link displayport output has an increased voltage swing
	6.49 kΩ	Nominal Gain	Main link displayport output has a nominal voltage swing
	10 kΩ	Decreased Gain	Main link displayport output has a decreased voltage swing
VS_{adj}	5.11 kΩ	Compliant Voltage Swing	Driver output voltage swing precision control to aid with system compliance

(1) (H) Logic High; (L) Logic Low

Explanation of the internal switching logic of the SN75DP122 is located in the application section at the end of this data sheet.

ORDERING INFORMATION(1)

PART NUMBER	PART MARKING	PACKAGE
SN75DP122RTQR	75DP122	56-pin QFN Reel (large)
SN75DP122RTQT	75DP122	56-pin QFN Reel (small)

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

			VALUE	UNIT
Supply voltage range(2)	V_{DD}, V_{DD}*1		–0.3 to 5.25	V
Supply voltage range	V_{CC}		–0.3 to 3.6	V
Voltage range	Main Link I/O (ML_IN x, DP_SINK x) Differential Voltage		1.5	V
	TMDS I/O		–0.3 to 4	V
	HPD and CAD I/O		–0.3 to 5.25	V
	Auxiliary I/O		–0.3 to 5.25	V
	Control I/O		–0.3 to 5.25	V
Electrostatic discharge	Human body model(3)	Auxiliary and I^2C I/O	±8000	V
		All other pins	±12000	
	Charged-device model(3)		±1000	V
	Machine model(4)		±200	V
Continuous power dissipation			See Dissipation Rating Table	

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-B
(4) Tested in accordance with JEDEC Standard 22, Test Method A115-A

DISSIPATION RATINGS

PACKAGE	PCB JEDEC STANDARD	T_A < 25°C	DERATING FACTOR(1) ABOVE T_A = 25°C	T_A = 85°C POWER RATING
56-Pin QFN (RTQ)	Low-K	3623 mW	36.23 mW/°C	1449 mW
	High-K	1109 mW	11.03 mW/°C	443.9 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX(1)	UNIT
$R_{\theta JB}$	Junction-to-board thermal resistance	4x4 Thermal vias under powerpad		11.03		°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance			20.4		C/W
$P_{D(1)}$	Device power dissipation DisplayPort selected	$\overline{LP}$ = 5 V, ML: V_{ID} = 600 mV, 2.7 Gbps PRBS; AUX: V_{ID} = 500 mV, 1 Mbps PRBS; HPD/CAD = 5 V; V_{DD}*1 = V_{DD}		250	305	mW
$P_{D(2)}$	Device power dissipation TMDS selected	$\overline{LP}$ = 5 V, ML: V_{ID} = 500 mV, 2.5 Gbps PRBS; I^2C: V_{ID} = 3.3 V, 100 Kbps PRBS; HPD/CAD = 5 V; V_{DD}*1 = V_{DD}		270	420	mW
P_{SD}	Device power dissipation under low power	$\overline{LP}$ = 0 V, ML: V_{ID} = 600 mV, 2.7 Gbps PRBS; AUX: V_{ID} = 500 mV, 1 Mbps PRBS; HPD/CAD = 5 V; V_{DD}*1 = V_{DD}		75	85	µW

(1) The maximum rating is simulated under 5.25 V VDD.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	4.5	5	5.25	V
V_{DD}*1	HPD and CAD output reference voltage	1.62		5.25	V
V_{CC}	Supply voltage	3	3.3	3.6	V
T_A	Operating free-air temperature	0		85	°C
MAIN LINK DIFFERENTIAL PINS					
V_{ID}	Peak-to-peak input differential voltage	0.15		1.40	V
d_R	Data rate			2.7	Gbps
R_t	Termination resistance	45	50	55	Ω
V_{Oterm}	Output termination voltage	0		2	V
TMDS DIFFERENTIAL OUTPUT PINS					
AV_{CC}	TMDS output termination voltage	3	3.3	3.6	V
d_R	Data rate			2.5	Gbps
R_t	Termination resistance	45	50	55	Ω
AUXILIARY AND I^2C PINS					
V_I	Input voltage	0		5.25	V
$d_{R(AUX)}$	Auxiliary data rate			1	MHz
$d_{R(I2C)}$	I^2C data rate			100	kHz
HPD, CAD, AND CONTROL PINS					
V_{IH}	High-level input voltage	2		5.25	V
V_{IL}	Low-level input voltage	0		0.8	V

DEVICE POWER

The SN75DP122 is designed to operate off of two supply voltages. The DisplayPort port and the digital logic run off of the 5V supply voltage. The TMDS level translator is powered off of the 3.3V supply.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	Supply current	LP = 5 V, V_{DD}*1 = V_{DD}, Priority = 0 V ML: V_{ID} = 600 mV, 2.7 Gbps PRBS AUX: V_{ID} = 500 mV, 1 Mbps PRBS DP/TMDS_HPD_SINK and CAD_SINK = 5 V		60	65	mA
I_{CC}				0.1	0.25	
$I_{DD(2)}$	Supply current	LP = 5 V, V_{DD}*1 = V_{DD}, Priority = 1 V ML: V_{ID} = 500 mV, 2.5 Gbps PRBS AUX: V_I = 2 V, 100 kHz DP/TMDS_HPD_SINK and CAD_SINK = 5 V		2	4	mA
$I_{CC(2)}$				80	110	
I_{DD}*1	Supply current	V_{DD}*1 = 5.25 V		0.1	4	mA
I_{SD}	Shutdown current	$\overline{LP}$ = 0 V		1	16	µA

HOT PLUG AND CABLE ADAPTER DETECT

The SN75DP122 is designed to support the switching of the Hot Plug Detect and Cable adapter Detect signals. The SN75DP122 has a built in level shifter for the HPD and CAD outputs. The output voltage level of the HPD and CAD pins is defined by the voltage level of the V_{DD}*1 pin.

When the DisplayPort port is selected, the state of CAD_SINK is propagated to the CAD output pin. If the TMDS port is selected, the CAD output pin stays HIGH as long as that port is selected.

Explanation of HPD and the internal logic of the SN75DP122 is located in the application section at the end of the data sheet.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH5}	High-level output voltage	I_{OH} = –100 µA,	V_{DD}*1 = 5 V	4.5		5	V
$V_{OH3.3}$	High-level output voltage	I_{OH} = –100 µA,	V_{DD}*1 = 3.3 V	3		3.3	V
$V_{OH2.5}$	High-level output voltage	I_{OH} = –100 µA,	V_{DD}*1 = 2.5 V	2.25		2.5	V
$V_{OH1.8}$	High-level output voltage	I_{OH} = –100 µA,	V_{DD}*1 = 1.8 V	1.62		1.8	V
V_{OL}	Low-level output voltage	I_{OH} = 100 µA,		0		0.4	V
I_H	High-level input current	V_{IH} = 2.0 V,	V_{DD} = 5.25 V	–10		10	µA
I_L	Low-level input current	V_{IL} = 0.8 V,	V_{DD} = 5.25 V	–10		10	µA

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PD(CAD)}$	Propagation delay	V_{DD}*1 = 5 V	5		30	ns
$t_{PD(HPD)}$	Propagation delay	V_{DD}*1 = 5 V	30		110	ns
$t_{T1(HPD)}$	HPD logic switch pause time	V_{DD}*1 = 5 V	2		4.7	ms
$t_{T2(HPD)}$	HPD logic switch time	V_{DD}*1 = 5 V	170		400	ms
$t_{M(HPD)}$	Minimum output pulse duration	V_{DD}*1 = 5 V	100			ns
$t_{Z(HPD)}$	Low power to high-level propagation delay	V_{DD}*1 = 5 V	30	50	110	ns

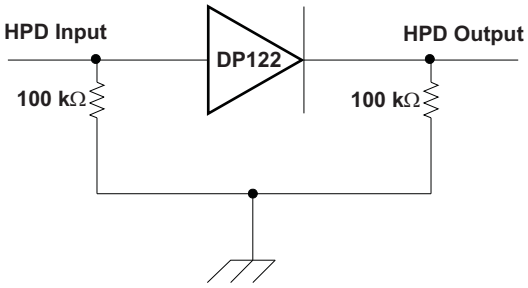


Figure 1. HPD Test Circuit

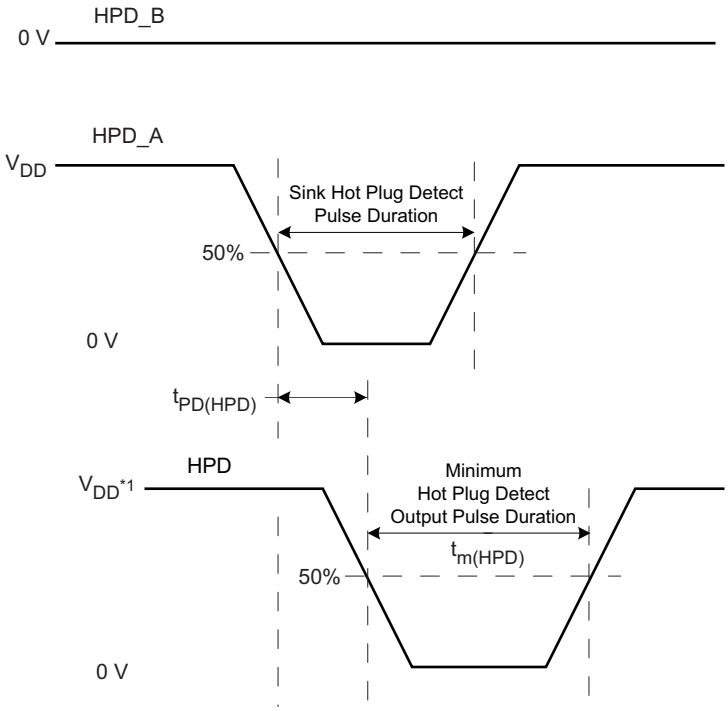


Figure 2. HPD Timing Diagram #1

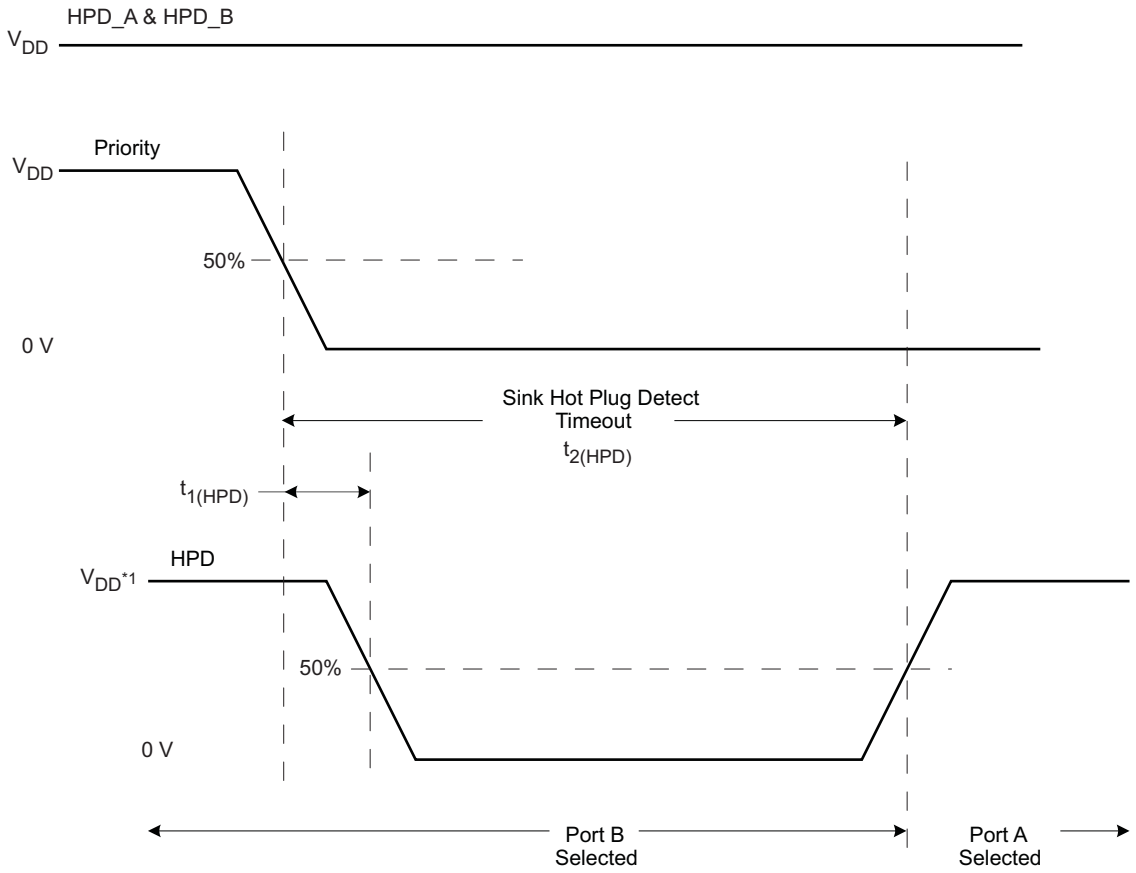


Figure 3. HPD Timing Diagram #2

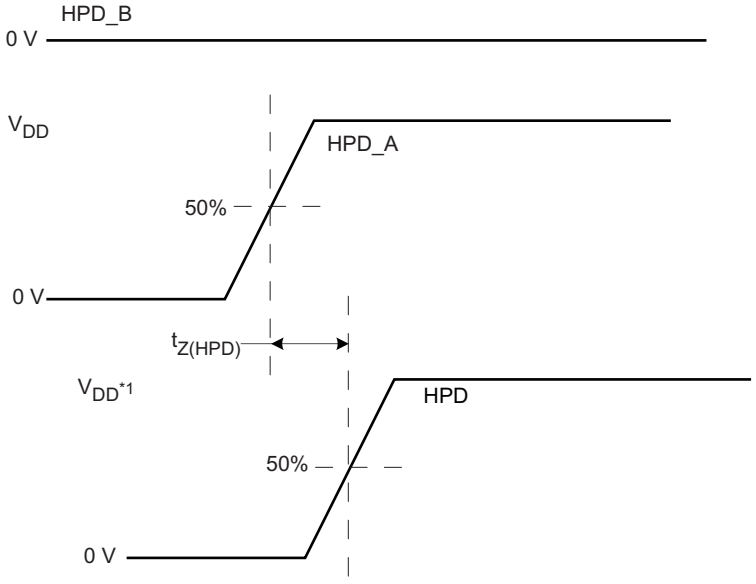


Figure 4. HPD Timing Diagram #3

DisplayPort Auxiliary Pins

The SN75DP122 is designed to support the bidirectional auxiliary signals through the DisplayPort port in both a differential (DisplayPort) mode and an I^2C (DVI, HDMI) mode. The performance of the Auxiliary bus is optimized based on the status of the CAD_SINK pin.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{Pass1}	Maximum passthrough voltage (CAD=1)	V_{DD} = 4.5 V, V_I = 5 V, I_O = 100 µA	2.4		3.6	V
I_{OZ}	Output current from unselected output	V_{DD} = 5.25 V, V_O = 0 V to 3.6 V, V_I = 0 V	–5		5	µA
$C_{IO(off)}$	I/O capacitance when in low power	DC bias = 1 V, AC = 1.4 V_{p-p}, F = 100 kHz, CAD = High		9	12	pF
$C_{IO(on)}$	I/O capacitance when in normal operation	DC bias = 1 V, AC = 1.4 V_{p-p}, F = 100 kHz, CAD = Low		18	25	pF
$r_{ON(C0)}$	On resistance	V_{DD} = 4.5 V, V_I = 0 V or 3.6 V, I_O = 5 mA, CAD = Low		5	10	Ω
Δr_{ON}	On resistance	V_{DD} = 4.5 V, V_I = 0 V or 2 V, I_O = 5 mA, CAD = Low		1	5	Ω
$r_{ON(C1)}$	On resistance	V_{DD} = 4.5 V, V_I = 0.4 V , I_O = 3 mA , CAD = High		10	18	Ω

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{sk(AUX)}$	Intra-pair skew	V_{ID} = 400 mV, V_{IC} = 2 V		40	80	ps
$I_{L(AUX)}$	Single Line Insertion Loss	V_{ID} = 500 mV, V_{IC} = 2 V, F = 1 MHz, CAD = Low			0.4	dB
$t_{PLH(AUXC0)}$	Propagation delay time, low to high	CAD = Low, F = 1 MHz			3	ns
$t_{PHL(AUXC0)}$	Propagation delay time, high to low	CAD = Low, F = 1 MHz			3	ns
$t_{PLH(AUXC1)}$	Propagation delay time, low to high	CAD = High, F = 100 kHz			3	ns
$t_{PHL(AUXC1)}$	Propagation delay time, high to low	CAD = High, F = 100 kHz			3	ns

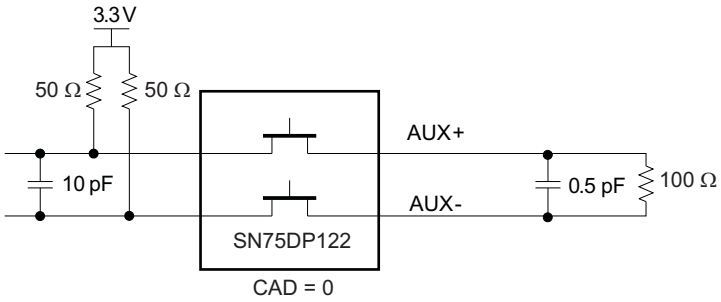


Figure 5. Auxiliary Channel Test Circuit (CAD = LOW)

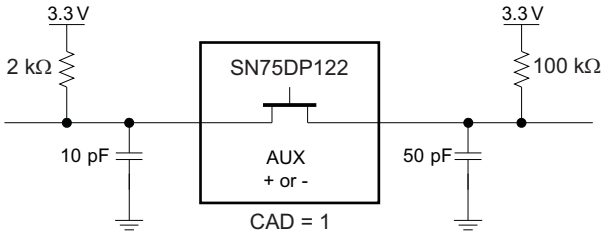


Figure 6. Auxiliary Channel Test Circuit (CAD = HIGH)

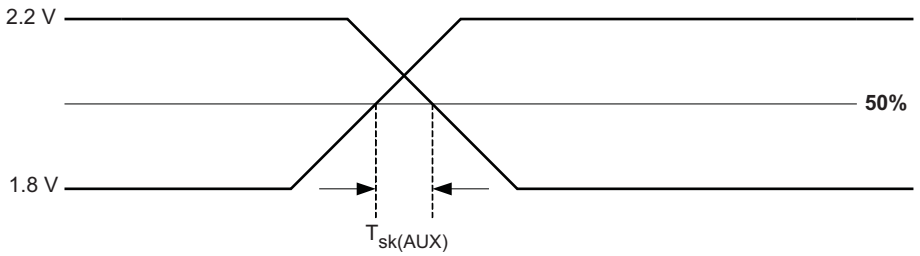


Figure 7. Auxiliary Channel Skew Measurement

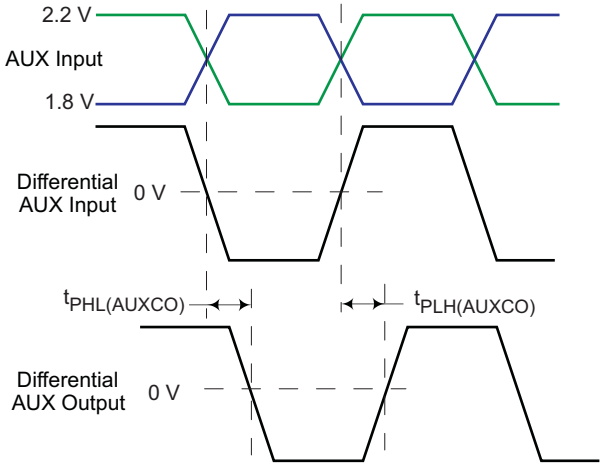


Figure 8. Auxiliary Channel Delay Measurement (CAD = LOW)

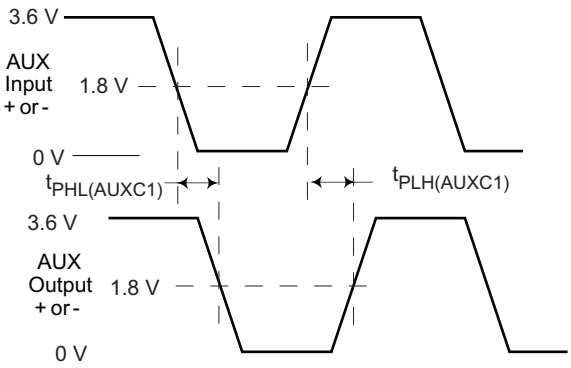


Figure 9. Auxiliary Channel Delay Measurement (CAD = HIGH)

DisplayPort Link Pins

The SN75DP122 is designed to support DisplayPort's high speed differential main link through the DisplayPort port. The main link I/O of the SN75DP122 are designed to track the magnitude and frequency characteristics of the input waveform and replicate them on the output. A feature has also been incorporated in the SN75DP122 to increase the either increase of decrease the output amplitude via the resistor connected between the DPVADJ pin and ground.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\Delta V_{I/O(2)}$	Difference between input and output) voltages ($V_{OD} - V_{ID}$)	V_{ID} = 200 mV, DPV_{adj} = 6.5 kΩ	0	30	60	mV
$\Delta V_{I/O(3)}$		V_{ID} = 300 mV, DPV_{adj} = 6.5 kΩ	–24	11	36	mV
$\Delta V_{I/O(4)}$		V_{ID} = 400 mV, DPV_{adj} = 6.5 kΩ	–45	–15	15	mV
$\Delta V_{I/O(6)}$		V_{ID} = 600 mV, DPV_{adj} = 6.5 kΩ	–87	–47	–22	mV
R_{INT}	Input termination impedance		45	50	55	Ω
V_{Iterm}	Input termination voltage		0		2	V

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{R/F(DP)}$	Output edge rate (20%–80%)	Input edge rate = 80 ps (20%–80%)		115	160	ps
t_{PD}	Propagation delay time	F= 1 MHz, V_{ID} = 400 mV		227		ps
$t_{SK(1)}$	Intra-pair skew	F= 1 MHz, V_{ID} = 400 mV			20	ps
$t_{SK(2)}$	Inter-pair skew	F= 1 MHz, V_{ID} = 400 mV			40	ps
$t_{DPJIT(PP)}$	Peak-to-peak output residual jitter	d_R = 2.7 Gbps, V_{ID} = 400 mV, PRBS 27-1		25	35	ps

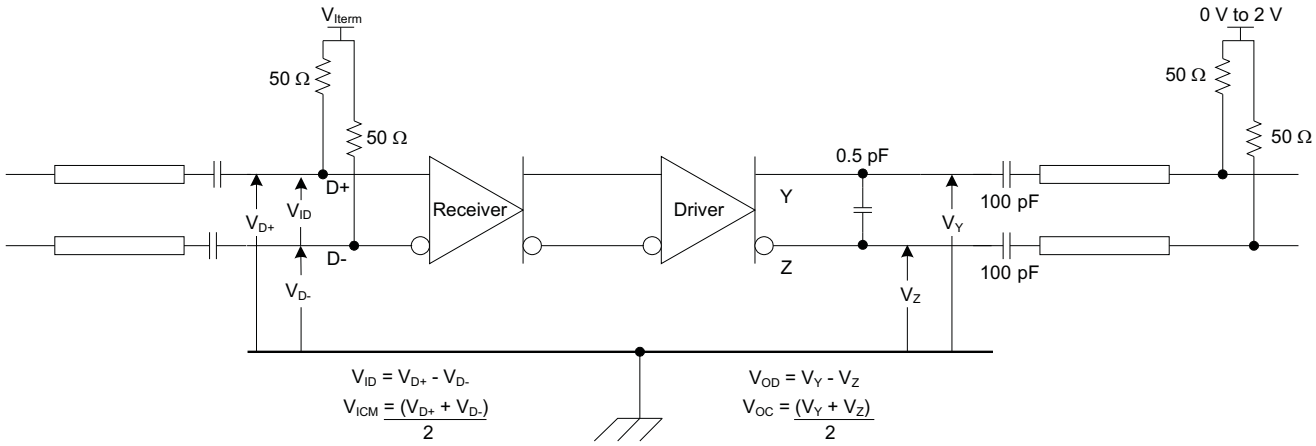


Figure 10. Main Link Test Circuit

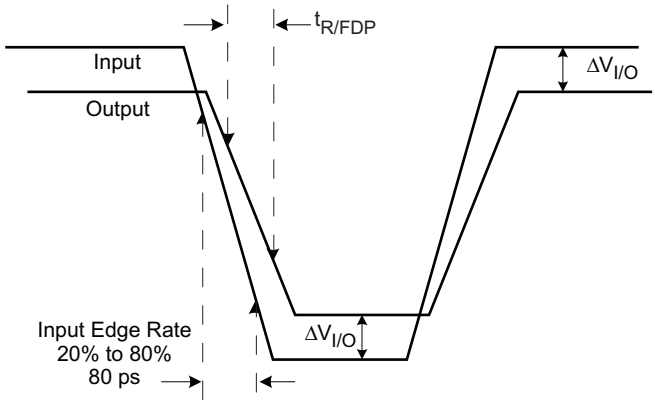


Figure 11. Main Link $\Delta V_{I/O}$ and Edge Rate Measurements

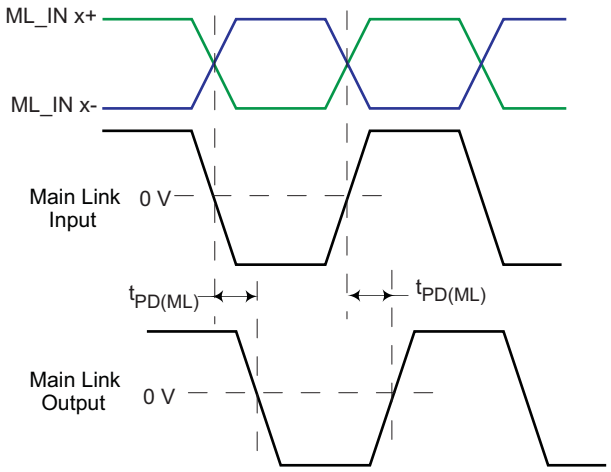


Figure 12. Main Link Delay Measurements

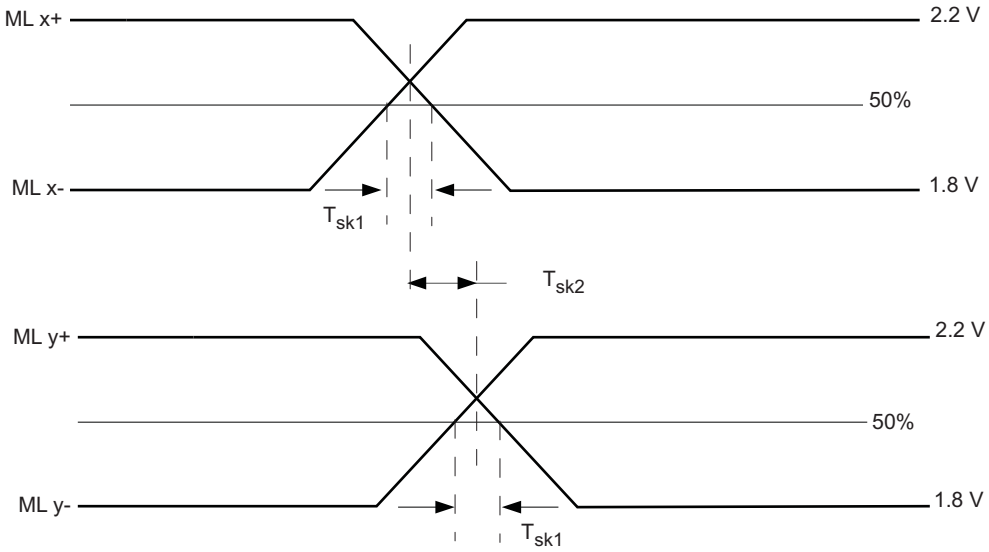


Figure 13. Main Link Skew Measurements

TMDS I²C Pins

When the TMDS port is selected the SN75DP122 utilizes an I²C repeater. The repeater is designed to isolate the parasitic effects of the system in order to aid with system level compliance.

In addition to the I²C repeater, the SN75DP122 also supports the connector detection I²C register. This register is enabled via the I²C_EN pin. When active an internal memory register is readable via the AUX_I²C I/O. The functionality of this register block is described in the application section

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_L	Low input current		V_{CC} = 3.6 V, V_I = 0 V			10	µA
$I_{lkg(AUX)}$	Input leakage	AUX_I²C pins	V_{CC} = 3.6 V, V_I = 3.6 V	–10		10	µA

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$C_{IO(AUX)}$	Input/output capacitance	AUX_I²C pins	DC bias = 1 V, AC = 1.4 V_{p-p}, f = 100 kHz			15	pF
$V_{IH(AUX)}$	High-level input voltage	AUX_I²C pins		1.6			V
$V_{IL(AUX)}$	Low-level input voltage	AUX_I²C pins		–0.2		0.4	V
$V_{OL(AUX)}$	Low-level output voltage	AUX_I²C pins	I_O = 4 mA	0.5		0.6	V
$I_{lkg(I2C)}$	Input leakage current	I²C SDA/SCL pins	V_{CC} = 3.6 V, V_I = 4.95 V	–10		10	µA
$C_{IO(I2C)}$	Input/output capacitance	I²C SDA/SCL pins	DC bias = 2.5 V, AC = 3.5 V_{p-p}, f = 100 kHz			15	pF
$V_{IH(I2C)}$	High-level input voltage	I²C SDA/SCL pins		2.1			V
$V_{IL(I2C)}$	Low-level input voltage	I²C SDA/SCL pins		-0.2		1.5	V
$V_{OL(I2C)}$	Low-level output voltage	I²C SDA/SCL pins	IO = 4 mA			0.2	V

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH1}	Propagation delay time, low to high	Source to sink	204		459	ns
t_{PHL1}	Propagation delay time, high to low	Source to sink	35		140	ns
t_{PLH2}	Propagation delay time, low to high	Sink to source	80		251	ns
t_{PHL2}	Propagation delay time, high to low	Sink to source	35		200	ns
t_{f1}	Output signal fall time	Sink side	20		72	ns
t_{f2}	Output signal fall time	Source side	20		72	ns
f_{SCL}	SCL clock frequency for internal register	Source side			100	kHz
$t_{W(L)}$	Clock LOW period for I²C register	Source side	4.7			µs
$t_{W(H)}$	Clock HIGH period for internal register	Source side	4.0			µs
t_{SU1}	Internal register setup time, SDA to SCL	Source side	250			ns
$t_{h(1)}$	Internal register hold time, SCL to SDA	Source side	0			µs
$T_{(buf)}$	Internal register bus free time between STOP and START	Source side	4.7			µs
$t_{su(2)}$	Internal register setup time, SCL to START	Source side	4.7			µs
$t_{h(2)}$	Internal register hold time, START to SCL	Source side	4.0			µs
$t_{su(3)}$	Internal register hold time, SCL to STOP	Source side	4.0			µs

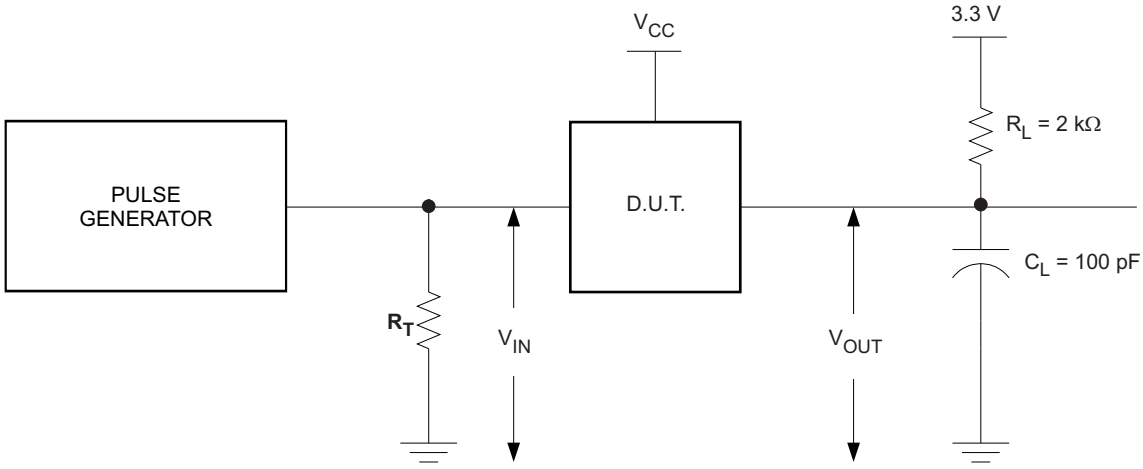


Figure 14. Source Side Test Circuit (AUX_I²C)

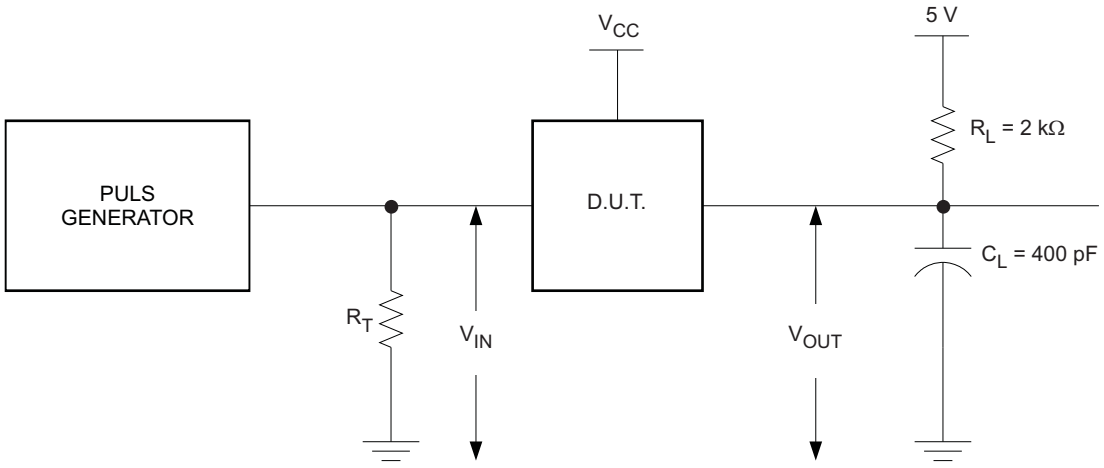


Figure 15. Sink Side Test Circuit (SCL, SDA)

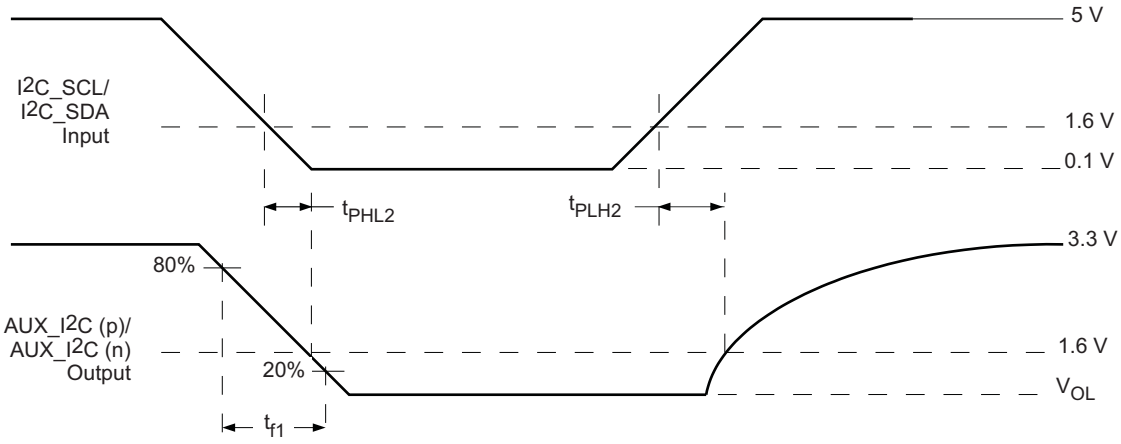


Figure 16. Source Side Output AC Measurements

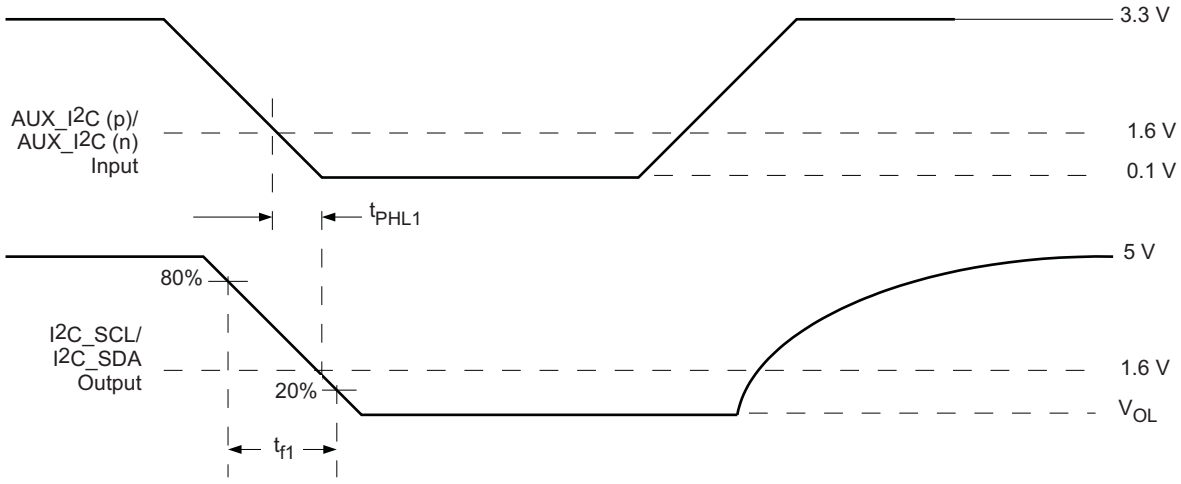


Figure 17. Sink Side Output AC Measurements

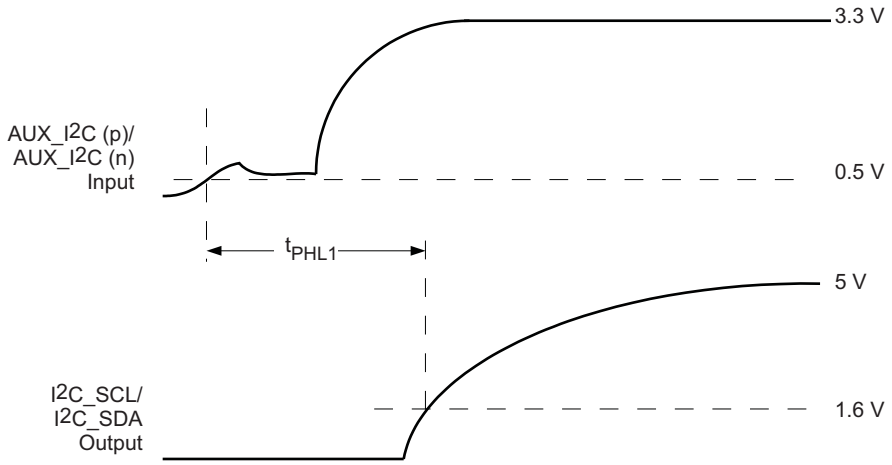


Figure 18. Sink Side Output AC Measurements Continued

TMDS MAIN LINK PINS

The TMDS port of the SN75DP122 is designed to be compliant with the Digital Video Interface (DVI) 1.0 and High Definition Multimedia Interface (HDMI) 1.3 specifications. The differential output voltage swing can be fine tuned with the VSadj resistor.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	Single-ended HIGH level output voltage	AVCC = 3.3 V, R_T = 50 Ω	AVCC –10		AVCC+10	mV
V_{OL}	Single-ended LOW level output voltage		AVCC –600		AVCC –400	mV
V_{SWING}	Single-ended output voltage swing		400		600	mV
$V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states		–5		5	mV
$V_{OD(PP)}$	Peak-to-Peak output differential voltage		800		1200	mV
$V_{(O)SBY}$	Single-ended standby output voltage	AVCC = 3.3 V, R_T = 50 Ω, DP Port Selected	AVCC –10		AVCC+10	mV
$I_{(O)OFF}$	Single-ended power down output current	0 V ≤ VCC ≤ 1.5 V , AVCC = 3.3 V, R_T = 50 Ω	–10		10	µA
I_{OS}	Short circuit output current	VID = 500 mV	–15		15	mA

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time	AVCC = 3.3 V, R_T = 50 Ω, f = 1 MHz	250	480	600	ps
t_{PHL}	Propagation delay time		250	400	800	ps
t_R	Rise time		60	90	140	ps
t_F	Fall time		60	90	140	ps
$t_{SK(P)}$	Pulse skew			8	15	ps
$t_{SK(D)}$	Intra-pair skew			20	40	ps
$t_{SK(O)}$	Inter-pair skew			20	65	ps
$t_{JITD(PP)}$	Peak-to-peak output residual data jitter	AVCC = 3.3 V, R_T = 50 Ω, dR = 2.5 Gbps		20	50	ps
$t_{JITC(PP)}$	Peak-to-peak output residual clock jitter	AVCC = 3.3 V, R_T = 50 Ω, f = 250 MHz		10	30	ps

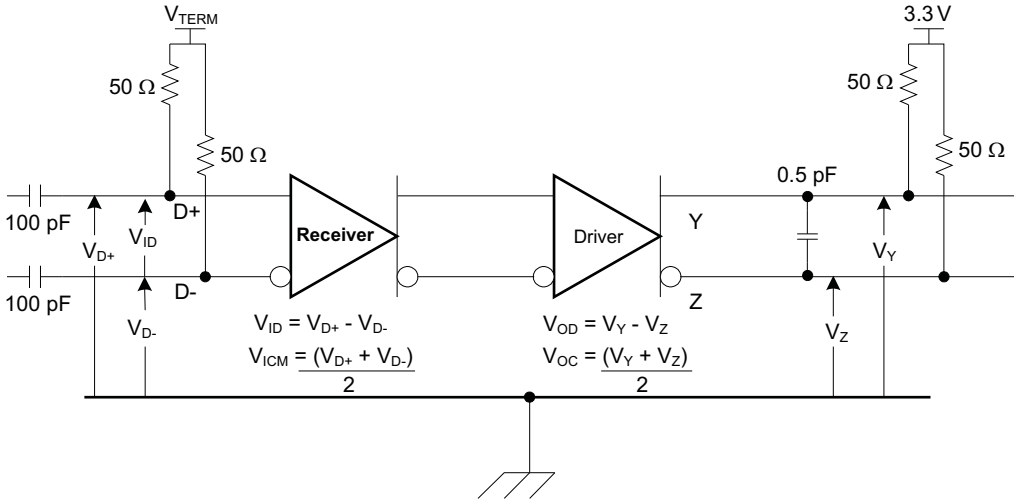


Figure 19. TMDS Main Link Test Circuit

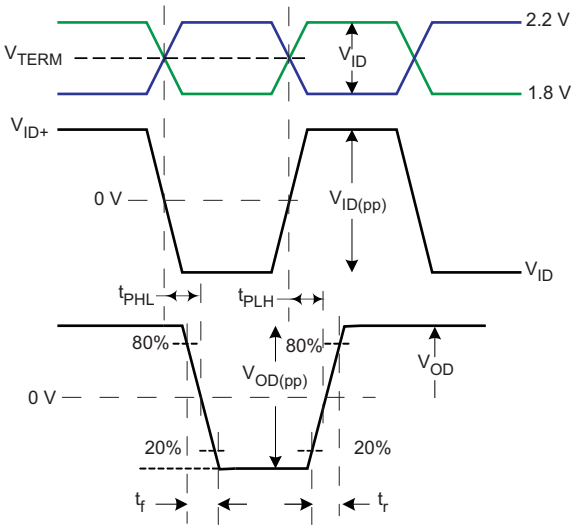


Figure 20. TMDS Main Link Timing Measurements

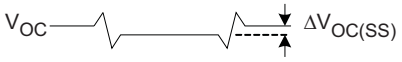
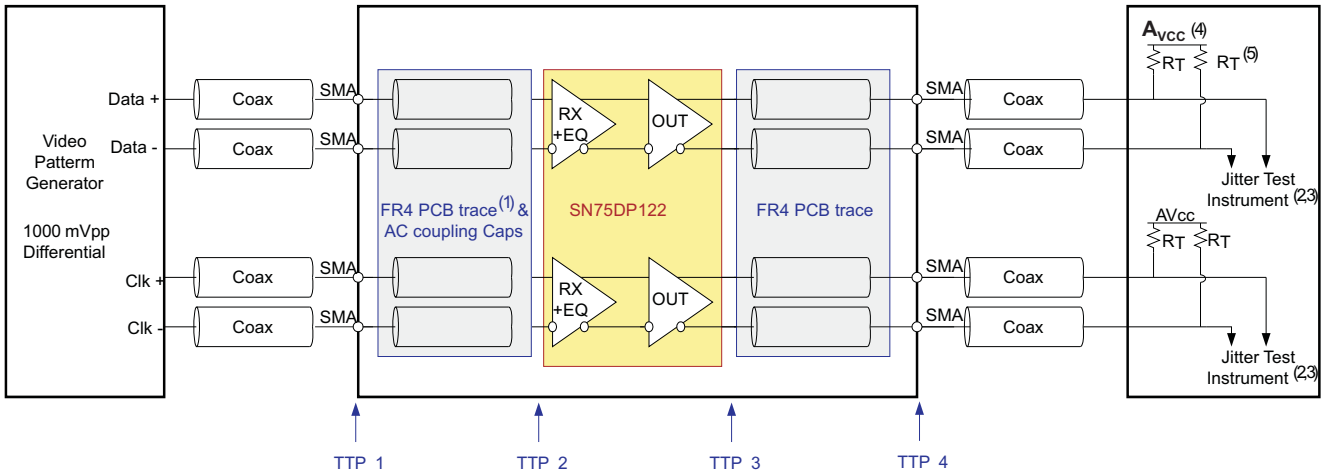


Figure 21. TMDS Main Link Common Mode Measurements



(1) The FR4 trace between TTP1 and TTP2 is designed to emulate 8" of FR4, a connector, and another 8" of FR4.

(2) All Jitter is measured at a BER of 10^{-12}

(3) Residual jitter reflects the total jitter measured at TTP4 minus the jitter measured at TTP1

(4) AVCC = 3.3 V

(5) R_T = 50 Ω

Figure 22. TMDS Jitter Measurements

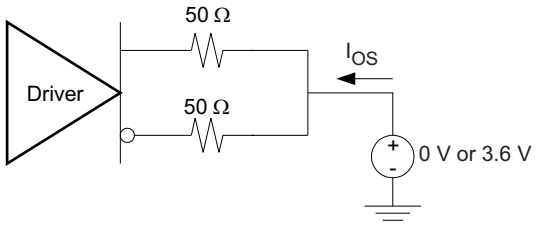


Figure 23. TMDS Main Link Short Circuit Output Circuit

TYPICAL CHARACTERISTICS

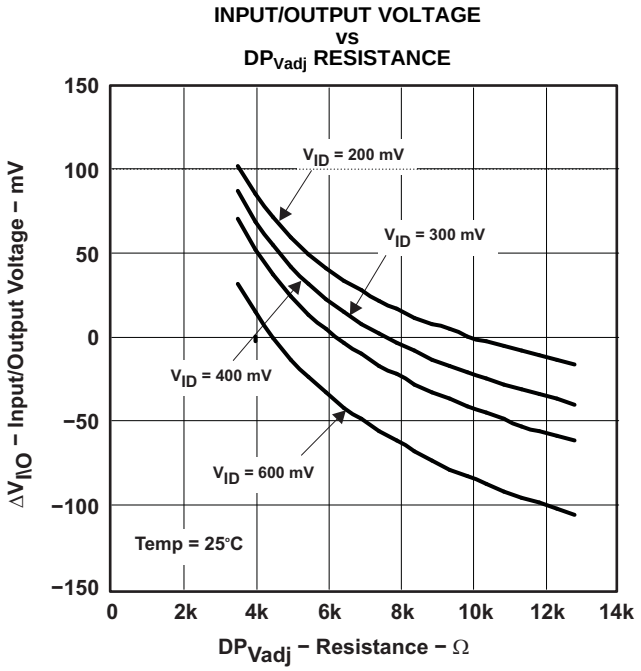


Figure 24.

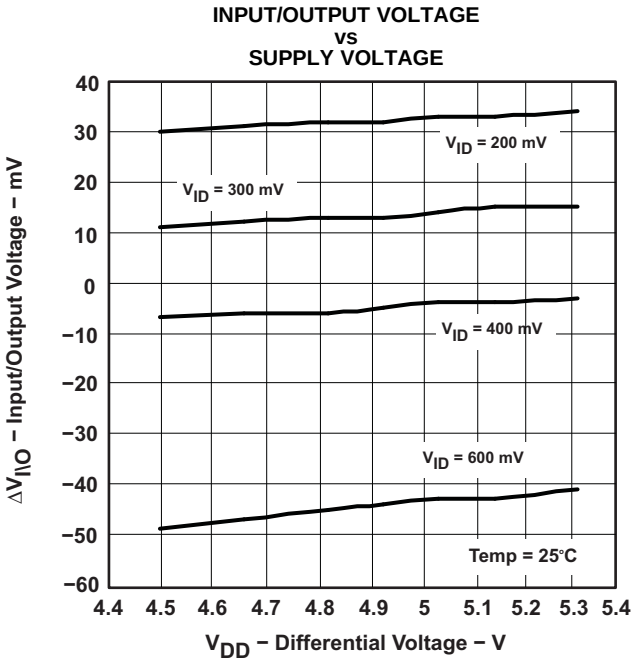


Figure 25.

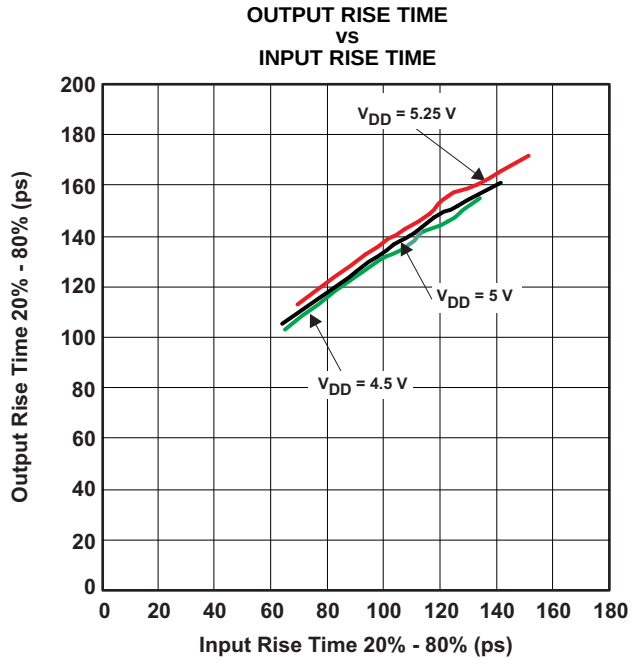
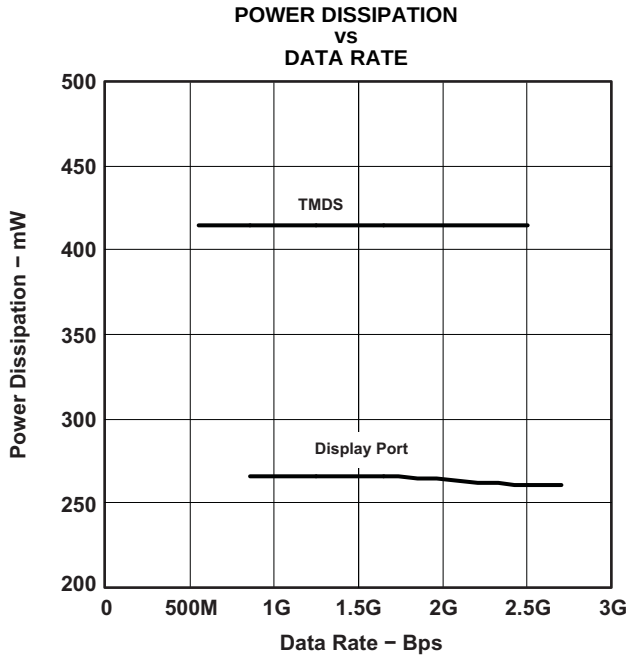


Figure 26.



(1) TMDS power dissipation in this graph includes 132 mW of power supplied by the AVCC termination.

Figure 27.

TYPICAL CHARACTERISTICS (continued)

TMDS PORT SUPPLY VOLTAGE
vs
RESIDUAL DATA JITTER

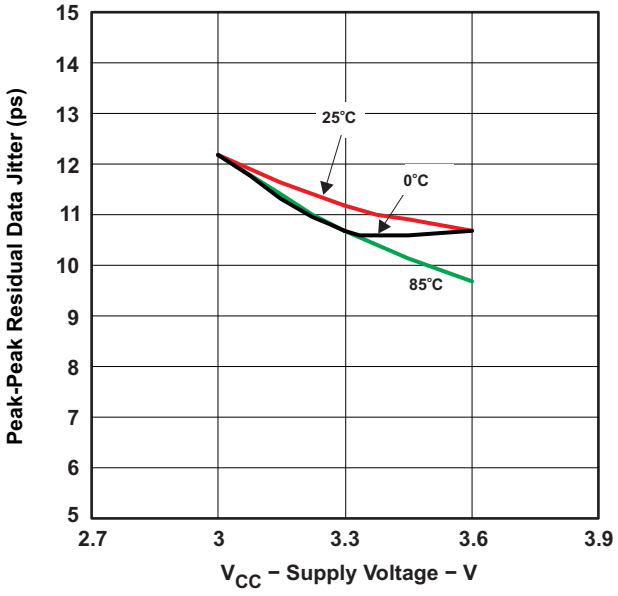


Figure 28.

TMDS PORT JITTER
vs
DATA RATE

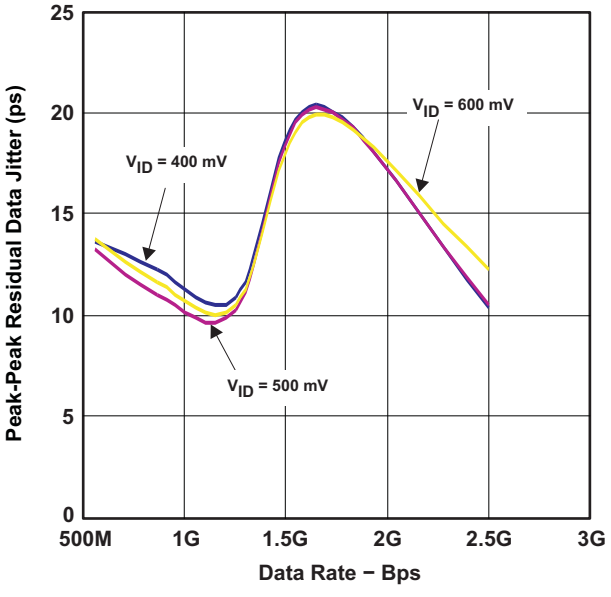


Figure 29.

TMDS OUTPUT DIFFERENTIAL VOLTAGE
vs
VSadj RESISTANCE

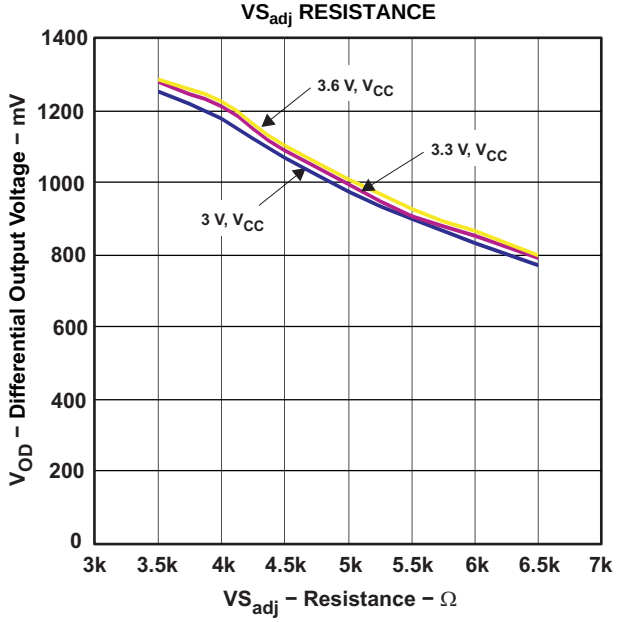


Figure 30.

APPLICATION INFORMATION

SWITCHING LOGIC

The Switching logic of the SN75DP122 is tied to the state of the HPD pins as well as the LP and priority pins. When both HPD_A and HPD_B input pins are LOW, the SN75DP122 enters the low power state. In this state the outputs are high impedance. When either HPD_A or HPD_B goes high, the device enters the normal operational state and the port associated with the HPD pin that went high is selected. If both HPD_A and HPD_B are HIGH, the port selection is determined by the state of the priority pin.

In order to ease the transitioning from one output port to the other output port the SN75DP122 forces the HPD output pin LOW for an extended duration. This forced Low is designed to mimic an unplug event for the transmitting device. This should allow for a smooth transition from one port to another. This forced LOW timer can be bypassed by pulsing the LP pin LOW for a short duration and then returning to HIGH. When the LP pin if driven LOW the device enters a low power state and the internal logic block is reset.

I²C INTERFACE NOTES

The I²C interface can be used to access the internal memory of the SN75DP122. I²C is a two-wire serial interface developed by Philips Semiconductor (see I²C-Bus Specification, Version 2.1, January 2000). The bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is *idle*, both SDA and SCL lines are pulled high. All the I²C compatible devices connect to the I²C bus through open drain I/O pins, SDA and SCL. A *master* device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A *slave* device receives and/or transmits data on the bus under control of the master device. The SN75DP122 works as a slave and supports the standard mode transfer (100 kbps) and fast mode transfer (400 kbps) as defined in the I²C-Bus Specification.

The basic I²C start and stop access cycles are shown in Figure 31.

The basic access cycle consists of the following:

- A start condition
- A slave address cycle
- Any number of data cycles
- A stop condition

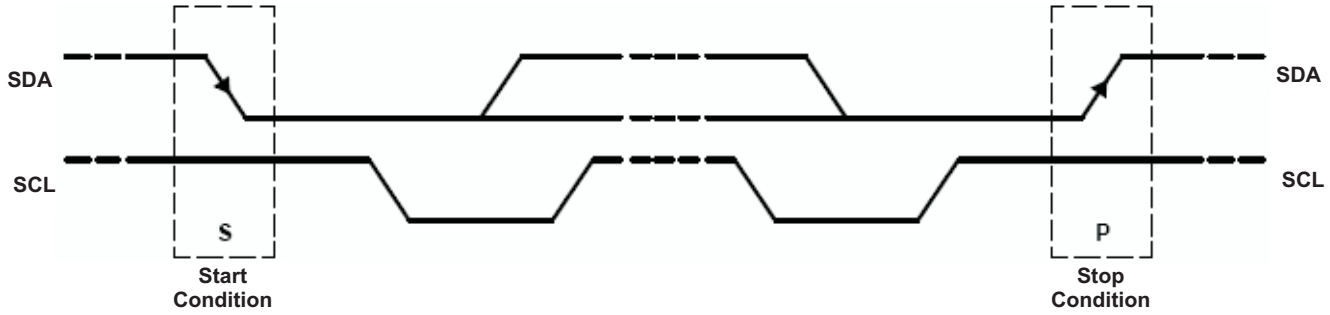


Figure 31. I²C Start and Stop Conditions

GENERAL I²C PROTOCOL

- The *master* initiates data transfer by generating a *start condition*. The *start condition* is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 31. All I²C-compatible devices should recognize a *start condition*.
- The master then generates the SCL pulses and transmits the 7-bit address and the *read/write direction bit* R/W on the SDA line. During all transmissions, the master ensures that data is *valid*. A *valid data* condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 32). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an *acknowledge* (see Figure 33) by pulling the SDA line low during the entire high period of the ninth SCL cycle. On detecting this acknowledge, the master knows that a

communication link with a slave has been established.

- The master generates further SCL cycles to either *transmit* data to the slave (R/W bit 0) or *receive* data from the slave (R/W bit 1). In either case, the *receiver* needs to acknowledge the data sent by the *transmitter*. So an acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. The 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary (see Figure 34).
- To signal the end of the data transfer, the master generates a *stop condition* by pulling the SDA line from low to high while the SCL line is high (see Figure 31). This releases the bus and stops the communication link with the addressed slave. All I^2C compatible devices must recognize the *stop condition*. Upon the receipt of a stop condition, all devices know that the bus is released, and they wait for a *start condition* followed by a matching address.

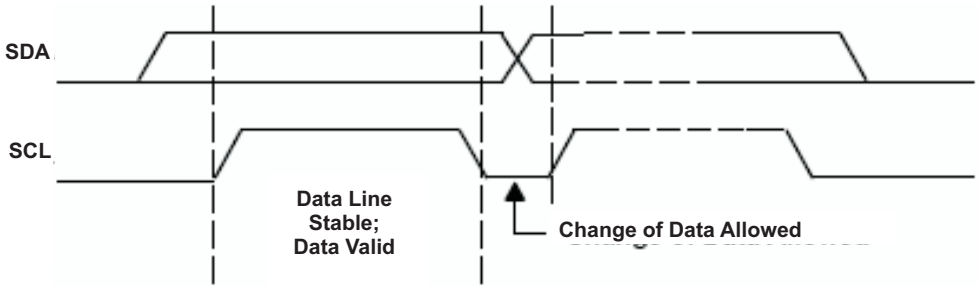


Figure 32. I^2C Bit Transfer

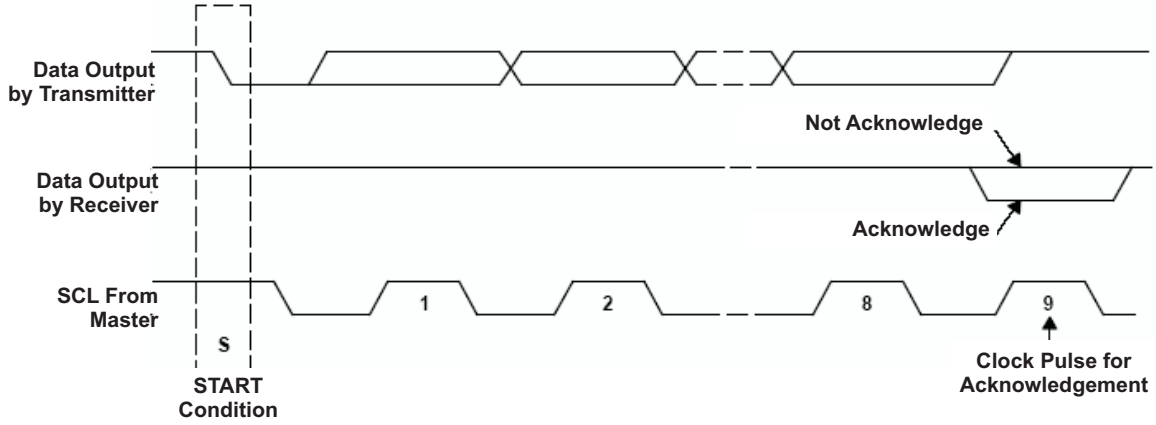


Figure 33. I^2C Acknowledge

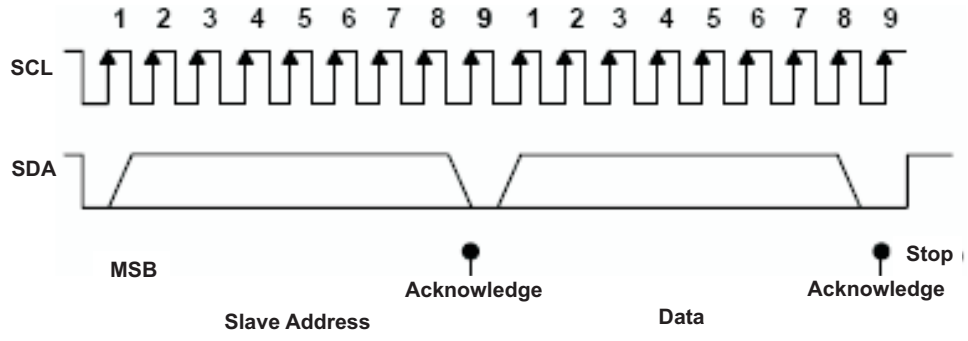


Figure 34. I^2C Address and Data Cycles

During a read cycle, the slave receiver acknowledges the initial address byte if it decodes the address as its

address. Following this initial acknowledge by the slave, the master device becomes a receiver and acknowledges data bytes sent by the slave. When the master has received all of the requested data bytes from the slave, the not acknowledge (A) condition is initiated by the master by keeping the SDA signal high just before it asserts the stop (P) condition. This sequence terminates a read cycle as shown in Figure 35 and Figure 36. See **Example – Reading from the SN75DP122** section for more information.

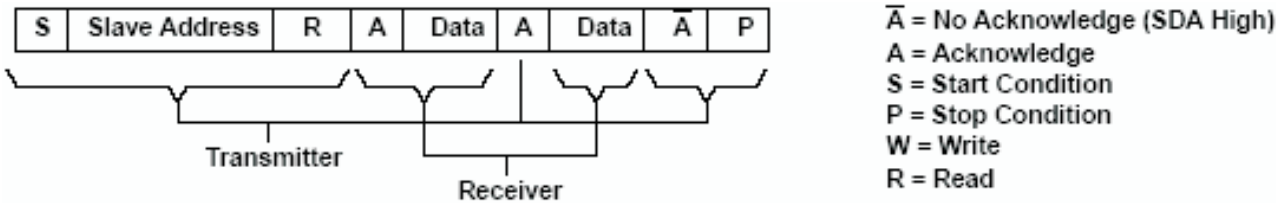


Figure 35. I²C Read Cycle

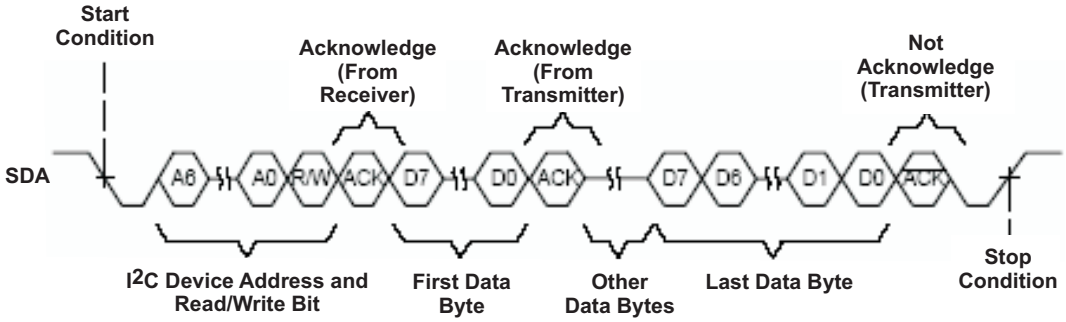


Figure 36. Multiple Byte Read Transfer

Slave Address

Both SDA and SCL must be connected to a positive supply voltage via a pull-up resistor. These resistors should comply with the I²C specification that ranges from 2 kΩ to 19 kΩ. When the bus is free, both lines are high. The address byte is the first byte received following the START condition from the master device. The 7-bit address is factory preset to 1000000. Table 2 lists the calls that the SN75DP122 responds to.

Table 2. SN75DP122 Slave Address

FIXED ADDRESS							READ/WRITE BIT
Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (R/W)
1	0	0	0	0	0	0	1

Sink Port Selection Register and Source Plug-In Status Register Description (Sub-Address)

The SN75DP122 operates using a multiple byte transfer protocol similar to Figure 36. The internal memory of the SN75DP122 contains the phrase *DP-HDMI ADAPTOR<EOT>* converted to ASCII characters. The internal memory address registers and the value of each can be found in Table 3.

During a read cycle, the SN75DP122 sends the data in its selected sub-address in a single transfer to the master device requesting the information. See the **Example – Reading from the SN75DP122** section of this document for the proper procedure on reading from the SN75DP122.

Table 3. SN75DP122 Sink Port and Source Plug-In Status Registers Selection

Address	0x00	0x01	0x02	0x03	0x04	0x05	0x06	0x07	0x08	0x09	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F	0x10
Data	44	50	2D	48	44	4D	49	20	41	44	41	50	54	4F	52	04	FF

EXAMPLE – READING FROM THE SN75DP122

The read operation consists of several steps. The I^2C master begins the communication with the transmission of the start sequence followed by the slave address of the SN75DP122. The SN75DP122 acknowledges its presence to the master and begin to transmit the contents of the memory registers. After each byte is transferred the SN75DP122 waits for either an acknowledge (ACK) or a not-acknowledge (NACK) from the master. If an ACK is received, the next byte of data is transmitted. If a NACK is received the data transmission sequence is expected to end and the master should send the stop command.

The SN75DP122 continues to send data as long as the master continues to acknowledge each byte transmission. If an ACK is received after the transmission of byte 0x0F, the SN75DP122 transmits byte 0x10 and continue to transmit byte 0x10 for all further ACK's until a NACK is received.

SN75DP122 Read Phase:

Step 1	0
I^2C Start (Master)	S

Step 2	7	6	5	4	3	2	1	0
I^2C General Address (Master)	1	0	0	0	0	0	0	1

Step 3	9
I^2C Acknowledge (Slave)	A

Step 10	7	6	5	4	3	2	1	0
I^2C Read Data (Slave)	Data	Data	Data	Data	Data	Data	Data	Data

Where Data is determined by the logic values contained in the Sink port register

Step 11	9
I^2C Not-Acknowledge (Master)	X

Where X is either an A (Acknowledge) or $\overline{A}$ (Not-Acknowledge)
An A causes the pointer to increment and step 10 is repeated
An $\overline{A}$ causes the slave to stop transmitting and proceed to step 12

Step 12	0
I^2C Stop (Master)	P

SWITCHING LOGIC

The switching logic of the SN75DP122 is tied to the state of the HPD input pins as well as the priority pin and low power pin. When both HPD_A and HPD_B input pins are LOW, the SN75DP122 enters the low power state. In this state the outputs are high impedance, and the device is shutdown to optimize power conservation. When either HPD_A or HPD_B goes high, the device enters the normal operational state, and the port associated with the HPD pin that went high is selected. If both HPD_A and HPD_B are HIGH, the port selection is determined by the state of the priority pin.

Several key factors were taken into consideration with this digital logic implementation of channel selection as well as HPD repeating. This logic has been divided into the following four scenarios.

1. Low power state to active state. There are two possible cases for this scenario depending on the state of the low power pin:
   - Case one: In this case both HPD inputs are initially LOW and the low power pin is also LOW. In this initial state the device is in a low power mode. Once one of the HPD inputs goes to a HIGH state, the device remains in the low power mode with both the main link and auxiliary I/O in a high impedance state. However, the port associated with the HPD input that went HIGH is still selected and the HPD output to the source is enabled and follows the logic state of the input HPD (see Figure 37). The state of the Priority pin has no effect in this scenario as only one HPD input port is active.

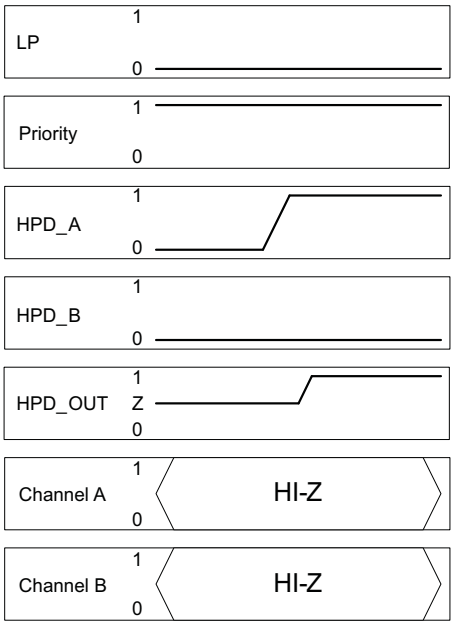


Figure 37.

– Case two: In this case both HPD inputs are initially LOW and the low power pin is HIGH. In this initial state the device is in a low power mode. Once one of the HPD inputs goes to a HIGH state, the device comes out of the low power mode and enters active mode enabling the main link and auxiliary I/O. The port associated with the HPD input that went HIGH is selected and the HPD output to the source is enabled and follows the logic state of the input HPD (see Figure 38). This is specified as $t_{Z(HPD)}$. Again, the state of the Priority pin has no effect in this scenario as only one HPD input port is active.

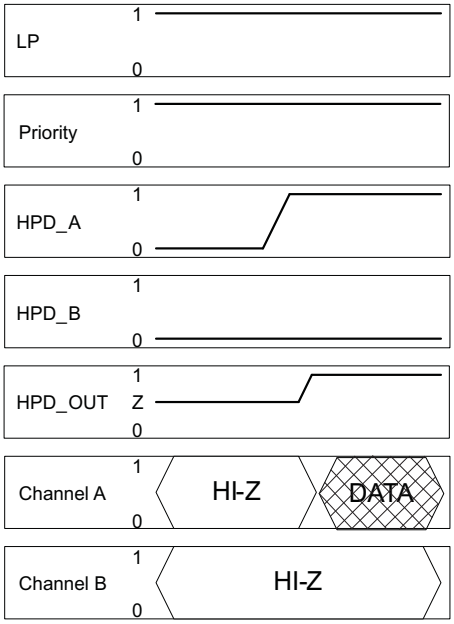


Figure 38.

2. HPD Changes on the selected port. There are also two possible starting cases for this scenario:
   – Case one: In this case only one HPD input is initially HIGH. The HPD output logic state follows the state of the HPD input. If the HPD input pulses LOW, as may be the case if the Sink device is requesting an interrupt, the HPD output to the source also pulses LOW for the same duration of time with a slight delay

(see Figure 39). The delay of this signal through the SN75DP122 is specified as $t_{PD(HPD)}$. If the duration of the LOW pulse is less then $t_{M(HPD)}$, it may not be accurately repeated to the source. If the duration of the LOW pulse exceeds $t_{T2(HPD)}$, the device assumes that an unplug event has occurred and enters the low power state (see Figure 40). Once the HPD input goes high again, the device returns to the active state as indicated in scenario 1. The state of the Priority pin has no effect in this scenario as only one HPD input port is active.

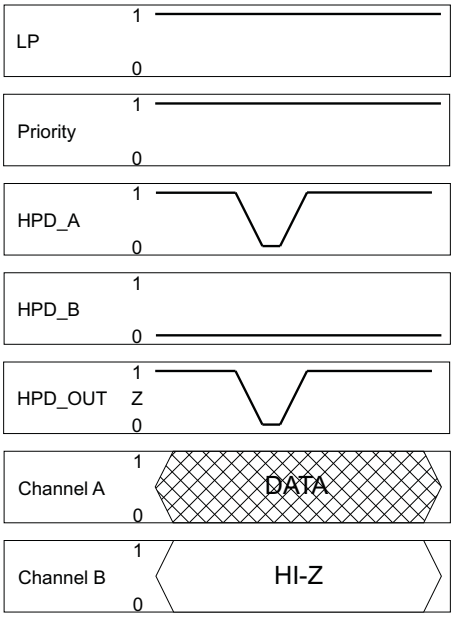


Figure 39.

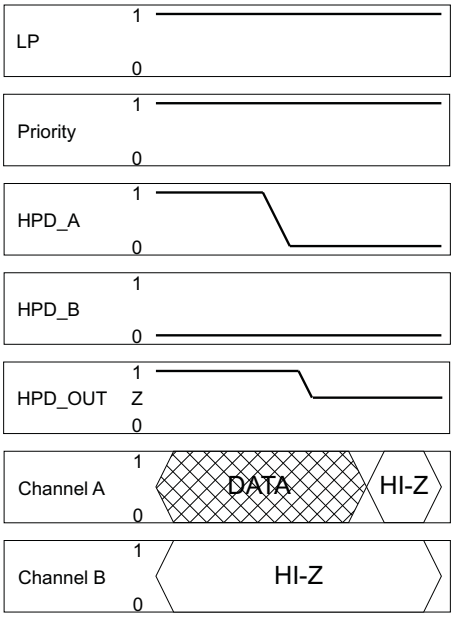


Figure 40.

– Case two: In this case both HPD inputs are initially HIGH and the selected port has been determined by the state of the priority pin. The HPD output logic state follows the state of the selected HPD input. If the HPD input pulses LOW, the HPD output to the source also pulses LOW for the same duration of time, again with a slight delay (see Figure 41). If the duration of the LOW pulse exceeds $t_{T2(HPD)}$, the device assumes that an unplug event has occurred and the other port is selected (see Figure 42). The case in

which the previously selected port with priority goes high again is covered in scenario 3.

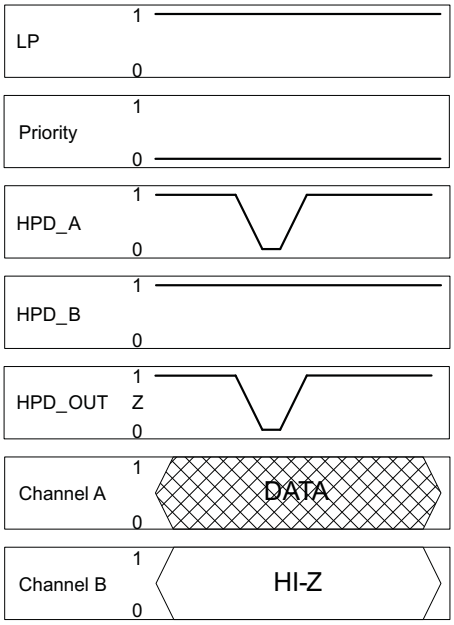


Figure 41.

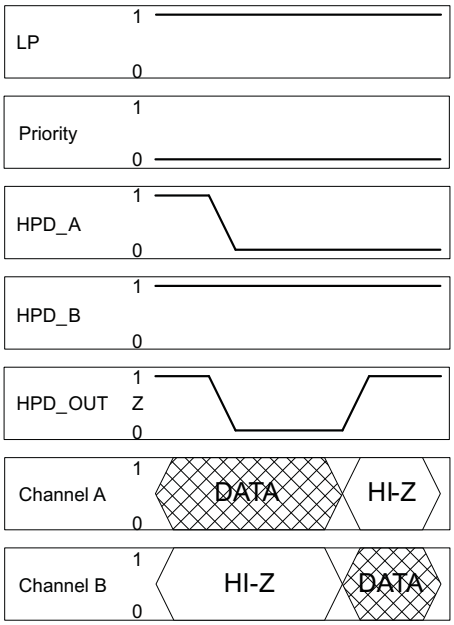


Figure 42.

3. One channel becomes active while other channel is already selected. There are also two possible starting cases for this scenario:
   – Case one: In this case the HPD input that is initially HIGH is from the port that has priority. Since the port with priority is already selected, any activity on the HPD input from the other port does not have any effect on the switch whatsoever (see Figure 43).

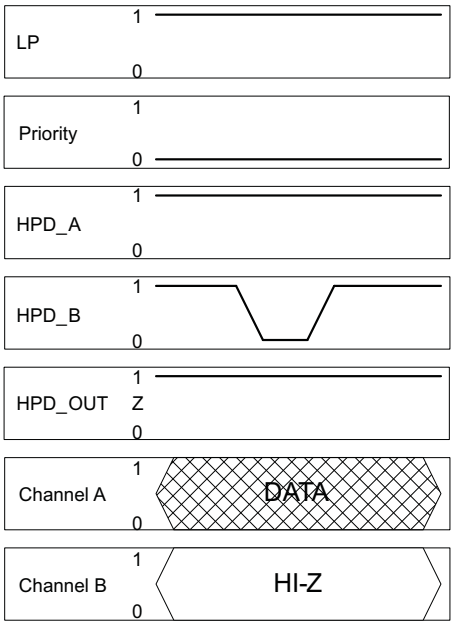


Figure 43.

– Case two: In this case the HPD input that is initially HIGH is not the port with priority. When the HPD input of the port that has priority goes high, the HPD output is forced LOW for some time in order to simulate an unplug event to the source device. The duration of this LOW output is defined as $t_{T2(HPD)}$. If the HPD input of the port with priority pulses LOW for a short duration while the $t_{T2(HPD)}$ timer is counting down, the timer is reset. Once this time has passed the switch switches to the port with priority and the output HPD once again follows the state of the newly selected channel's HPD input (see Figure 44).

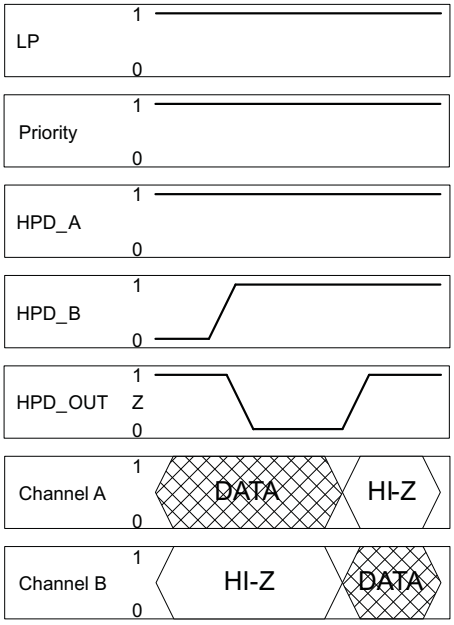


Figure 44.

4. 4. Priority pin is toggled. There are also two possible starting cases for this scenario:
   – Case one: In this case only one HPD input is HIGH. A port whose HPD input is LOW cannot be selected. In this case, the state of the priority pin has no effect on the switch (see Figure 45).

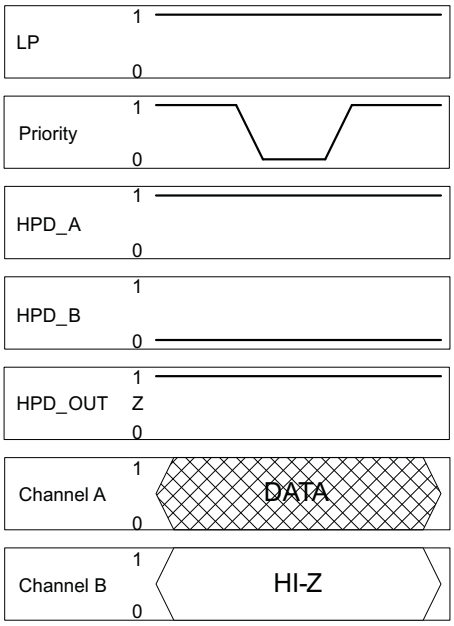


Figure 45.

– Case two: In this case both HPD inputs are HIGH. Changing the state of the priority pin when both HPD inputs are high forces the device to switch which channel is selected. When a state change is detected on the priority pin, the device waits for a short period of time $t_{T1(HPD)}$ before responding (see Figure 46). The purpose for this pause is to allow for the priority signal to settle and also to allow the device to ignore potential glitches on the priority pin. Once $t_{T1(HPD)}$ has expired, the HPD output is forced LOW for $t_{T2(HPD)}$ and the device follows the chain of events outlined in scenario 3 case 2.

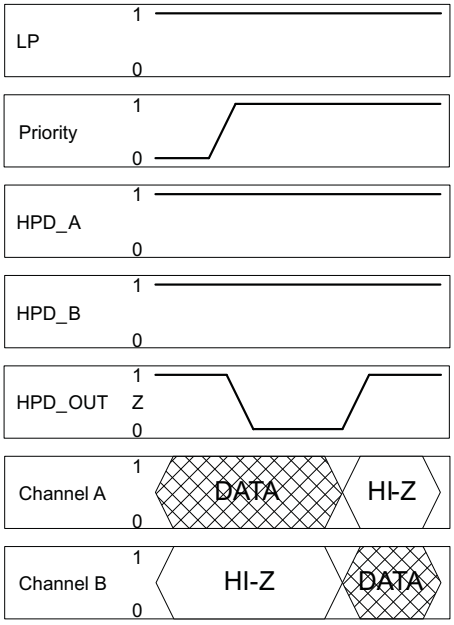


Figure 46.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN75DP122RTQR	NRND	QFN	RTQ	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 85	75DP122	
SN75DP122RTQRG4	NRND	QFN	RTQ	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 85	75DP122	
SN75DP122RTQT	NRND	QFN	RTQ	56	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 85	75DP122	
SN75DP122RTQTG4	NRND	QFN	RTQ	56	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	0 to 85	75DP122	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

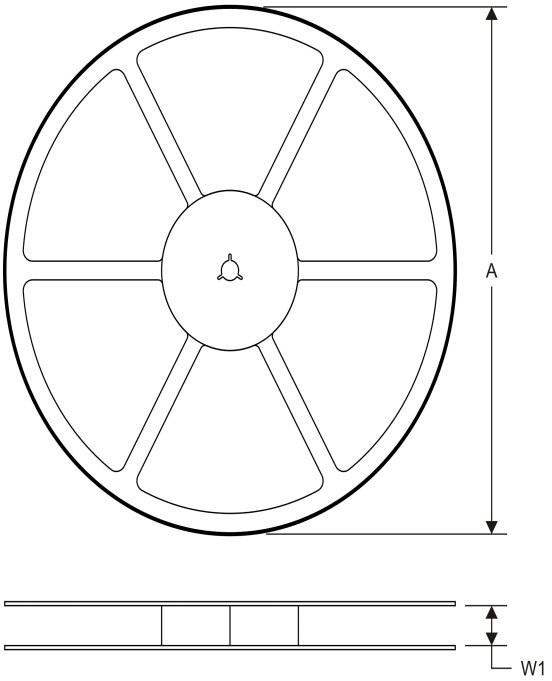
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

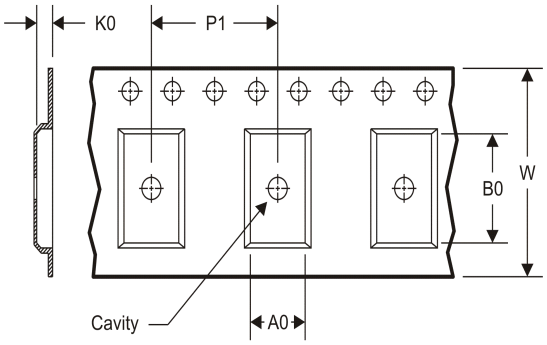
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



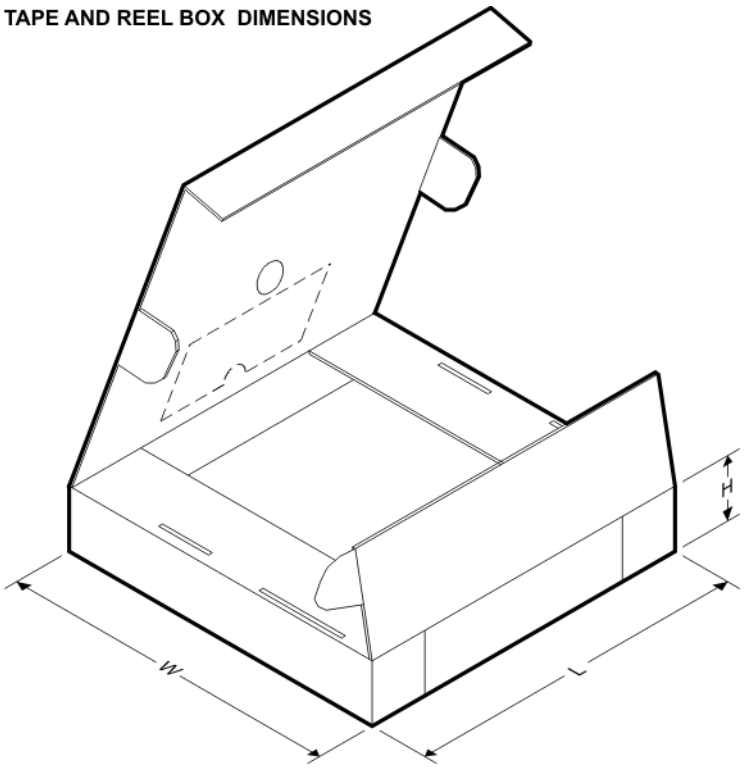
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75DP122RTQR	QFN	RTQ	56	2000	330.0	16.4	8.3	8.3	2.25	12.0	16.0	Q2
SN75DP122RTQT	QFN	RTQ	56	250	180.0	16.4	8.3	8.3	2.25	12.0	16.0	Q2

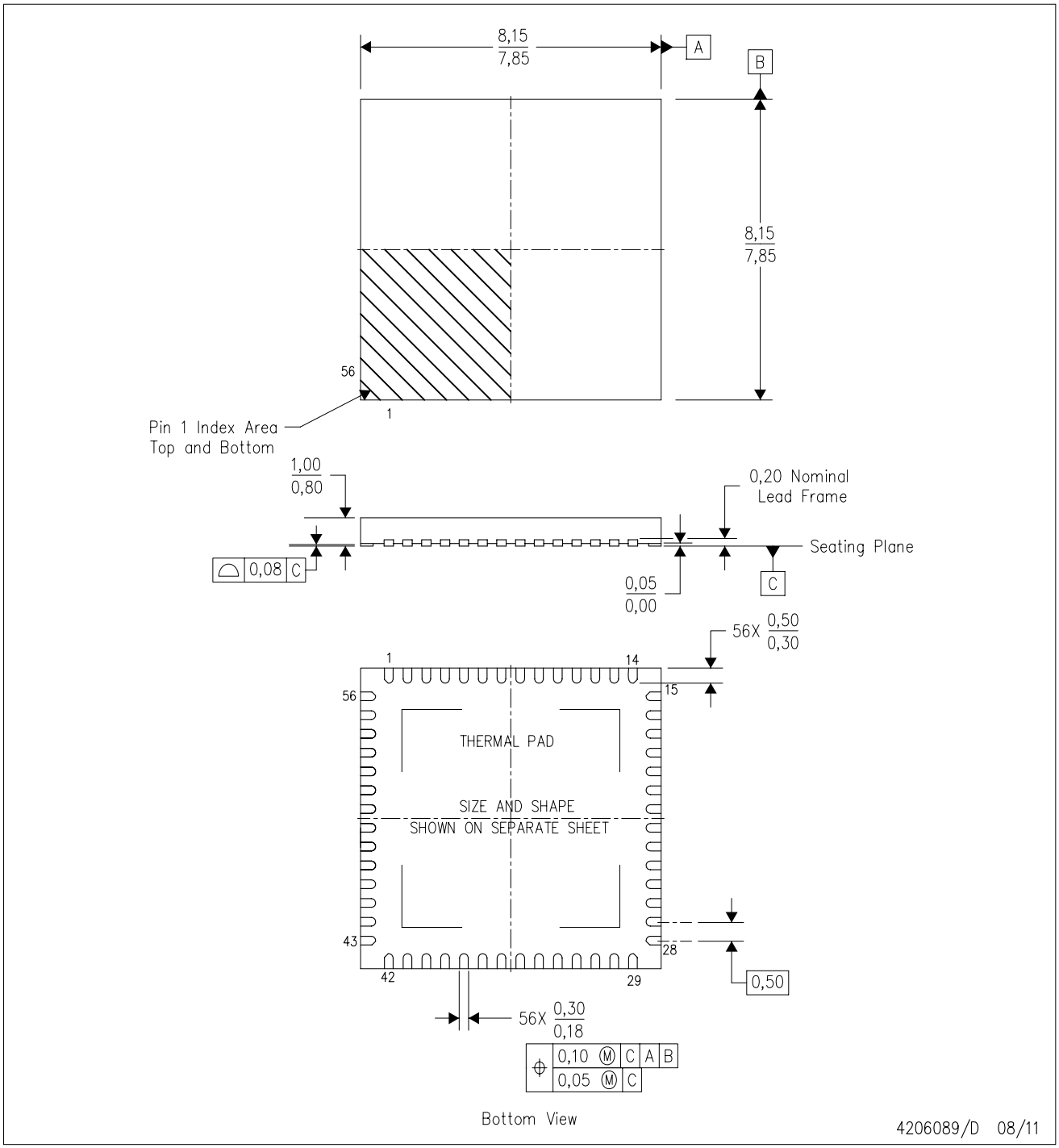
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75DP122RTQR	QFN	RTQ	56	2000	367.0	367.0	38.0
SN75DP122RTQT	QFN	RTQ	56	250	210.0	185.0	35.0

RTQ (S–PVQFN–N56) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Package complies to JEDEC MO–220.

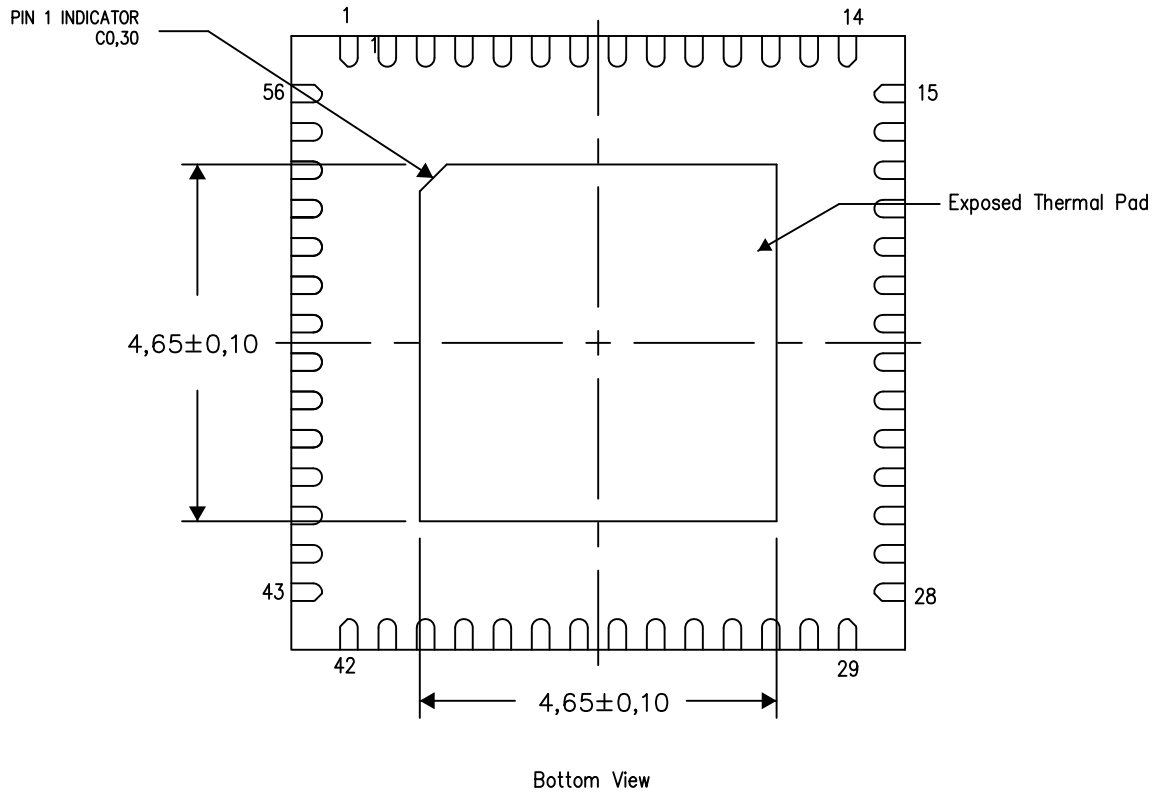
RTQ (S–PVQFN–N56) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



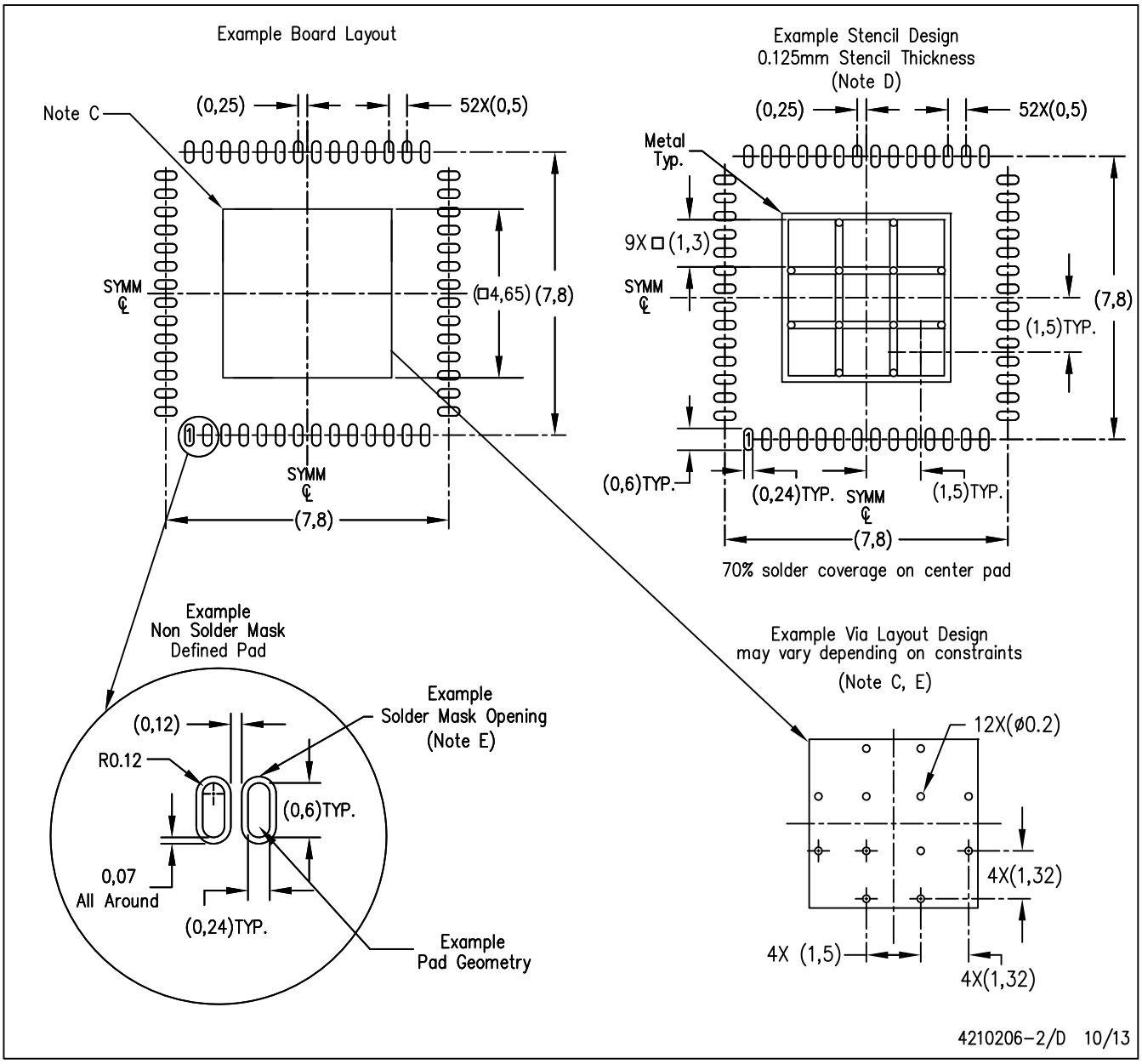
Bottom View

Exposed Thermal Pad Dimensions

4206252–4/P 10/13

NOTE: All linear dimensions are in millimeters

RTQ (S–PVQFN–N56) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

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