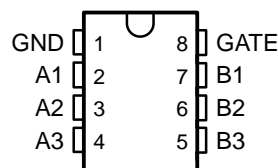


FEATURES

- Designed to Be Used in Voltage-Limiting Applications
- 3.5-Ω On-State Connection Between Ports A and B
- Flow-Through Pinout for Ease of Printed Circuit Board Trace Routing
- Direct Interface With GTL+ Levels
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DCT OR DCU PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The SN74TVC3306 provides three parallel NMOS pass transistors with a common unbuffered gate. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

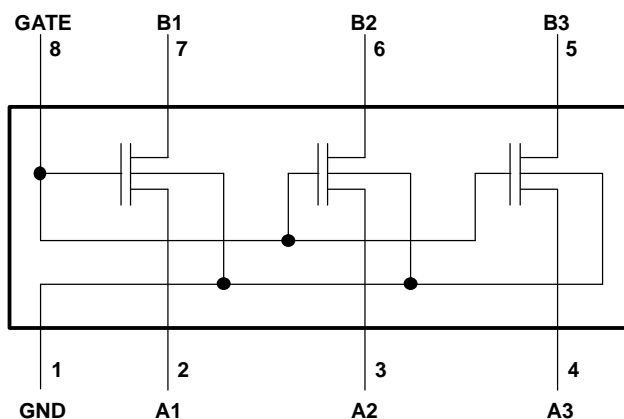
The device can be used as a dual switch, with the gates cascaded together to a reference transistor. The low-voltage side of each pass transistor is limited to a voltage set by the reference transistor. This is done to protect components with inputs that are sensitive to high-state voltage-level overshoots.

ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SSOP – DCT	Tape and reel	SN74TVC3306DCTR	FA6
	VSSOP – DCU	Tape and reel	SN74TVC3306DCUR	FA6

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

LOGIC DIAGRAM (POSITIVE LOGIC)



NOTE A: The SN74TVC3306 has bidirectional capability across many voltage levels. The voltage levels documented in this data sheet are examples.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SN74TVC3306

DUAL VOLTAGE CLAMP

SCDS112C—MARCH 2001—REVISED MARCH 2005

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_I	Input voltage range ⁽²⁾	−0.5	7	V
$V_{I/O}$	Input/output voltage range ⁽²⁾	−0.5	7	V
	Continuous channel current		128	mA
I_{IK}	Input clamp current	$V_I < 0$	−50	mA
θ_{JA}	Package thermal impedance ⁽³⁾	DCT package	220	°C/W
		DCU package	227	
T_{stg}	Storage temperature range	−65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and input/output negative-voltage ratings may be exceeded if the input and input/output clamp-current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions

		MIN	MAX	UNIT
V _{I/O}	Input/output voltage	0	5	V
V _{GATE}	GATE voltage	0	5	V
I _{PASS}	Pass transistor current		64	mA
T _A	Operating free-air temperature	−40	85	°C

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
V_{IK}	$I_I = -18$ mA,	$V_{GATE} = 0$			−1.2	V
I_{IH}	$V_I = 5$ V,	$V_{GATE} = 0$			5	μA
$C_{i(GATE)}$	$V_I = 3$ V or 0			11		pF
$C_{io(off)}$	$V_O = 3$ V or 0,	$V_{GATE} = 0$		4	6	pF
$C_{io(on)}$	$V_O = 3$ V or 0,	$V_{GATE} = 3$ V		10.5	12.5	pF
r_{on} ⁽²⁾	$V_I = 0,$	$I_O = 64$ mA	$V_{GATE} = 4.5$ V	3.5	5.5	Ω
			$V_{GATE} = 3$ V	4.7	7	
			$V_{GATE} = 2.3$ V	6.3	9.5	
			$V_{GATE} = 1.5$ V	25.5	32	
	$V_I = 2.4$ V,	$I_O = 15$ mA	$V_{GATE} = 4.5$ V	4.8	7.5	
			$V_{GATE} = 3$ V	14.7	23	
	$V_I = 1.7$ V,	$I_O = 15$ mA	$V_{GATE} = 2.3$ V	11.3	16.5	

- (1) All typical values are at $T_A = 25^\circ\text{C}$.
- (2) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

AC Performance (Translating Down)

Switching Characteristics

over recommended operating free-air temperature range, $V_{GATE} = 3.3\text{ V}$, $V_{IH} = 3.3\text{ V}$, $V_{IL} = 0$, and $V_M = 1.15\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$C_L = 50\text{ pF}$		$C_L = 30\text{ pF}$		$C_L = 15\text{ pF}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	0	0.8	0	0.6	0	0.3	ns
t_{PHL}			0	1.2	0	1	0	0.5	

Switching Characteristics

over recommended operating free-air temperature range, $V_{GATE} = 2.5\text{ V}$, $V_{IH} = 2.5\text{ V}$, $V_{IL} = 0$, and $V_M = 0.75\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$C_L = 50\text{ pF}$		$C_L = 30\text{ pF}$		$C_L = 15\text{ pF}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	0	1	0	0.7	0	0.4	ns
t_{PHL}			0	1.3	0	1	0	0.6	

AC Performance (Translating Up)

Switching Characteristics

over recommended operating free-air temperature range, $V_{GATE} = 3.3\text{ V}$, $V_{IH} = 2.3\text{ V}$, $V_{IL} = 0$, $V_T = 3.3\text{ V}$, $V_M = 1.15\text{ V}$, and $R_L = 300\text{ }\Omega$ (unless otherwise noted) (see Figure 1)

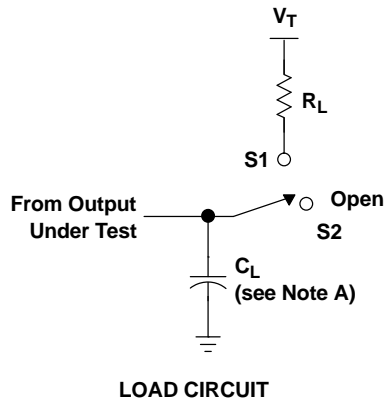
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$C_L = 50\text{ pF}$		$C_L = 30\text{ pF}$		$C_L = 15\text{ pF}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	0	0.9	0	0.6	0	0.4	ns
t_{PHL}			0	1.4	0	1.1	0	0.7	

Switching Characteristics

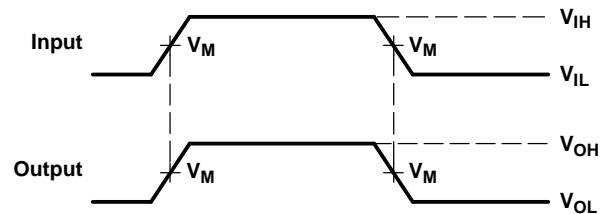
over recommended operating free-air temperature range, $V_{GATE} = 2.5\text{ V}$, $V_{IH} = 1.5\text{ V}$, $V_{IL} = 0$, $V_T = 2.5\text{ V}$, $V_M = 0.75\text{ V}$, and $R_L = 300\text{ }\Omega$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$C_L = 50\text{ pF}$		$C_L = 30\text{ pF}$		$C_L = 15\text{ pF}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	0	1	0	0.6	0	0.4	ns
t_{PHL}			0	1.3	0	1.3	0	0.8	

PARAMETER MEASUREMENT INFORMATION



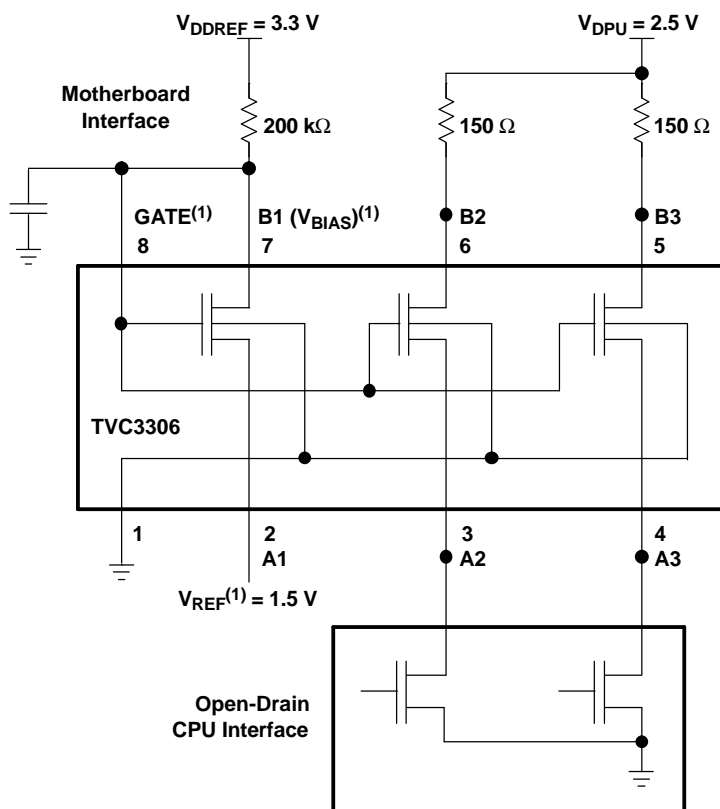
USAGE	SWITCH
Translating up	S1
Translating down	S2



- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2$ ns, $t_f \leq 2$ ns.
 C. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuit for Outputs

APPLICATION INFORMATION



(1) V_{REF} and V_{BIAS} can be applied to any one of the pass transistors. GATE must be connected externally to V_{BIAS} .

Figure 2. Typical Application Circuit

For the clamping configuration, the common GATE input must be connected to one side (An or Bn) of any one of the pass transistors, making that the V_{BIAS} connection of the reference transistor and the opposite side (Bn or An) the V_{REF} connection. When V_{BIAS} is connected through a 200-kΩ resistor to a 3-V to 5.5-V V_{CC} supply and V_{REF} is set to 0 V to $V_{CC} - 0.6$ V, the output of each switch has a maximum clamp voltage equal to V_{REF} . A filter capacitor on V_{BIAS} is recommended.

Application Operating Conditions

see Figure 2

		MIN	TYP ⁽¹⁾	MAX	UNIT
V_{BIAS}	BIAS voltage	$V_{REF} + 0.6$	2.1	5	V
V_{GATE}	GATE voltage	$V_{REF} + 0.6$	2.1	5	V
V_{REF}	Reference voltage	0	1.5	4.4	V
V_{DPU}	Drain pullup voltage	2.36	2.5	2.64	V
I_{PASS}	Pass-transistor current		14		mA
I_{REF}	Reference-transistor current		5		μA
T_A	Operating free-air temperature	-40		85	°C

(1) All typical values are at $T_A = 25^\circ\text{C}$.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74TVC3306DCTR	ACTIVE	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FA6 Y	Samples
SN74TVC3306DCTRE4	ACTIVE	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FA6 Y	Samples
SN74TVC3306DCTRG4	ACTIVE	SM8	DCT	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	FA6 Y	Samples
SN74TVC3306DCUR	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-40 to 85	(FA6P ~ FA6S)	Samples
SN74TVC3306DCURE4	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(FA6P ~ FA6S)	Samples
SN74TVC3306DCURG4	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(FA6P ~ FA6S)	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74TVC3306DCUR	US8	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3

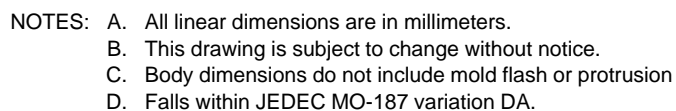
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

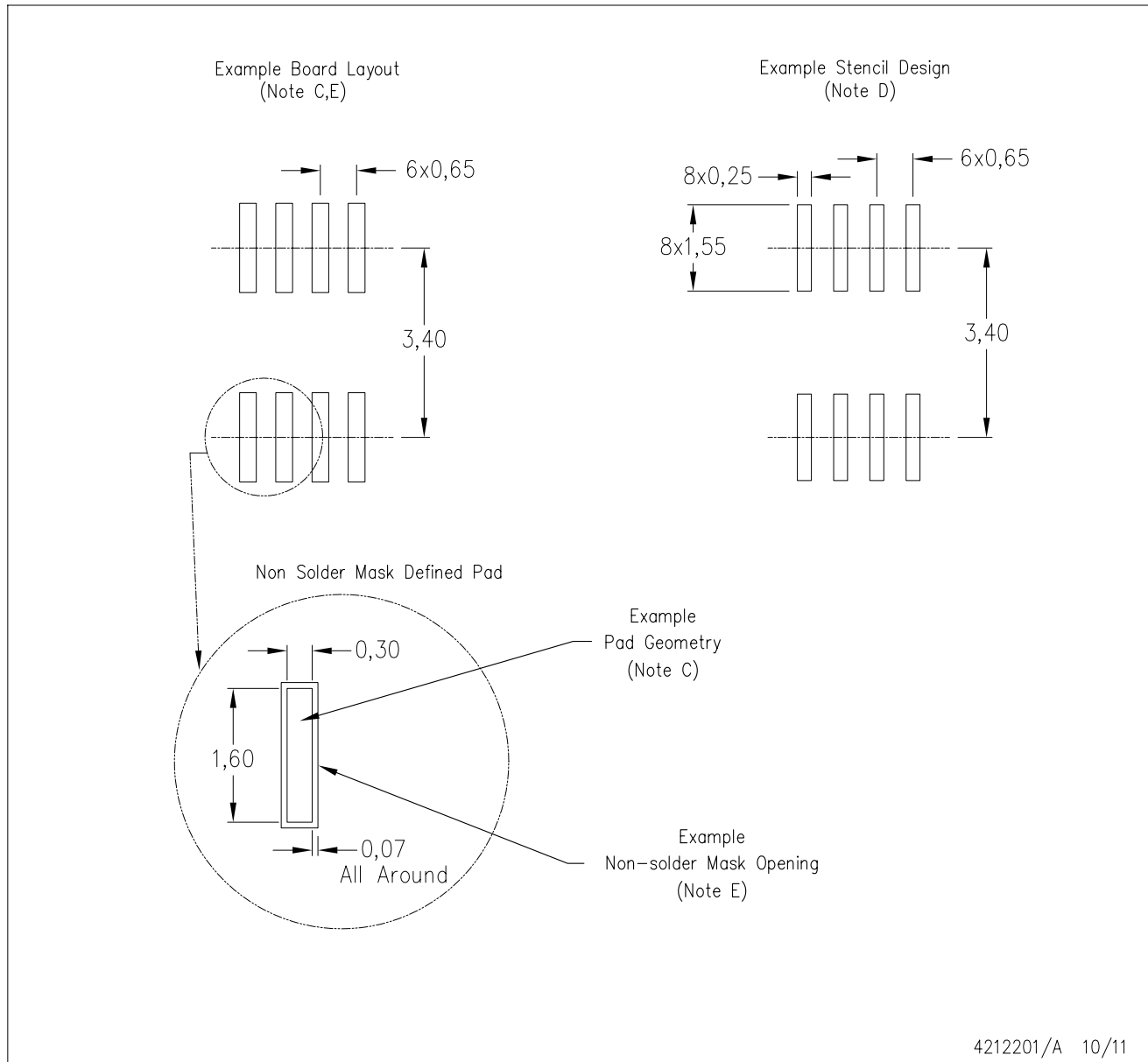
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74TVC3306DCUR	US8	DCU	8	3000	202.0	201.0	28.0

PLASTIC SMALL-OUTLINE PACKAGE



DCT (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DCU (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- Falls within JEDEC MO-187 variation CA.

DCU (S-PDSO-G8)

PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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