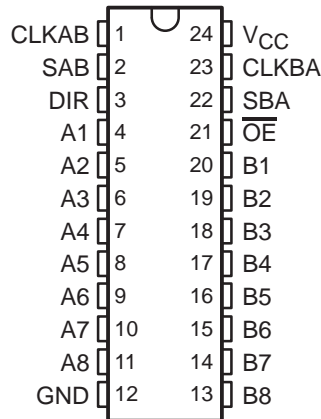


SN54LVTH646, SN74LVTH646 3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

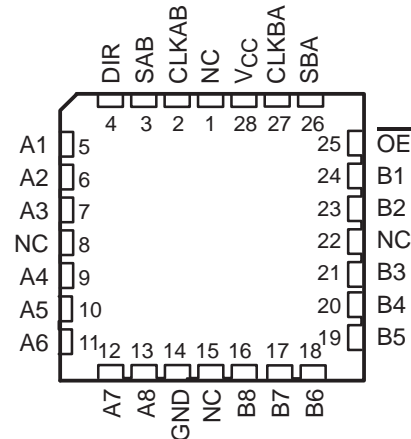
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- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- I_{off} and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

SN54LVTH646 . . . JT OR W PACKAGE
SN74LVTH646 . . . DB, DGV, DW, NS, OR PW PACKAGE
(TOP VIEW)



SN54LVTH646 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

These bus transceivers and registers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

ORDERING INFORMATION

| T_A | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|-------------|---------------|-----------------------|------------------|
| –40°C to 85°C | SOIC – DW | Tube | SN74LVTH646DW | LVTH646 |
| | | Tape and reel | SN74LVTH646DWR | |
| | SOP – NS | Tape and reel | SN74LVTH646NSR | LVTH646 |
| | SSOP – DB | Tape and reel | SN74LVTH646DBR | LXH646 |
| | TSSOP – PW | Tube | SN74LVTH646PW | LXH646 |
| | | Tape and reel | SN74LVTH646PWR | |
| –55°C to 125°C | TVSOP – DGV | Tape and reel | SN74LVTH646DGV | LXH646 |
| | CDIP – JT | Tube | SNJ54LVTH646JT | SNJ54LVTH646JT |
| | CFP – W | Tube | SNJ54LVTH646W | SNJ54LVTH646W |
| | LCCC – FK | Tube | SNJ54LVTH646FK | SNJ54LVTH646FK |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCBS705H – AUGUST 1997 – REVISED MAY 2004

description/ordering information (continued)

The 'LVTH646 devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'LVTH646.

Output-enable (\overline{OE}) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port can be stored in either register or in both.

The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The direction control (DIR) determines which bus receives data when \overline{OE} is low. In the isolation mode (\overline{OE} high), A data can be stored in one register and/or B data can be stored in the other register.

When an output function is disabled, the input function still is enabled and can be used to store and transmit data. Only one of the two buses, A or B, can be driven at a time.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

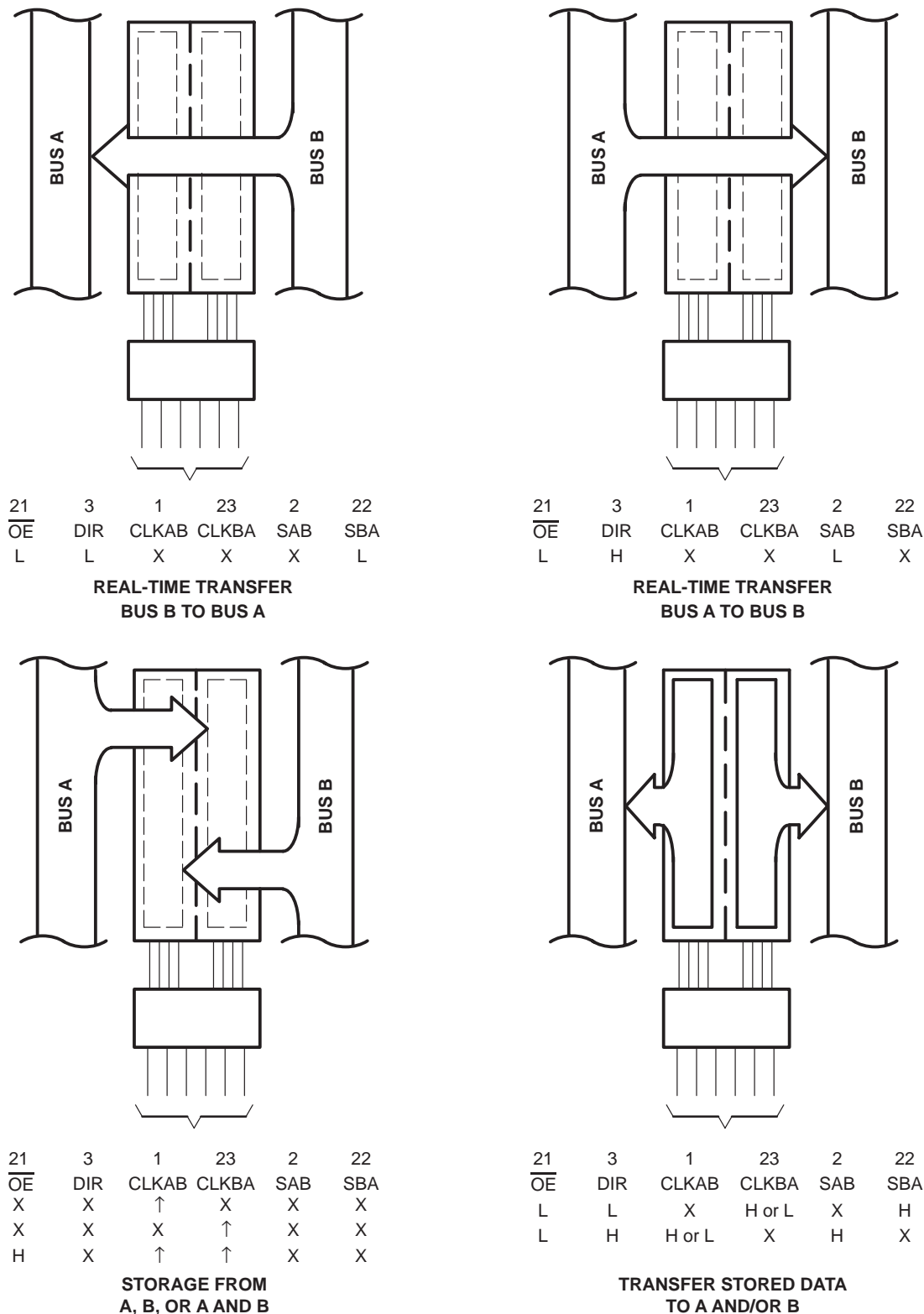
FUNCTION TABLE

| INPUTS | | | | | | DATA I/Os | | OPERATION OR FUNCTION |
|-----------------|-----|--------|--------|-----|-----|----------------|----------------|---------------------------|
| \overline{OE} | DIR | CLKAB | CLKBA | SAB | SBA | A1–A8 | B1–B8 | |
| X | X | ↑ | X | X | X | Input | Unspecified† | Store A, B unspecified† |
| X | X | X | ↑ | X | X | Unspecified† | Input | Store B, A unspecified† |
| H | X | ↑ | ↑ | X | X | Input | Input | Store A and B data |
| H | X | H or L | H or L | X | X | Input disabled | Input disabled | Isolation, hold storage |
| L | L | X | X | X | L | Output | Input | Real-time B data to A bus |
| L | L | X | H or L | X | H | Output | Input | Stored B data to A bus |
| L | H | X | X | L | X | Input | Output | Real-time A data to B bus |
| L | H | H or L | X | H | X | Input | Output | Stored A data to B bus |

† The data-output functions can be enabled or disabled by various signals at \overline{OE} and DIR. Data-input functions always are enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

SN54LVTH646, SN74LVTH646 **3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS** **WITH 3-STATE OUTPUTS**

SCBS705H – AUGUST 1997 – REVISED MAY 2004



Pin numbers shown are for the DB, DGV, DW, JT, NS, PW, and W packages.

Figure 1. Bus-Management Functions

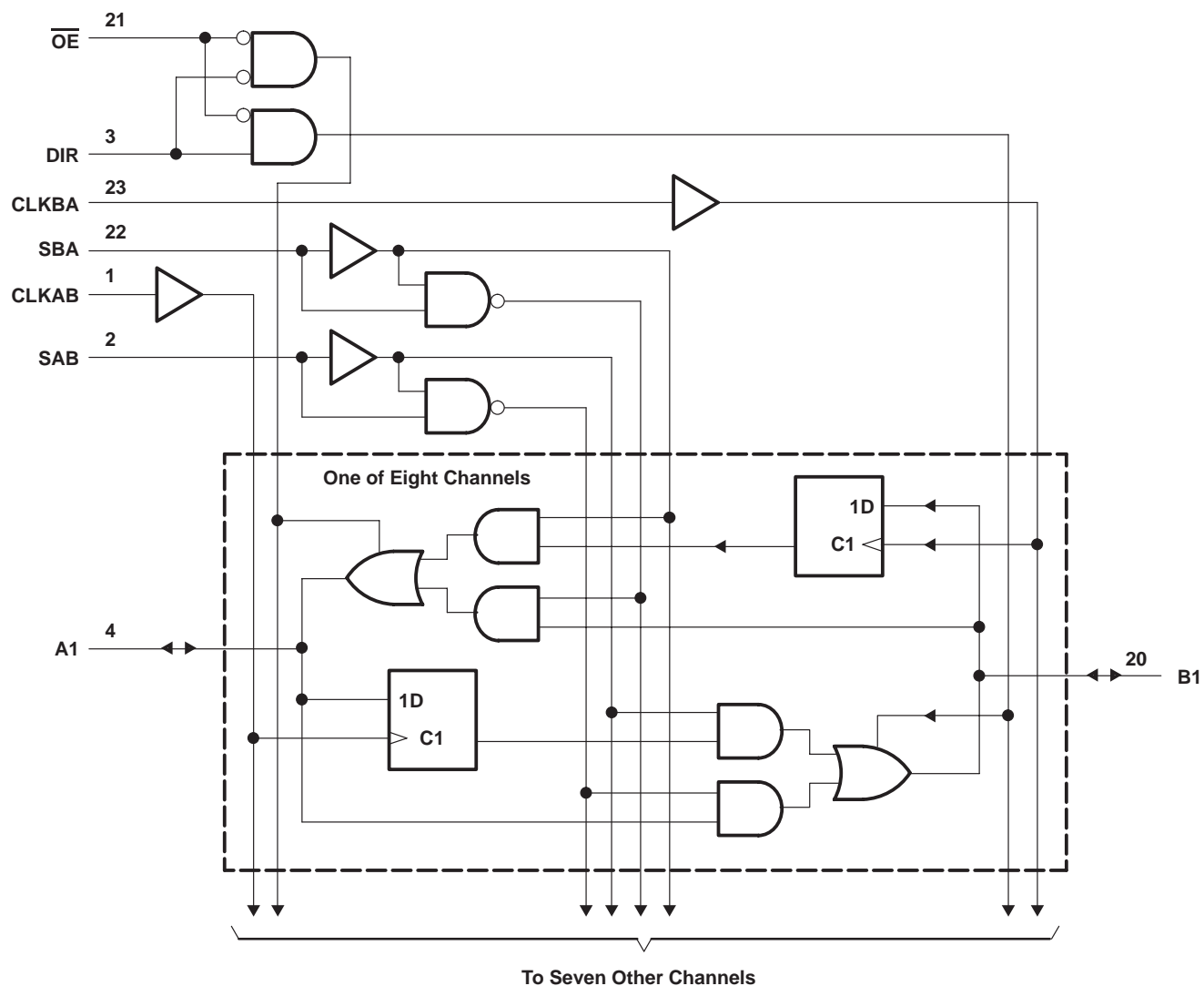
SN54LVTH646, SN74LVTH646

3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS

WITH 3-STATE OUTPUTS

SCBS705H – AUGUST 1997 – REVISED MAY 2004

logic diagram (positive logic)



Pin numbers shown are for the DB, DGV, DW, JT, NS, PW, and W packages.

SCBS705H – AUGUST 1997 – REVISED MAY 2004

| | | |
|---|-------|----------------------------|
| Supply voltage range, V_{CC} | | –0.5 V to 4.6 V |
| Input voltage range, V_I (see Note 1) | | –0.5 V to 7 V |
| Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1) | | –0.5 V to 7 V |
| Voltage range applied to any output in the high state, V_O (see Note 1) | | –0.5 V to $V_{CC} + 0.5$ V |
| Current into any output in the low state, I_O : SN54LVTH646 | | 96 mA |
| SN74LVTH646 | | 128 mA |
| Current into any output in the high state, I_O (see Note 2): SN54LVTH646 | | 48 mA |
| SN74LVTH646 | | 64 mA |
| Input clamp current, I_{IK} ($V_I < 0$) | | –50 mA |
| Output clamp current, I_{OK} ($V_O < 0$) | | –50 mA |
| Package thermal impedance, θ_{JA} (see Note 3): DB package | | 63°C/W |
| DGV package | | 86°C/W |
| DW package | | 46°C/W |
| NS package | | 65°C/W |
| PW package | | 88°C/W |
| Storage temperature range, T_{sta} | | –65°C to 150°C |

NOTES:

1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JEDEC 51-7.

| | | | SN54LVTH646 | | SN74LVTH646 | | UNIT |
|---------------------|------------------------------------|-----------------|-------------|-----|-------------|-----|------|
| | | | MIN | MAX | MIN | MAX | |
| V _{CC} | Supply voltage | | 2.7 | 3.6 | 2.7 | 3.6 | V |
| V _{IH} | High-level input voltage | | 2 | | 2 | | V |
| V _{IL} | Low-level input voltage | | 0.8 | | 0.8 | | V |
| V _I | Input voltage | | 5.5 | | 5.5 | | V |
| I _{OH} | High-level output current | | −24 | | −32 | | mA |
| I _{OL} | Low-level output current | | 48 | | 64 | | mA |
| Δt/Δv | Input transition rise or fall rate | Outputs enabled | 10 | | 10 | | ns/V |
| Δt/ΔV _{CC} | Power-up ramp rate | | 200 | | 200 | | μs/V |
| T _A | Operating free-air temperature | | −55 | 125 | −40 | 85 | °C |



**TEXAS
INSTRUMENTS**

SN54LVTH646, SN74LVTH646

3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCBS705H – AUGUST 1997 – REVISED MAY 2004

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | SN54LVTH646 | | | SN74LVTH646 | | | UNIT | |
|----------------------|----------------|--|----------------------------------|----------------------|------|-----|----------------------|------|-----|------|----|
| | | | | MIN | TYP† | MAX | MIN | TYP† | MAX | | |
| V _{IK} | | V _{CC} = 2.7 V, I _I = −18 mA | | −1.2 | | | −1.2 | | | V | |
| V _{OH} | | V _{CC} = 2.7 V to 3.6 V, I _{OH} = −100 μA | | V _{CC} −0.2 | | | V _{CC} −0.2 | | | V | |
| | | V _{CC} = 2.7 V, I _{OH} = −8 mA | | 2.4 | | | 2.4 | | | | |
| | | V _{CC} = 3 V | I _{OH} = −24 mA | 2 | | | | | | | |
| | | | I _{OH} = −32 mA | | | | 2 | | | | |
| V _{OL} | | V _{CC} = 2.7 V | I _{OL} = 100 μA | 0.2 | | | 0.2 | | | V | |
| | | | I _{OL} = 24 mA | 0.5 | | | 0.5 | | | | |
| | | V _{CC} = 3 V | I _{OL} = 16 mA | 0.4 | | | 0.4 | | | | |
| | | | I _{OL} = 32 mA | 0.5 | | | 0.5 | | | | |
| | | | I _{OL} = 48 mA | 0.55 | | | | | | | |
| | | | I _{OL} = 64 mA | | | | 0.55 | | | | |
| I _I | Control inputs | V _{CC} = 3.6 V, V _I = V _{CC} or GND | | ±1 | | | ±1 | | | μA | |
| | | V _{CC} = 0 or 3.6 V, V _I = 5.5 V | | 10 | | | 10 | | | | |
| | A or B ports‡ | V _{CC} = 3.6 V | V _I = 5.5 V | 20 | | | 20 | | | | |
| | | | V _I = V _{CC} | 1 | | | 1 | | | | |
| | | | V _I = 0 | −5 | | | −5 | | | | |
| I _{off} | | V _{CC} = 0, V _I or V _O = 0 to 4.5 V | | | | | ±100 | | | μA | |
| I _{I(hold)} | A or B ports | V _{CC} = 3 V | V _I = 0.8 V | 75 | | | 75 | | | μA | |
| | | | V _I = 2 V | −75 | | | −75 | | | | |
| | | V _{CC} = 3.6 V§, V _I = 0 to 3.6 V | | | | | ±500 | | | | |
| I _{OZPU} | | V _{CC} = 0 to 1.5 V, V _O = 0.5 V to 3 V, OE = don't care | | ±100 | | | ±100 | | | μA | |
| I _{OZPD} | | V _{CC} = 1.5 V to 0, V _O = 0.5 V to 3 V, OE = don't care | | ±100 | | | ±100 | | | μA | |
| I _{CC} | | V _{CC} = 3.6 V, I _O = 0, V _I = V _{CC} or GND | Outputs high | | 0.19 | | | 0.19 | | | mA |
| | | | Outputs low | | 5 | | | 5 | | | |
| | | | Outputs disabled | | 0.19 | | | 0.19 | | | |
| ΔI _{CC} ¶ | | V _{CC} = 3 V to 3.6 V, One input at V _{CC} − 0.6 V, Other inputs at V _{CC} or GND | | 0.2 | | | 0.2 | | | mA | |
| C _i | | V _I = 3 V or 0 | | 4 | | | 4 | | | pF | |
| C _{io} | | V _O = 3 V or 0 | | 9 | | | 9 | | | pF | |

† All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Unused terminals at $V_{CC}\text{ or GND}$

§ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than $V_{CC}\text{ or GND}$.

SN54LVTH646, SN74LVTH646

3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCBS705H – AUGUST 1997 – REVISED MAY 2004

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

| | | | SN54LVTH646 | | | | SN74LVTH646 | | | | UNIT |
|--------------------|---|-----------|--|-----|-------------------------|-----|--|-----|-------------------------|-----|------|
| | | | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | | $V_{CC} = 2.7\text{ V}$ | | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | | $V_{CC} = 2.7\text{ V}$ | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| f _{clock} | Clock frequency | | 150 | | 150 | | 150 | | 150 | | MHz |
| t _w | Pulse duration, CLK high or low | | 3.3 | | 3.3 | | 3.3 | | 3.3 | | ns |
| t _{su} | Setup time, A or B before CLKAB↑ or CLKBA↑ | Data high | 1.3 | | 1.6 | | 1.2 | | 1.5 | | ns |
| | | Data low | 1.9 | | 2.6 | | 1.6 | | 2.2 | | |
| t _h | Hold time, A or B after CLKAB↑ or CLKBA↑ | | 1.2 | | 1.2 | | 0.8 | | 0.8 | | ns |

switching characteristics over recommended operating free-air temperature range, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LVTH646 | | | | SN74LVTH646 | | | | UNIT | |
|------------------|-------------------|----------------|------------------------------------|-----|-------------------------|-----|------------------------------------|------|-----|-------------------------|------|-----|
| | | | V _{CC} = 3.3 V ± 0.3 V | | V _{CC} = 2.7 V | | V _{CC} = 3.3 V ± 0.3 V | | | V _{CC} = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | TYP† | MAX | MIN | | MAX |
| f _{max} | | | 150 | | 150 | | 150 | | | 150 | | MHz |
| t _{PLH} | CLKBA or CLKAB | A or B | 1 5.3 | | 5.9 | | 1.8 | 3.1 | 4.7 | 5.6 | | ns |
| t _{PHL} | | | 1.5 5 | | 5.9 | | 1.8 | 3.1 | 4.7 | 5.6 | | |
| t _{PLH} | A or B | B or A | 1 4.9 | | 5.6 | | 1.3 | 2.3 | 3.5 | 4.1 | | ns |
| t _{PHL} | | | 1.2 4.8 | | 5 | | 1.3 | 2.4 | 3.5 | 4.1 | | |
| t _{PLH} | SBA or SAB‡ | A or B | 1 5.3 | | 6.3 | | 1.5 | 3 | 4.9 | 6 | | ns |
| t _{PHL} | | | 1.3 5.3 | | 6.3 | | 1.5 | 3.3 | 4.9 | 6 | | |
| t _{PZH} | OE | A or B | 1 5.4 | | 6.7 | | 1.1 | 3.1 | 5.2 | 6.5 | | ns |
| t _{PZL} | | | 1 5.6 | | 6.7 | | 1.1 | 3.4 | 5.2 | 6.5 | | |
| t _{PHZ} | OE | A or B | 1.7 6.3 | | 6.5 | | 2.3 | 3.9 | 5.5 | 6.1 | | ns |
| t _{PLZ} | | | 2.2 6.3 | | 6.5 | | 2.3 | 4 | 5.5 | 5.9 | | |
| t _{PZH} | DIR | A or B | 1.2 5.6 | | 6.8 | | 1.3 | 3.4 | 5.2 | 6.6 | | ns |
| t _{PZL} | | | 1.2 6.7 | | 6.8 | | 1.3 | 3.6 | 5.2 | 6.6 | | |
| t _{PHZ} | DIR | A or B | 1.1 7.2 | | 8.1 | | 1.5 | 3.2 | 5.6 | 6.7 | | ns |
| t _{PLZ} | | | 1.4 6.1 | | 6.6 | | 1.5 | 3.8 | 5.6 | 6.3 | | |

\dagger All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

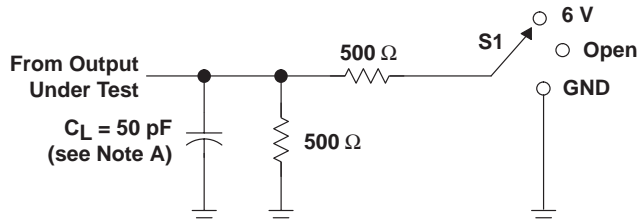
\ddagger These parameters are measured with the internal output state of the storage register opposite that of the bus input.

SN54LVTH646, SN74LVTH646

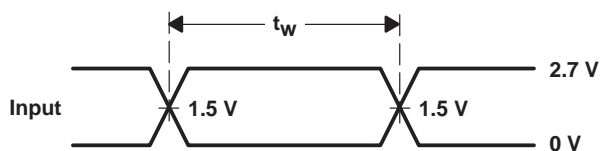
3.3-V ABT OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCBS705H – AUGUST 1997 – REVISED MAY 2004

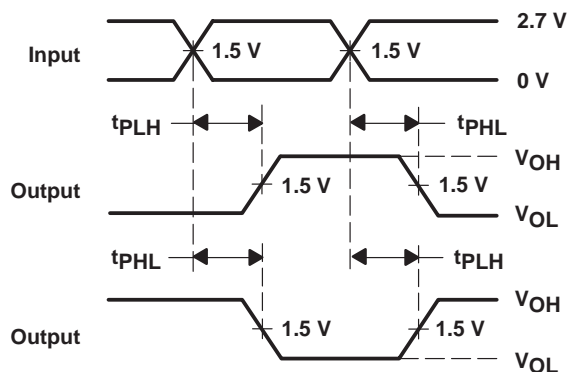
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

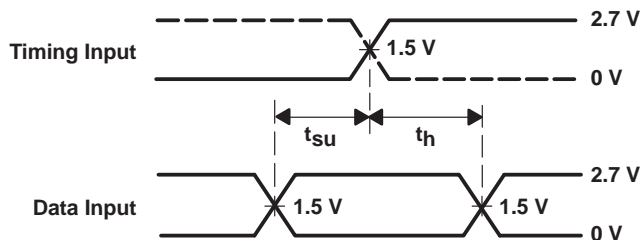


VOLTAGE WAVEFORMS
PULSE DURATION

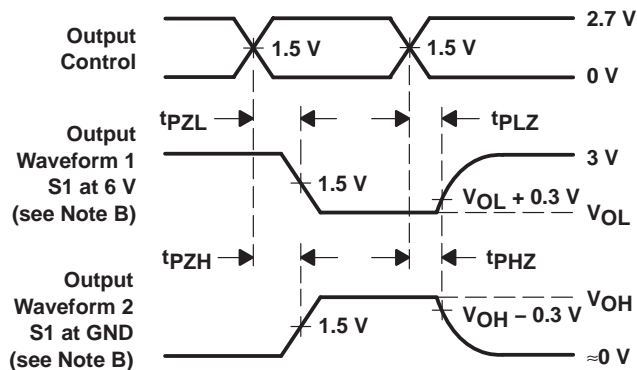


VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

| TEST | S1 |
|-------------------|------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | 6 V |
| t_{PHZ}/t_{PZH} | GND |



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|---|-------------------------|
| 5962-9674801Q3A | ACTIVE | LCCC | FK | 28 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962- 9674801Q3A SNJ54LVTH 646FK | Samples |
| 5962-9674801QKA | ACTIVE | CFP | W | 24 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-9674801QK A SNJ54LVTH646W | Samples |
| 5962-9674801QLA | ACTIVE | CDIP | JT | 24 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-9674801QL A SNJ54LVTH646JT | Samples |
| SN74LVTH646DBLE | OBSOLETE | SSOP | DB | 24 | | TBD | Call TI | Call TI | -40 to 85 | | |
| SN74LVTH646DW | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVTH646 | Samples |
| SN74LVTH646DWE4 | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVTH646 | Samples |
| SN74LVTH646DWG4 | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVTH646 | Samples |
| SN74LVTH646PWLE | OBSOLETE | TSSOP | PW | 24 | | TBD | Call TI | Call TI | -40 to 85 | | |
| SN74LVTH646PWR | ACTIVE | TSSOP | PW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LXH646 | Samples |
| SN74LVTH646PWRE4 | ACTIVE | TSSOP | PW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LXH646 | Samples |
| SN74LVTH646PWRG4 | ACTIVE | TSSOP | PW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LXH646 | Samples |
| SNJ54LVTH646FK | ACTIVE | LCCC | FK | 28 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962- 9674801Q3A SNJ54LVTH 646FK | Samples |
| SNJ54LVTH646JT | ACTIVE | CDIP | JT | 24 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-9674801QL A SNJ54LVTH646JT | Samples |
| SNJ54LVTH646W | ACTIVE | CFP | W | 24 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-9674801QK A SNJ54LVTH646W | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54LVTH646, SN74LVTH646 :

● Catalog: [SN74LVTH646](#)

● Enhanced Product: [SN74LVTH646-EP](#), [SN74LVTH646-EP](#)

- Military: [SN54LVTH646](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVTH646PWR | TSSOP | PW | 24 | 2000 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



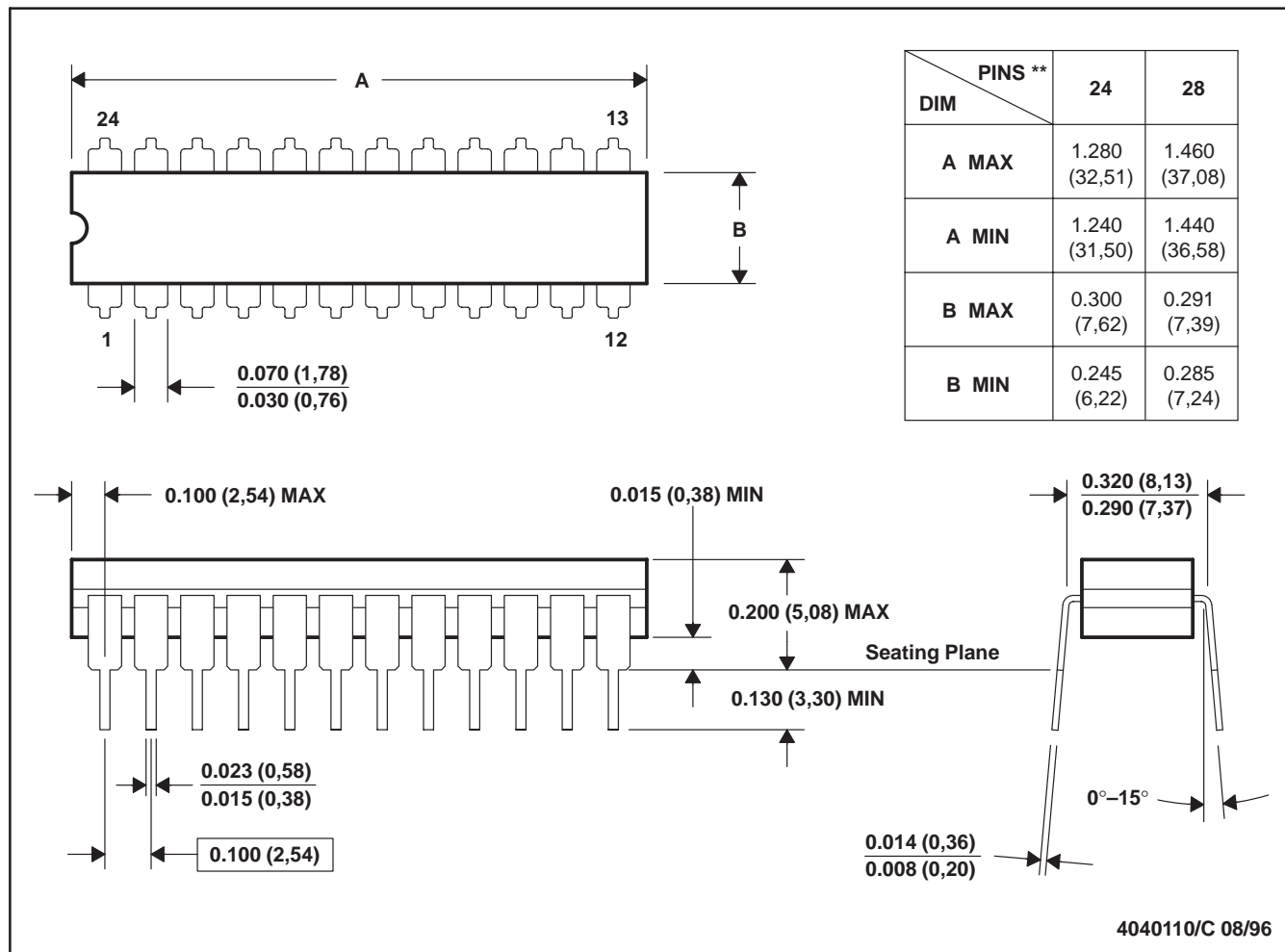
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVTH646PWR | TSSOP | PW | 24 | 2000 | 367.0 | 367.0 | 38.0 |

JT (R-GDIP-T**)

CERAMIC DUAL-IN-LINE

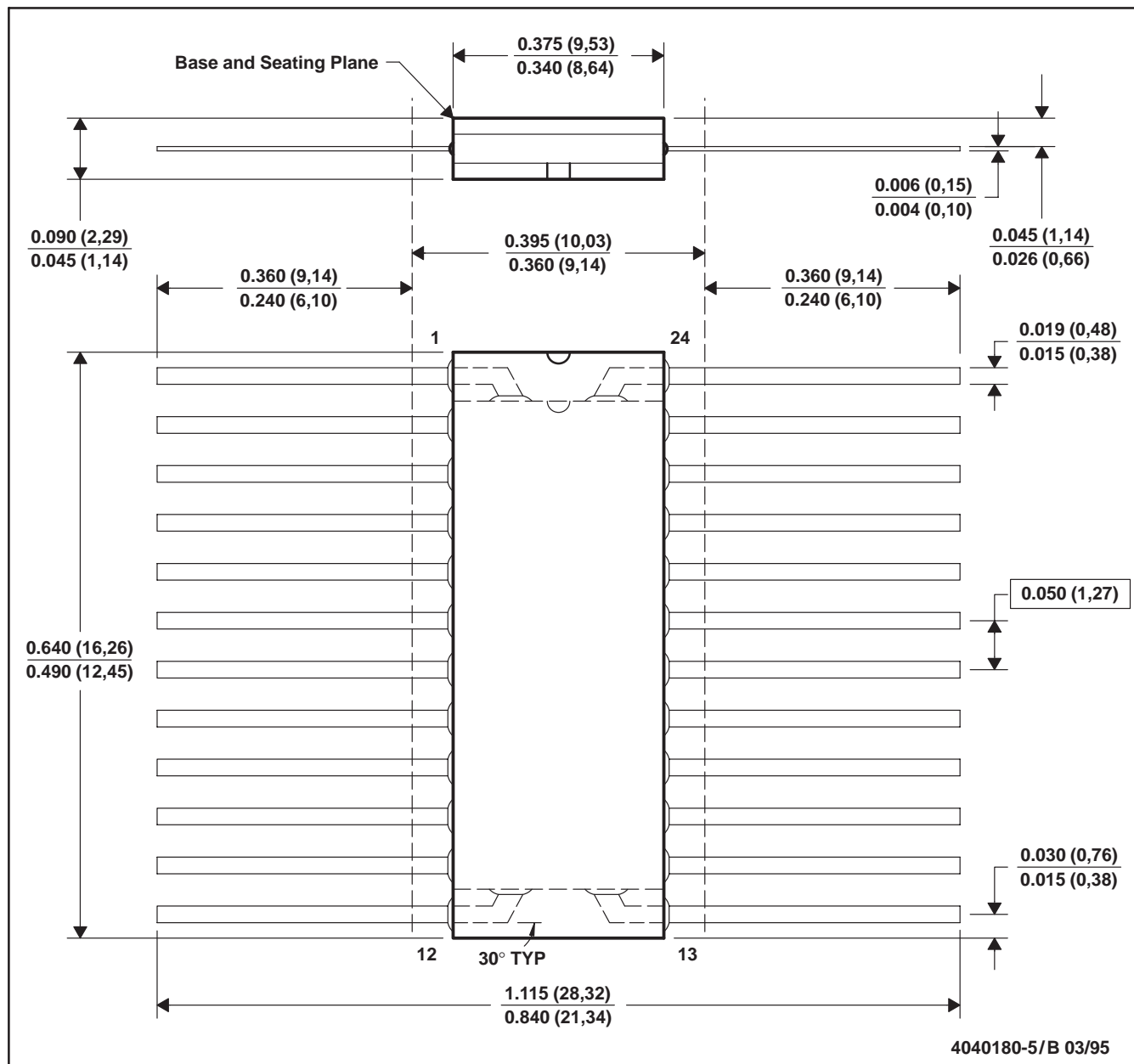
24 LEADS SHOWN



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification.
 - Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

W (R-GDFP-F24)

CERAMIC DUAL FLATPACK

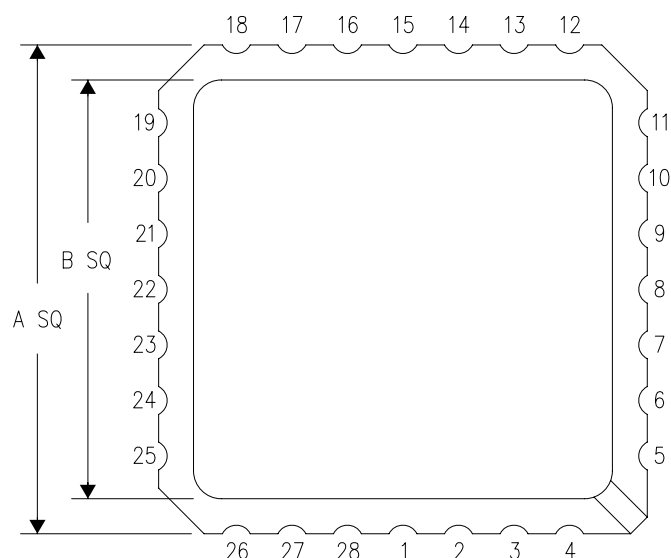


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Falls within MIL-STD-1835 GDFP2-F24 and JEDEC MO-070AD
 - E. Index point is provided on cap for terminal identification only.

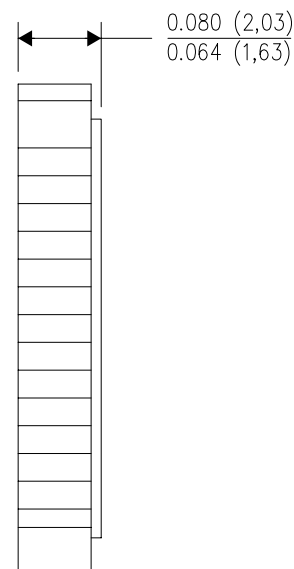
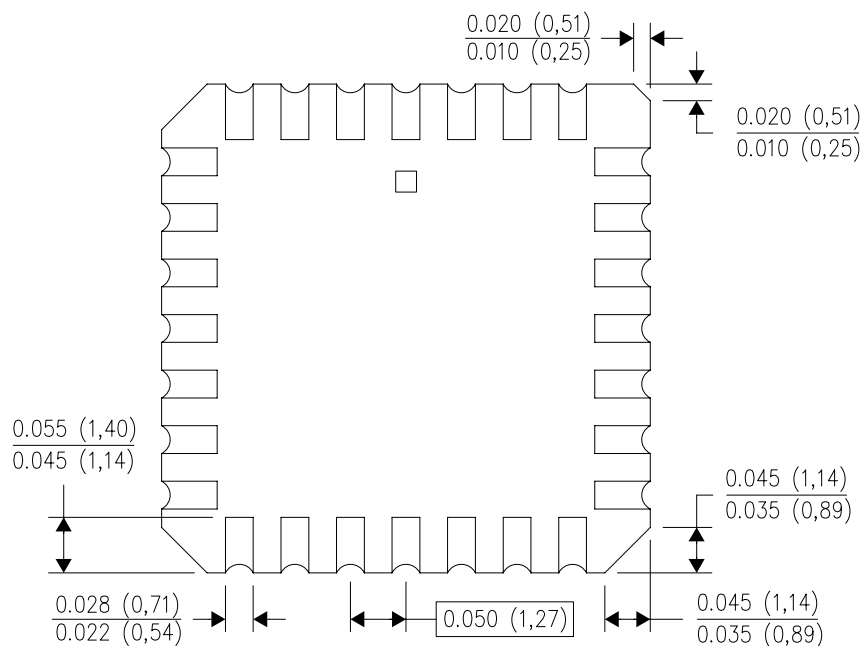
FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF TERMINALS ** | A | | B | |
|---------------------------|------------------|------------------|------------------|------------------|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.740 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |

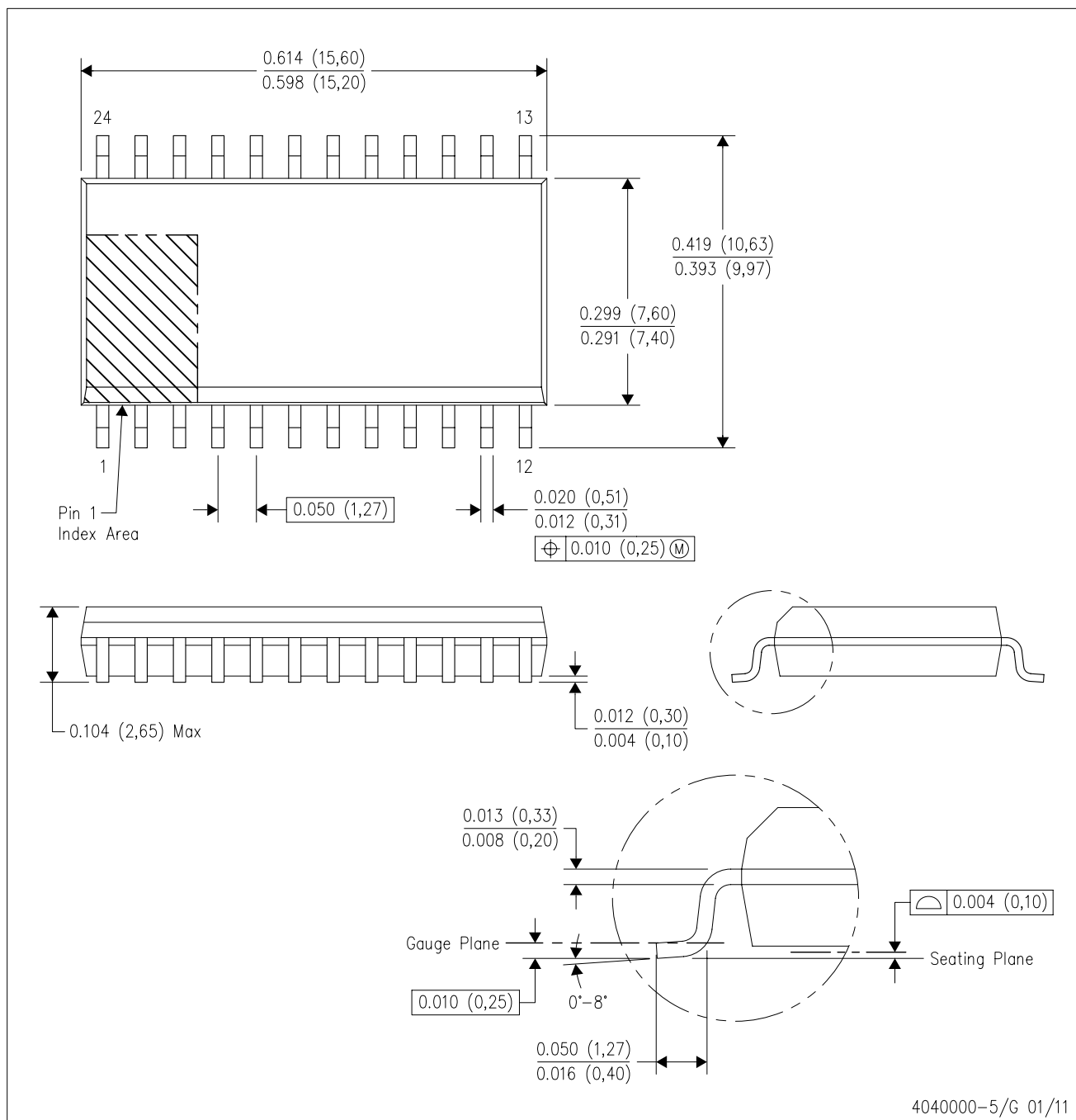


4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

DW (R-PDSO-G24)

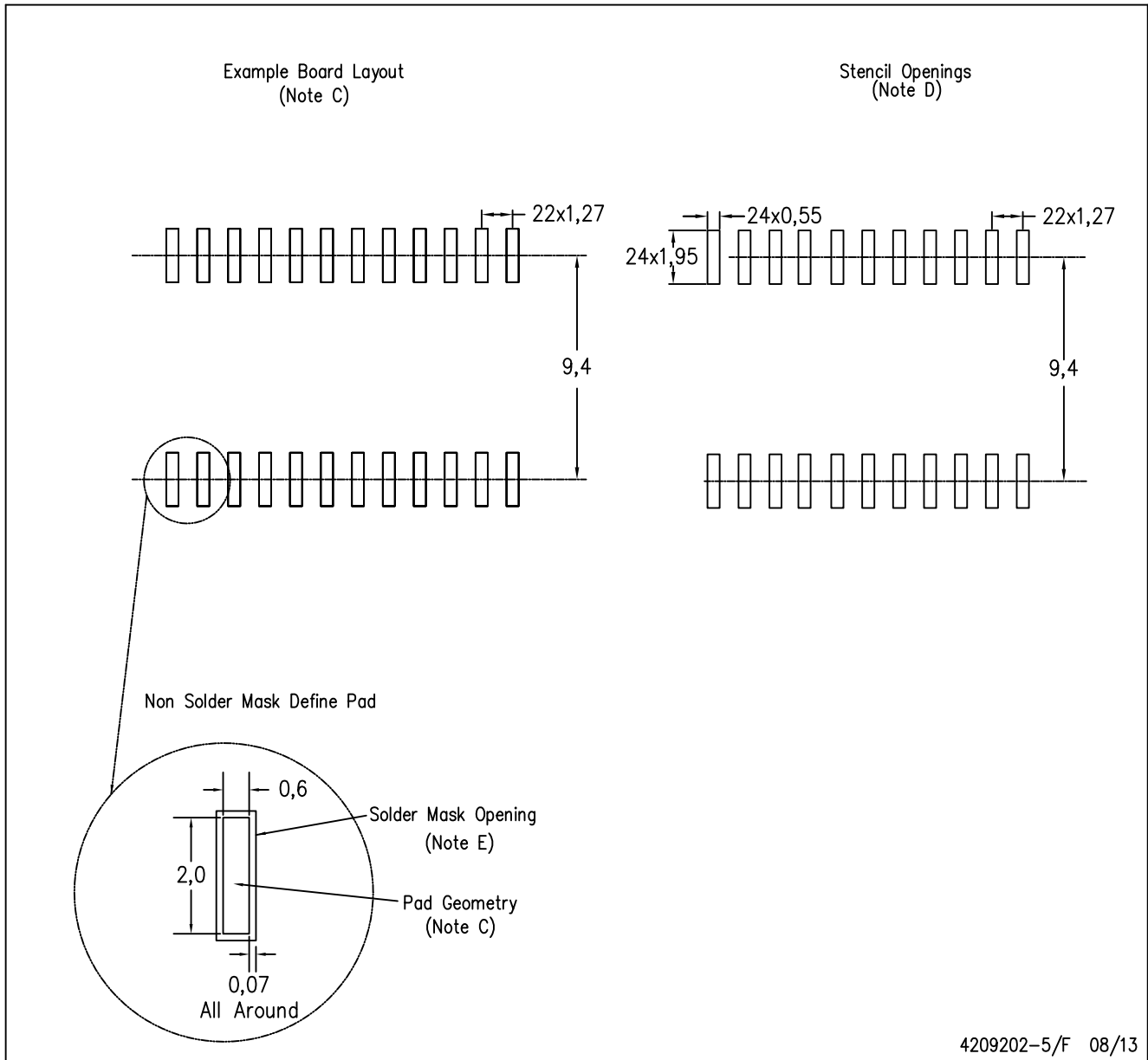
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AD.

DW (R-PDSO-G24)

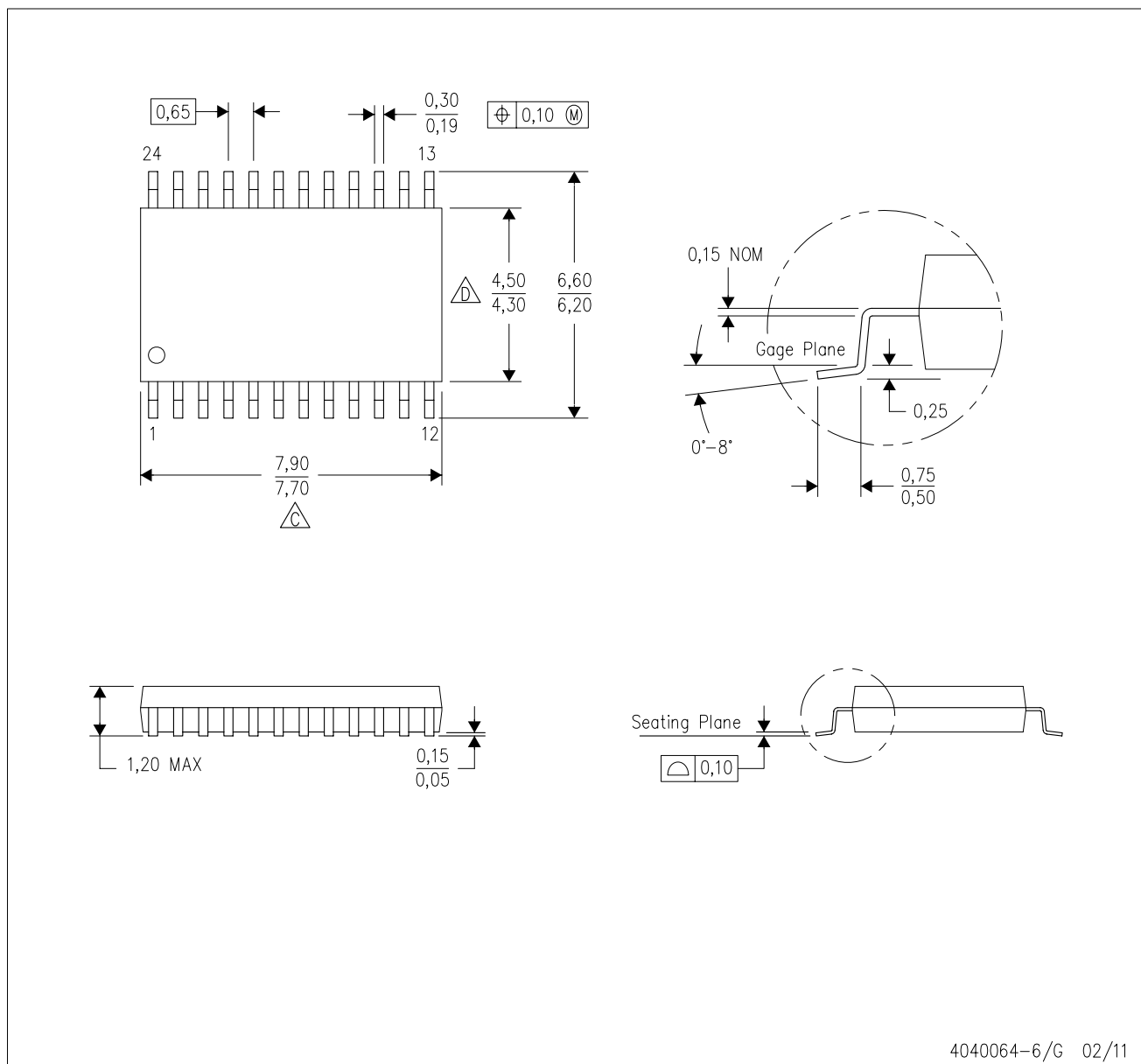
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G24)

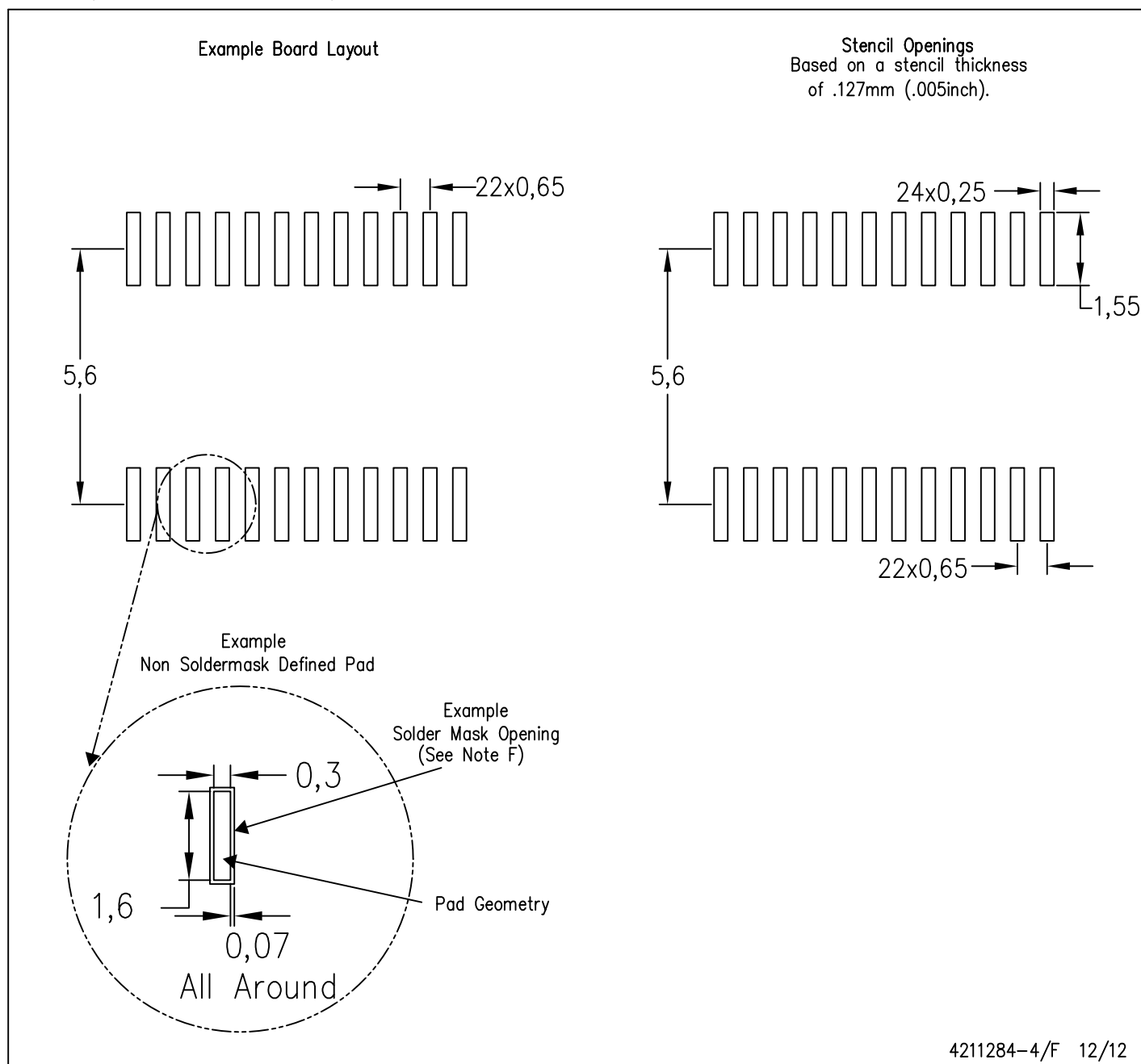
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G24)

PLASTIC SMALL OUTLINE

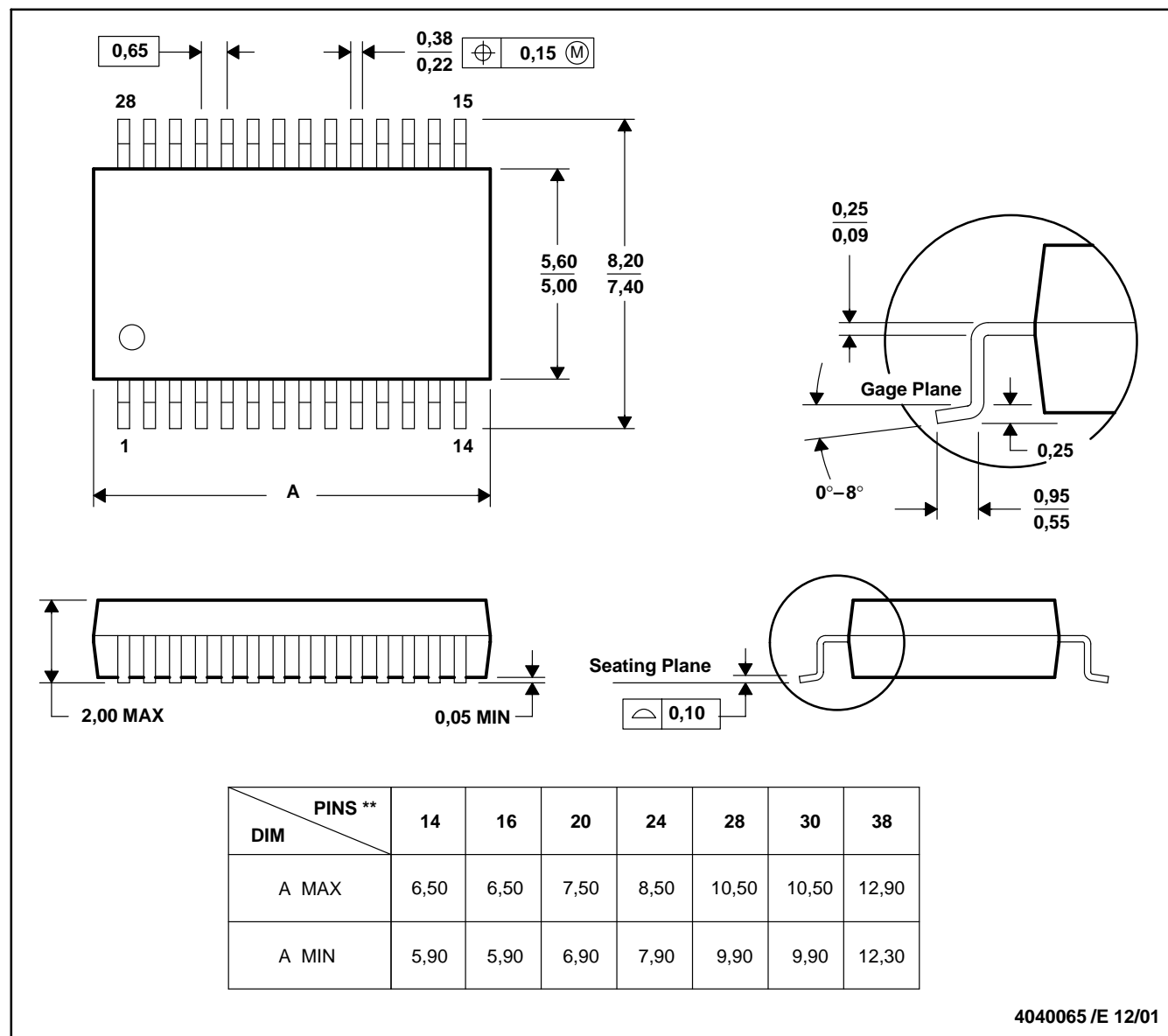


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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