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TEXAS INSTRUMENTS

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SN54LVTH162373, SN74LVTH162373
3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES
WITH 3-STATE OUTPUTS

SCBS261M−JULY 1993−REVISED DECEMBER 2006

FEATURES

- **Members of the Texas Instruments Widebus™ Family**

- **Output Ports Have Equivalent 22-Ω Series Resistors, So No External Resistors Are Required**

- **Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**

- **Support Unregulated Battery Operation Down to 2.7 V**

- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C**

- **I_{off} and Power-Up 3-State Support Hot Insertion**

- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**

- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**

- **Flow-Through Architecture Optimizes PCB Layout**

- **Latch-Up Performance Exceeds 500 mA Per JESD 17**

- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**

SN54LVTH162373 . . . WD PACKAGE
SN74LVTH162373 . . . DGG OR DL PACKAGE
(TOP VIEW)

1$\overline{\text{OE}}$	1	48	1LE
1Q1	2	47	1D1
1Q2	3	46	1D2
GND	4	45	GND
1Q3	5	44	1D3
1Q4	6	43	1D4
V_{CC}	7	42	V_{CC}
1Q5	8	41	1D5
1Q6	9	40	1D6
GND	10	39	GND
1Q7	11	38	1D7
1Q8	12	37	1D8
2Q1	13	36	2D1
2Q2	14	35	2D2
GND	15	34	GND
2Q3	16	33	2D3
2Q4	17	32	2D4
V_{CC}	18	31	V_{CC}
2Q5	19	30	2D5
2Q6	20	29	2D6
GND	21	28	GND
2Q7	22	27	2D7
2Q8	23	26	2D8
2$\overline{\text{OE}}$	24	25	2LE

DESCRIPTION/ORDERING INFORMATION

The 'LVTH162373 devices are 16-bit transparent D-type latches with 3-state outputs designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. These devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

ORDERING INFORMATION

T_A	PACKAGE[1]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP – DL	Tube of 25	SN74LVTH162373DL	LVTH162373
			74LVTH162373DLG4	
		Reel of 1000	SN74LVTH162373DLR	
			74LVTH162373DLRG4	
	TSSOP – DGG	Reel of 2000	SN74LVTH162373DGGR	LVTH162373
			74LVTH162373DGGRE4	
	VFBGA – GQL	Reel of 1000	SN74LVTH162373KR	LL2373
	VFBGA – ZQL (Pb-free)		74LVTH162373ZQLR	
−55°C to 125°C	CFP – WD	Tube	SNJ54LVTH162373WD	SNJ54LVTH162373WD

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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DESCRIPTION/ORDERING INFORMATION (CONTINUED)

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The outputs, which are designed to source or sink up to 12 mA, include equivalent 22-Ω series resistors to reduce overshoot and undershoot.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When V_{CC} is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

These devices can be used as two 8-bit latches or one 16-bit latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the D inputs.

GQL OR ZQL PACKAGE
(TOP VIEW)
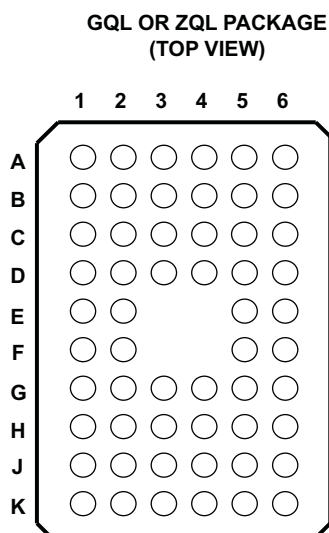
TERMINAL ASSIGNMENTS[1]

	1	2	3	4	5	6
A	1$\overline{OE}$	NC	NC	NC	NC	1LE
B	1Q2	1Q1	GND	GND	1D1	1D2
C	1Q4	1Q3	V_{CC}	V_{CC}	1D3	1D4
D	1Q6	1Q5	GND	GND	1D5	1D6
E	1Q8	1Q7			1D7	1D8
F	2Q1	2Q2			2D2	2D1
G	2Q3	2Q4	GND	GND	2D4	2D3
H	2Q5	2Q6	V_{CC}	V_{CC}	2D6	2D5
J	2Q7	2Q8	GND	GND	2D8	2D7
K	2$\overline{OE}$	NC	NC	NC	NC	2LE

(1) NC - No internal connection

FUNCTION TABLE
(each 8-bit section)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

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LOGIC DIAGRAM (POSITIVE LOGIC)
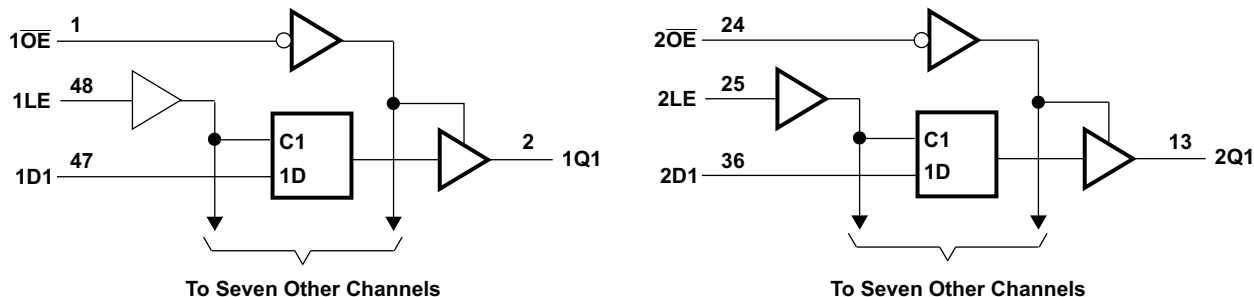
Pin numbers shown are for the DGG, DL, and WD packages.

Absolute Maximum Ratings[1]

over recommended operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		−0.5	4.6	V
V_I	Input voltage range[2]		−0.5	7	V
V_O	Voltage range applied to any output in the high-impedance or power-off state[2]		−0.5	7	V
V_O	Voltage range applied to any output in the high state[2]		−0.5	V_{CC} + 0.5	V
I_O	Current into any output in the low state			30	mA
I_O	Current into any output in the high state[3]			30	mA
I_{IK}	Input clamp current	$V_I < 0$		−50	mA
I_{OK}	Output clamp current	$V_O < 0$		−50	mA
θ_{JA}	Package thermal impedance[4]	DGG package		70	°C/W
		DL package		63	
		GQL/ZQL package		42	
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) This current flows only when the output is in the high state and $V_O > V_{CC}$.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions[1]

			SN54LVTH162373		SN74LVTH162373		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage range		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−12		−12	mA
I_{OL}	Low-level output current			12		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200		200		μs/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54LVTH162373			SN74LVTH162373			UNIT
				MIN	TYP[1]	MAX	MIN	TYP[1]	MAX	
V_{IK}		V_{CC} = 2.7 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 3 V,	I_{OH} = −12 mA	2			2			V
V_{OL}		V_{CC} = 3 V,	I_{OL} = 12 mA			0.8			0.8	V
I_I		V_{CC} = 0 or 3.6 V,	V_I = 5.5 V			10			10	μA
	Control inputs	V_{CC} = 3.6 V,	V_I = V_{CC} or GND			±1			±1	
	Data inputs	V_{CC} = 3.6 V	V_I = V_{CC}			1			1	
			V_I = 0			−5			−5	
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 4.5 V						±100	μA
$I_{I(hold)}$	Data inputs	V_{CC} = 3 V	V_I = 0.8 V	75			75			μA
			V_I = 2 V	−75			−75			
		V_{CC} = 3.6 V[2],	V_I = 0 to 3.6 V						500 −750	
I_{OZH}		V_{CC} = 3.6 V,	V_O = 3 V			5			5	μA
I_{OZL}		V_{CC} = 3.6 V,	V_O = 0.5 V			−5			−5	μA
I_{OZPU}		V_{CC} = 0 to 1.5 V, V_O = 0.5 V to 3 V, $\overline{OE}$ = don't care				±100[3]			±100	μA
I_{OZPD}		V_{CC} = 1.5 V to 0, V_O = 0.5 V to 3 V, $\overline{OE}$ = don't care				±100[3]			±100	μA
I_{CC}		V_{CC} = 3.6 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			0.19			0.19	mA
			Outputs low			5			5	
			Outputs disabled			0.19			0.19	
ΔI_{CC}[4]		V_{CC} = 3 V to 3.6 V, One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND				0.2			0.2	mA
C_i		V_I = 3 V or 0			3			3		pF
C_o		V_O = 3 V or 0			9			9		pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.
(3) On products compliant to MIL-PRF-38535, this parameter is not production tested.
(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

Timing Requirements

over operating free-air temperature range (unless otherwise noted) (see Figure 1)

		SN54LVTH162373				SN74LVTH162373				UNIT
		V_{CC} = 3.3 V ±0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ±0.3 V		V_{CC} = 2.7 V		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high	3		3		3		3		ns
t_{su}	Setup time, data before LE↓	1.3		0.6		1		0.6		ns
t_h	Hold time, data after LE↓	1		1.1		1		1.1		ns

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Switching Characteristics

over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH162373				SN74LVTH162373					UNIT
			V_{CC} = 3.3 V ±0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V ±0.3 V			V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP[1]	MAX	MIN	MAX	
t_{PLH}	D	Q	1.8	5		5.7	1.9	3.1	4.6		5.1	ns
t_{PHL}			1.8	4.4		4.8	1.9	2.8	4		4.3	
t_{PLH}	LE	Q	2.1	5.4		6.2	2.2	3.4	5.1		5.8	ns
t_{PHL}			2.1	4.9		4.7	2.2	3.2	4.6		4.3	
t_{PZH}	$\overline{OE}$	Q	1.7	5.6		7	1.8	3.2	5.4		6.6	ns
t_{PZL}			1.7	5.3		5.9	1.8	3.2	4.9		5.5	
t_{PHZ}	$\overline{OE}$	Q	2.3	6.3		6.6	2.4	3.8	5.4		5.7	ns
t_{PLZ}			1	7.4		6.4	2.2	3.5	5.1		5	
$t_{sk(LH)}$									0.5			ns
$t_{sk(HL)}$									0.5			

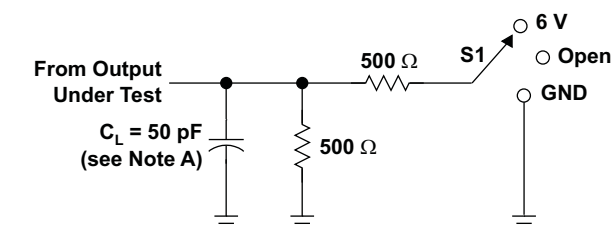(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

SN54LVTH162373, SN74LVTH162373
3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS
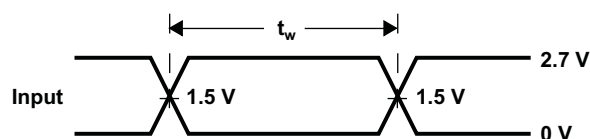SCBS261M−JULY 1993−REVISED DECEMBER 2006

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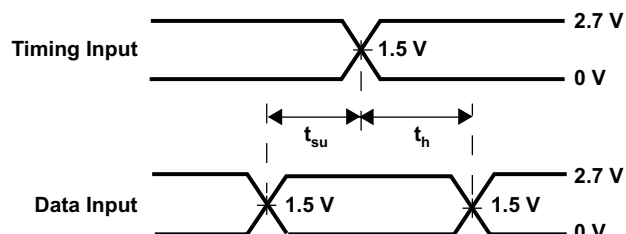
PARAMETER MEASUREMENT INFORMATION

LOAD CIRCUIT

From Output Under Test — 500 Ω — S1 — 6 V / Open / GND

C_L = 50 pF (see Note A)   500 Ω

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

VOLTAGE WAVEFORMS
PULSE DURATION

Input — t_w — 1.5 V — 1.5 V — 2.7 V / 0 V

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

Timing Input — 1.5 V — 2.7 V / 0 V

t_{su} — t_h

Data Input — 1.5 V — 1.5 V — 2.7 V / 0 V
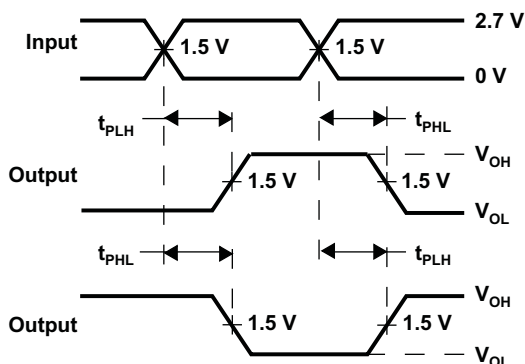
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

Input — 1.5 V — 1.5 V — 2.7 V / 0 V

t_{PLH} — t_{PHL}

Output — 1.5 V — 1.5 V — V_{OH} / V_{OL}

t_{PHL} — t_{PLH}

Output — 1.5 V — 1.5 V — V_{OH} / V_{OL}
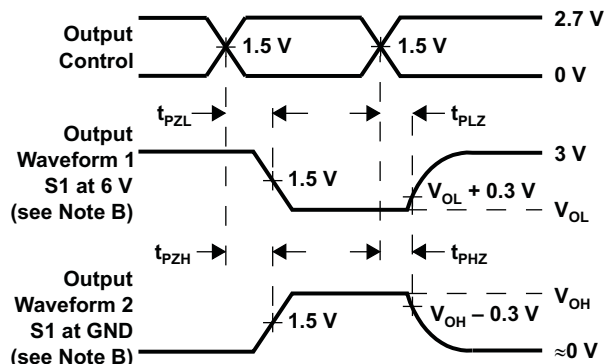
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

Output Control — 1.5 V — 1.5 V — 2.7 V / 0 V

t_{PZL} — t_{PLZ}

Output Waveform 1 S1 at 6 V (see Note B) — 1.5 V — V_{OL} + 0.3 V — 3 V / V_{OL}

t_{PZH} — t_{PHZ}

Output Waveform 2 S1 at GND (see Note B) — 1.5 V — V_{OH} − 0.3 V — V_{OH} / ≈0 V

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9763801QXA	ACTIVE	CFP	WD	48	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9763801QX A SNJ54LVTH16237 3WD	Samples
5962-9763801VXA	ACTIVE	CFP	WD	48	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9763801VX A SNV54LVTH16237 3WD	Samples
74LVTH162373DGGRE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH162373	Samples
74LVTH162373DGGRG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH162373	Samples
74LVTH162373DLG4	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH162373	Samples
74LVTH162373DLRG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH162373	Samples
74LVTH162373ZQLR	ACTIVE	BGA MICROSTAR JUNIOR	ZQL	56	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	LL2373	Samples
SN74LVTH162373DGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH162373	Samples
SN74LVTH162373DL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH162373	Samples
SN74LVTH162373DLR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH162373	Samples
SN74LVTH162373KR	OBSOLETE	BGA MICROSTAR JUNIOR	GQL	56		TBD	Call TI	Call TI	-40 to 85	LL2373	
SNJ54LVTH162373WD	ACTIVE	CFP	WD	48	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9763801QX A SNJ54LVTH16237 3WD	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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OTHER QUALIFIED VERSIONS OF SN54LVTH162373, SN54LVTH162373-SP, SN74LVTH162373 :

● Catalog: SN74LVTH162373, SN54LVTH162373

● Enhanced Product: SN74LVTH162373-EP, SN74LVTH162373-EP

● Military: SN54LVTH162373

● Space: SN54LVTH162373-SP

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

- Military - QML certified for Military and Defense Applications

- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74LVTH162373ZQLR	BGA MICROSTAR JUNIOR	ZQL	56	1000	330.0	16.4	4.8	7.3	1.5	8.0	16.0	Q1
SN74LVTH162373DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1
SN74LVTH162373DLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS
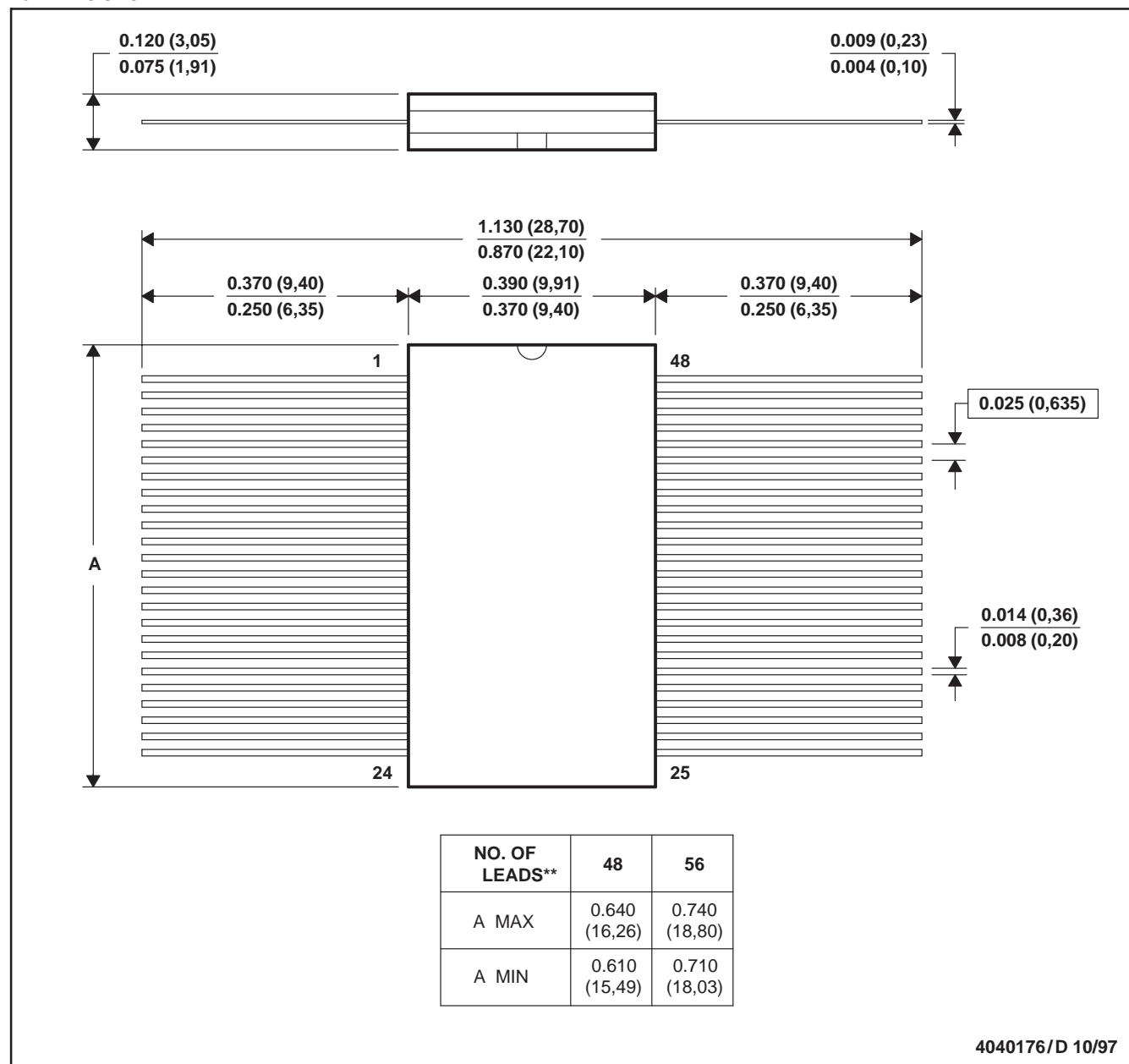

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74LVTH162373ZQLR	BGA MICROSTAR JUNIOR	ZQL	56	1000	333.2	345.9	28.6
SN74LVTH162373DGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0
SN74LVTH162373DLR	SSOP	DL	48	1000	367.0	367.0	55.0

WD (R-GDFP-F**)   **CERAMIC DUAL FLATPACK**

48 LEADS SHOWN

$$\frac{0.120\ (3,05)}{0.075\ (1,91)} \qquad\qquad \frac{0.009\ (0,23)}{0.004\ (0,10)}$$

$$\frac{1.130\ (28,70)}{0.870\ (22,10)}$$

$$\frac{0.370\ (9,40)}{0.250\ (6,35)} \qquad \frac{0.390\ (9,91)}{0.370\ (9,40)} \qquad \frac{0.370\ (9,40)}{0.250\ (6,35)}$$

1   48

0.025 (0,635)

A

$$\frac{0.014\ (0,36)}{0.008\ (0,20)}$$

24   25

NO. OF LEADS**	48	56
A MAX	0.640 (16,26)	0.740 (18,80)
A MIN	0.610 (15,49)	0.710 (18,03)

4040176 / D 10/97
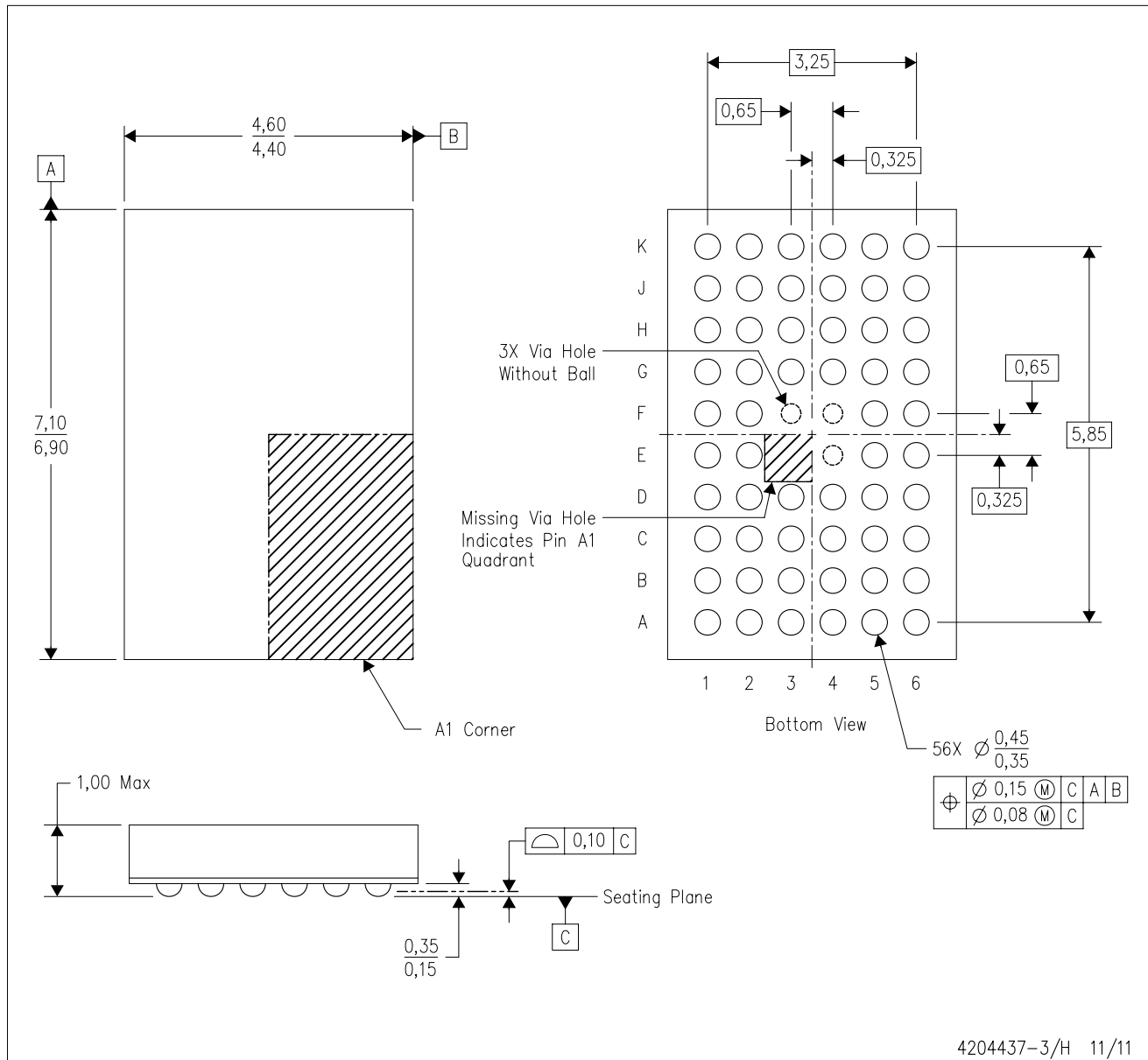
NOTES: A. All linear dimensions are in inches (millimeters).
  B. This drawing is subject to change without notice.
  C. This package can be hermetically sealed with a ceramic lid using glass frit.
  D. Index point is provided on cap for terminal identification only
  E. Falls within MIL STD 1835: GDFP1-F48 and JEDEC MO-146AA
        GDFP1-F56 and JEDEC MO-146AB

TEXAS INSTRUMENTS

ZQL (R−PBGA−N56) PLASTIC BALL GRID ARRAY

4,60 / 4,40

7,10 / 6,90

A1 Corner

1,00 Max

0,35 / 0,15

Seating Plane

3,25

0,65

0,325

3X Via Hole Without Ball

Missing Via Hole Indicates Pin A1 Quadrant

0,65

5,85

0,325

Bottom View

56X Ø 0,45 / 0,35

Ø 0,15 (M) C A B
Ø 0,08 (M) C

4204437−3/H 11/11
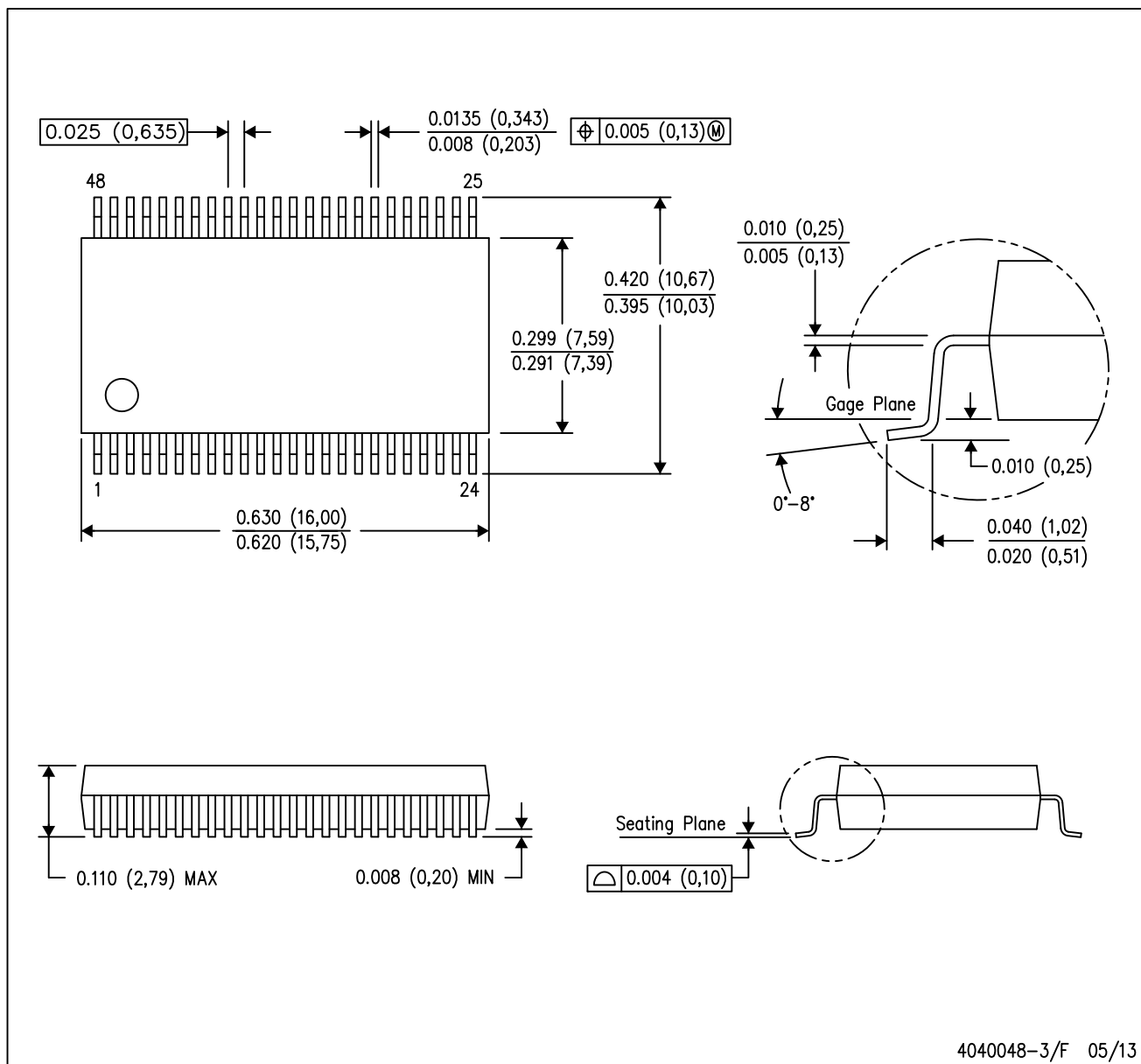
NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO−285 variation BA−2.
D. This package is Pb−free. Refer to the 56 GQL package (drawing 4200583) for tin−lead (SnPb).

MicroStar Junior is a trademark of Texas Instruments

TEXAS INSTRUMENTS
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DL (R−PDSO−G48)   PLASTIC SMALL−OUTLINE PACKAGE

0.025 (0,635)

0.0135 (0,343)
0.008 (0,203)

⊕ 0.005 (0,13) Ⓜ

48   25

0.420 (10,67)
0.395 (10,03)

0.299 (7,59)
0.291 (7,39)

0.010 (0,25)
0.005 (0,13)

Gage Plane

0.010 (0,25)

0°−8°

0.040 (1,02)
0.020 (0,51)

1   24

0.630 (16,00)
0.620 (15,75)

0.110 (2,79) MAX   0.008 (0,20) MIN

Seating Plane

△ 0.004 (0,10)

4040048−3/F 05/13

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
        D. Falls within JEDEC MO−118
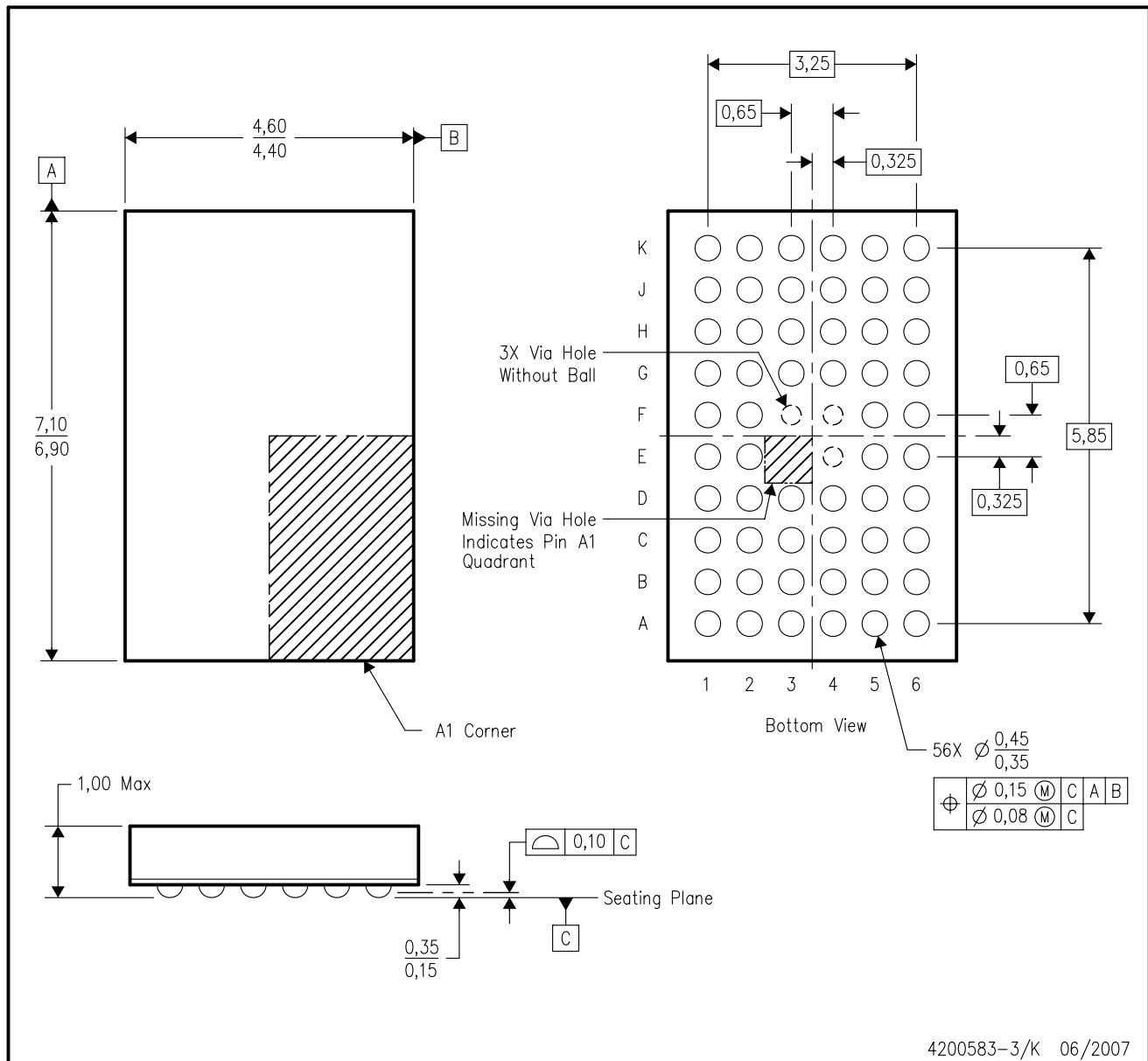
PowerPAD is a trademark of Texas Instruments.

TEXAS
INSTRUMENTS
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GQL (R−PBGA−N56)   PLASTIC BALL GRID ARRAY

4,60 / 4,40   B

A

7,10 / 6,90

A1 Corner

1,00 Max

0,10 C

Seating Plane

C

0,35 / 0,15

3,25

0,65

0,325

K
J
H
G
F
E
D
C
B
A

1 2 3 4 5 6

3X Via Hole
Without Ball

Missing Via Hole
Indicates Pin A1
Quadrant

Bottom View

0,65

5,85

0,325

56X Ø 0,45 / 0,35

⊕	Ø 0,15 Ⓜ	C	A	B
	Ø 0,08 Ⓜ	C		

4200583−3/K   06/2007

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
        B. This drawing is subject to change without notice.
        C. Falls within JEDEC MO−285 variation BA−2.
        D. This package is tin−lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead−free.

DGG (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN

PINS ** DIM	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

4040078 / F 12/97

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold protrusion not to exceed 0,15.
        D. Falls within JEDEC MO-153

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