

## FEATURES

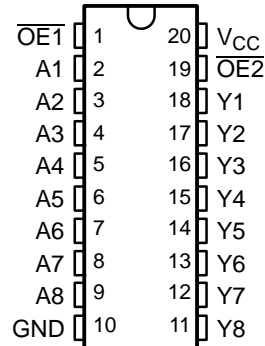
- Operate From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max  $t_{pd}$  of 5.3 ns at 3.3 V
- Typical  $V_{OLP}$  (Output Ground Bounce) < 0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot) > 2 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Support Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V  $V_{CC}$ )
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 1000-V Charged-Device Model (C101)

## DESCRIPTION/ORDERING INFORMATION

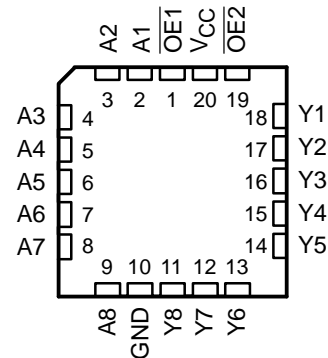
The SN54LVC540A octal buffer/driver is designed for 2.7-V to 3.6-V  $V_{CC}$  operation, and the SN74LVC540A octal buffer/driver is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

These devices are ideal for driving bus lines or buffer memory address registers. These devices feature inputs and outputs on opposite sides of the package that facilitate printed circuit board layout.

SN54LVC540A . . . J OR W PACKAGE  
SN74LVC540A . . . DB, DGV, DW, NS, OR PW PACKAGE  
(TOP VIEW)



SN54LVC540A . . . FK PACKAGE  
(TOP VIEW)



## ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOIC – DW	Tube of 25	SN74LVC540ADW	LVC540A
		Reel of 2000	SN74LVC540ADWR	
	SOP – NS	Reel of 2000	SN74LVC540ANSR	LVC540A
	SSOP – DB	Reel of 2000	SN74LVC540ADBR	LC540A
	TSSOP – PW	Tube of 70	SN74LVC540APW	LC540A
		Reel of 2000	SN74LVC540APWR	
		Reel of 250	SN74LVC540APWT	
–55°C to 125°C	TVSOP – DGV	Reel of 2000	SN74LVC540ADGVR	LC540A
	CDIP – J	Tube of 20	SNJ54LVC540AJ	SNJ54LVC540AJ
	CFP – W	Tube of 85	SNJ54LVC540AW	SNJ54LVC540AW
	LCCC – FK	Tube of 55	SNJ54LVC540AFK	SNJ54LVC540AFK

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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## SCAS297M–JANUARY 1993–REVISED MAY 2005

The 3-state control gate is a 2-input AND gate with active-low inputs so that, if either output-enable ( $\overline{\text{OE1}}$  or  $\overline{\text{OE2}}$ ) input is high, all outputs are in the high-impedance state.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

These devices are fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

To ensure the high-impedance state during power up or power down,  $\overline{\text{OE}}$  should be tied to  $V_{\text{CC}}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

INPUTS			OUTPUT Y
OE1	OE2	A	
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

The logic diagram for the 74VHC04 shows two inverters. The first inverter has inputs  $\overline{OE1}$  (pin 1) and  $\overline{OE2}$  (pin 19). Its output is connected to pin 18, which is labeled Y1. The second inverter has input A1 (pin 2) and its output is connected to pin 18. A vertical arrow points downwards from the output of the first inverter, labeled "To Seven Other Channels".

## Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	–0.5	6.5	V
$V_I$	Input voltage range <sup>(2)</sup>	–0.5	6.5	V
$V_O$	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	–0.5	6.5	V
$V_O$	Voltage range applied to any output in the high or low state <sup>(2)(3)</sup>	–0.5	$V_{CC} + 0.5$	V
$I_{IK}$	Input clamp current	$V_I < 0$		–50 mA
$I_{OK}$	Output clamp current	$V_O < 0$		–50 mA
$I_O$	Continuous output current			±50 mA
	Continuous current through $V_{CC}$ or GND			±100 mA
$\theta_{JA}$	Package thermal impedance <sup>(4)</sup>	DB package		70 °C/W
		DGV package		92
		DW package		58
		NS package		60
		PW package		83
$T_{stg}$	Storage temperature range	–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of  $V_{CC}$  is provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

## Recommended Operating Conditions<sup>(1)</sup>

			SN54LVC540A		SN74LVC540A		UNIT
			MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	Operating	2	3.6	1.65	3.6	V
		Data retention only	1.5		1.5		
$V_{IH}$	High-level input voltage	$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$			$0.65 \times V_{CC}$		V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$			1.7		
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		2		
$V_{IL}$	Low-level input voltage	$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$			$0.35 \times V_{CC}$		V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$			0.7		
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8		0.8	
$V_I$	Input voltage		0	5.5	0	5.5	V
$V_O$	Output voltage	High or low state	0	$V_{CC}$	0	$V_{CC}$	V
		3-state	0	5.5	0	5.5	
$I_{OH}$	High-level output current	$V_{CC} = 1.65 \text{ V}$				–4	mA
		$V_{CC} = 2.3 \text{ V}$				–8	
		$V_{CC} = 2.7 \text{ V}$		–12		–12	
		$V_{CC} = 3 \text{ V}$		–24		–24	
$I_{OL}$	Low-level output current	$V_{CC} = 1.65 \text{ V}$				4	mA
		$V_{CC} = 2.3 \text{ V}$				8	
		$V_{CC} = 2.7 \text{ V}$		12		12	
		$V_{CC} = 3 \text{ V}$		24		24	
$T_A$	Operating free-air temperature		–55	125	–40	85	°C

- (1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN54LVC540A, SN74LVC540A

## OCTAL BUFFERS/DRIVERS

### WITH 3-STATE OUTPUTS

SCAS297M–JANUARY 1993–REVISED MAY 2005

## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V <sub>CC</sub>	SN54LVC540A		SN74LVC540A		UNIT
				MIN	TYP <sup>(1)</sup> MAX	MIN	TYP <sup>(1)</sup> MAX	
V <sub>OH</sub>	I <sub>OH</sub> = –100 μA		1.65 V to 3.6 V	V <sub>CC</sub> – 0.2		V <sub>CC</sub> – 0.2		V
			2.7 V to 3.6 V					
	I <sub>OH</sub> = –4 mA		1.65 V			1.2		
	I <sub>OH</sub> = –8 mA		2.3 V			1.7		
	I <sub>OH</sub> = –12 mA		2.7 V	2.2		2.2		
			3 V	2.4		2.4		
	I <sub>OH</sub> = –24 mA		3 V	2.2		2.2		
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA		1.65 V to 3.6 V	0.2		0.2		V
			2.7 V to 3.6 V					
	I <sub>OL</sub> = 4 mA		1.65 V			0.45		
	I <sub>OL</sub> = 8 mA		2.3 V			0.7		
	I <sub>OL</sub> = 12 mA		2.7 V	0.4		0.4		
	I <sub>OL</sub> = 24 mA		3 V	0.55		0.55		
	I <sub>I</sub>	V <sub>I</sub> = 0 to 5.5 V	3.6 V	±5		±5		
I <sub>off</sub>	V <sub>I</sub> or V <sub>O</sub> = 5.5 V		0			±10		μA
I <sub>OZ</sub>	V <sub>O</sub> = 0 to 5.5 V		3.6 V	±15		±10		μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	I <sub>O</sub> = 0	3.6 V	10		10		μA
	3.6 V ≤ V <sub>I</sub> ≤ 5.5 V <sup>(2)</sup>			10		10		
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND		2.7 V to 3.6 V	500		500		μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND		3.3 V	4		4		pF
C <sub>o</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND		3.3 V	5.5		5.5		pF

(1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

(2) This applies in the disabled state only.

## Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVC540A				UNIT
			V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	7.1		1	5.3	ns
t <sub>en</sub>	$\overline{\text{OE}}$	Y	8		1	6.6	ns
t <sub>dis</sub>	$\overline{\text{OE}}$	Y	8.2		1	7.4	ns

## Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC540A								UNIT
			$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$		$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	A	Y	1	16.4	1	7.8	1	7.1	1.4	5.3	ns
$t_{en}$	$\overline{OE}$	Y	1	16.5	1	10.5	1	8	1.1	6.6	ns
$t_{dis}$	$\overline{OE}$	Y	1	15.9	1	9	1	8.2	1.8	7.4	ns
$t_{sk(o)}$									1		ns

## Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$	$V_{CC} = 2.5\text{ V}$	$V_{CC} = 3.3\text{ V}$	UNIT
				TYP	TYP	TYP	
$C_{pd}$	Power dissipation capacitance per buffer/driver	Outputs enabled	$f = 10\text{ MHz}$	63	56	31	pF
		Outputs disabled		3	3	3	

## PARAMETER MEASUREMENT INFORMATION



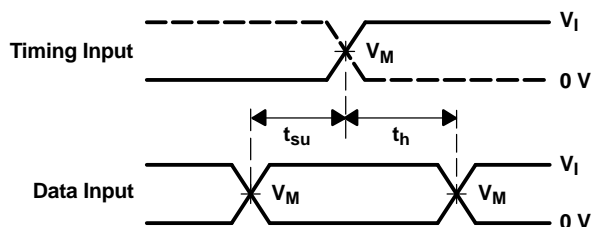
LOAD CIRCUIT

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

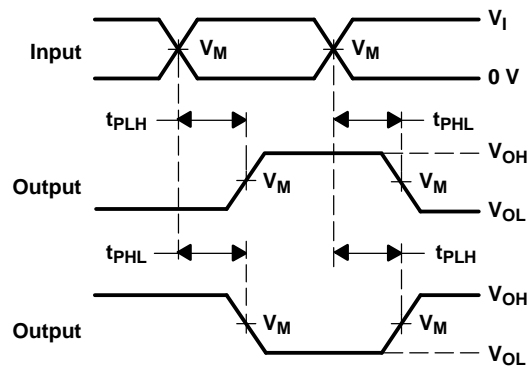
$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t_r/t_f$					
$1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k $\Omega$	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 $\Omega$	0.15 V
2.7 V	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
$3.3\text{ V} \pm 0.3\text{ V}$	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V



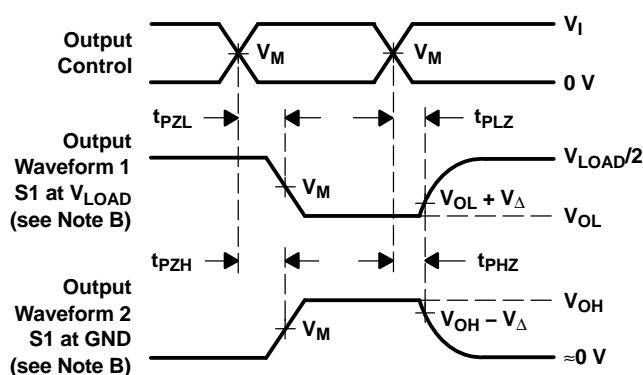
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ .
  - The outputs are measured one at a time, with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9759401Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9759401Q2A SNJ54LVC 540AFK	<a href="#">Samples</a>
5962-9759401QRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9759401QR A SNJ54LVC540AJ	<a href="#">Samples</a>
5962-9759401QSA	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-9759401QS A SNJ54LVC540AW	<a href="#">Samples</a>
SN74LVC540ADBLE	OBSOLETE	SSOP	DB	20		TBD	Call TI	Call TI	-40 to 85		
SN74LVC540ADBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC540A	<a href="#">Samples</a>
SN74LVC540ADBRE4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC540A	<a href="#">Samples</a>
SN74LVC540ADBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC540A	<a href="#">Samples</a>
SN74LVC540ADGVR	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC540A	<a href="#">Samples</a>
SN74LVC540ADGVRE4	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC540A	<a href="#">Samples</a>
SN74LVC540ADGVRG4	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC540A	<a href="#">Samples</a>
SN74LVC540ADW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC540A	<a href="#">Samples</a>
SN74LVC540ADWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC540A	<a href="#">Samples</a>
SN74LVC540ADWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC540A	<a href="#">Samples</a>
SN74LVC540ADWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC540A	<a href="#">Samples</a>
SN74LVC540ADWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC540A	<a href="#">Samples</a>
SN74LVC540ADWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC540A	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC540ANSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC540A	<a href="#">Samples</a>
SN74LVC540ANSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC540A	<a href="#">Samples</a>
SN74LVC540ANSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC540A	<a href="#">Samples</a>
SN74LVC540APW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC540A	<a href="#">Samples</a>
SN74LVC540APWE4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC540A	<a href="#">Samples</a>
SN74LVC540APWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC540A	<a href="#">Samples</a>
SN74LVC540APWLE	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI	-40 to 85		
SN74LVC540APWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC540A	<a href="#">Samples</a>
SN74LVC540APWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC540A	<a href="#">Samples</a>
SN74LVC540APWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC540A	<a href="#">Samples</a>
SN74LVC540APWT	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC540A	<a href="#">Samples</a>
SN74LVC540APWTE4	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC540A	<a href="#">Samples</a>
SN74LVC540APWTG4	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LC540A	<a href="#">Samples</a>
SNJ54LVC540AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9759401Q2A SNJ54LVC 540AFK	<a href="#">Samples</a>
SNJ54LVC540AJ	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9759401QR A SNJ54LVC540AJ	<a href="#">Samples</a>
SNJ54LVC540AW	ACTIVE	CFP	W	20	1	TBD	Call TI	N / A for Pkg Type	-55 to 125	5962-9759401QS A SNJ54LVC540AW	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:



**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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#### **OTHER QUALIFIED VERSIONS OF SN54LVC540A, SN74LVC540A :**

● Catalog: [SN74LVC540A](#)

● Automotive: [SN74LVC540A-Q1](#), [SN74LVC540A-Q1](#)

● Enhanced Product: [SN74LVC540A-EP](#), [SN74LVC540A-EP](#)

● Military: [SN54LVC540A](#)

**NOTE: Qualified Version Definitions:**

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC540ADBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LVC540ADGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC540ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74LVC540ANSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1
SN74LVC540APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74LVC540APWT	TSSOP	PW	20	250	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC540ADBR	SSOP	DB	20	2000	367.0	367.0	38.0
SN74LVC540ADGVR	TVSOP	DGV	20	2000	367.0	367.0	35.0
SN74LVC540ADWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74LVC540ANSR	SO	NS	20	2000	367.0	367.0	45.0
SN74LVC540APWR	TSSOP	PW	20	2000	367.0	367.0	38.0
SN74LVC540APWT	TSSOP	PW	20	250	367.0	367.0	38.0

J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only.
  - Falls within Mil-Std 1835 GDFP2-F20

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

24 PINS SHOWN

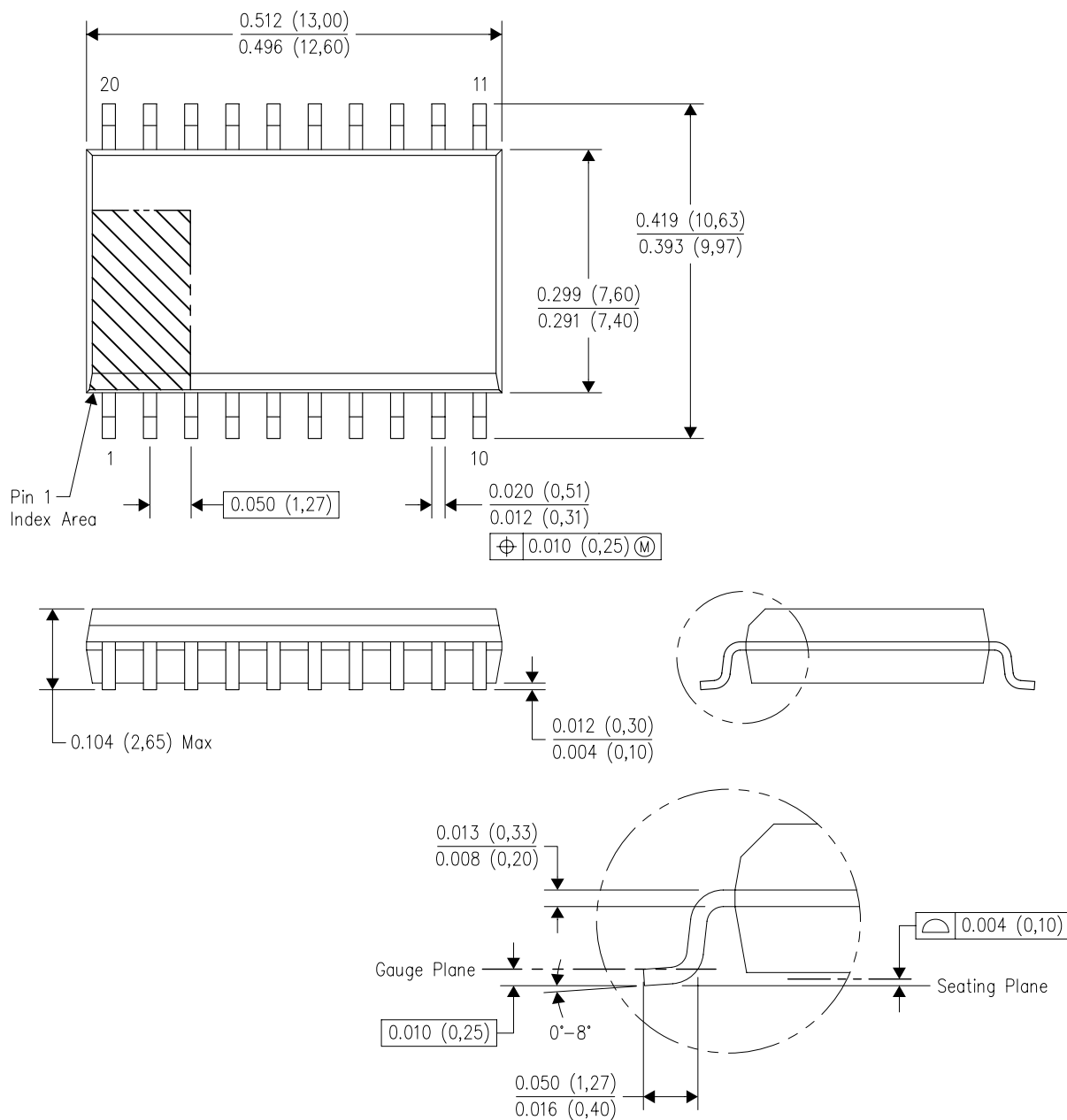


- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194



DW (R-PDSO-G20)

## PLASTIC SMALL OUTLINE



4040000-4/G 01/11

- NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.  
B. This drawing is subject to change without notice.  
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
D. Falls within JEDEC MS-013 variation AC.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



4040064-5/G 02/11

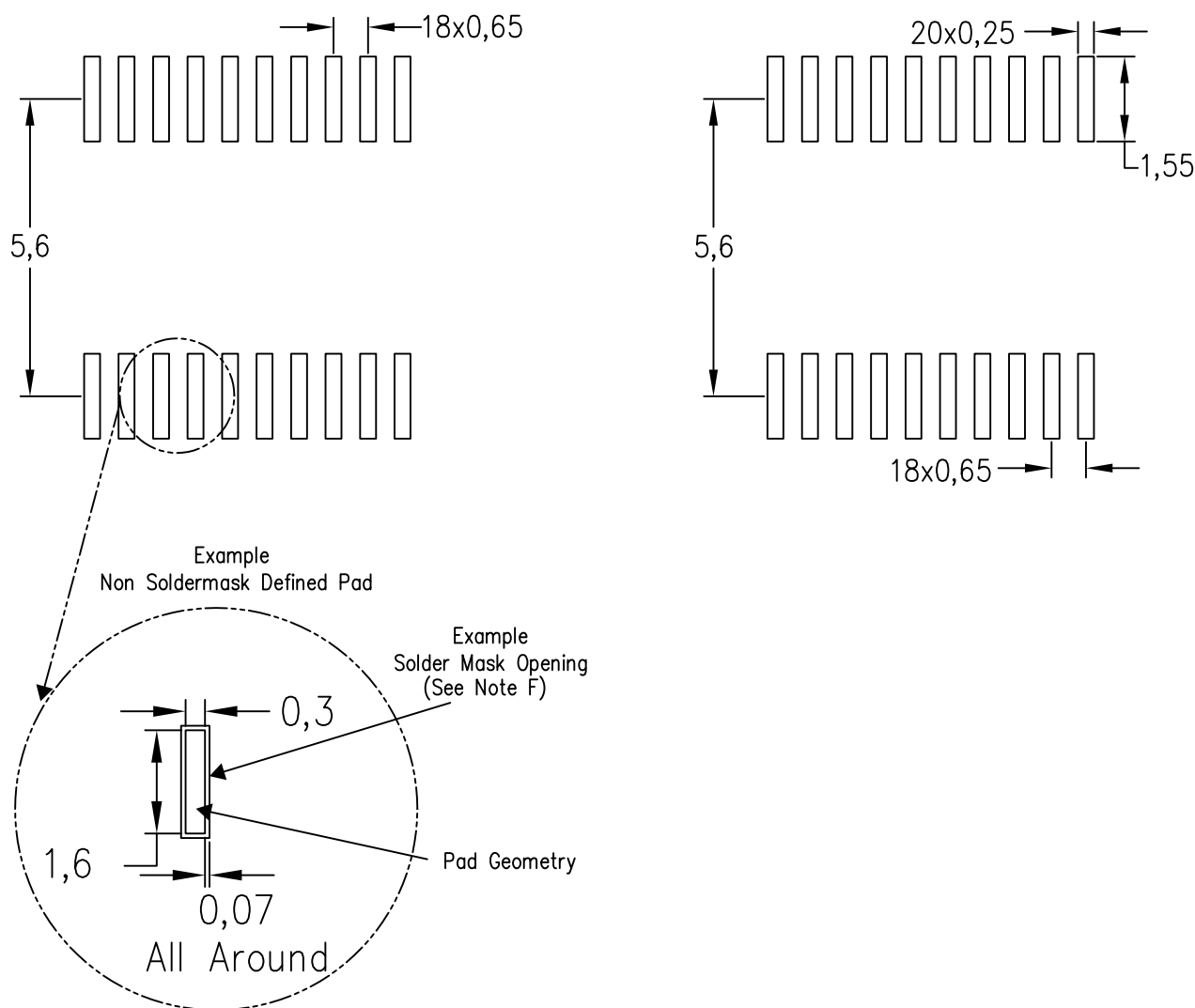
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

Example Board Layout

Based on a stencil thickness  
of .127mm (.005inch).



4211284-5/F 12/12

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

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