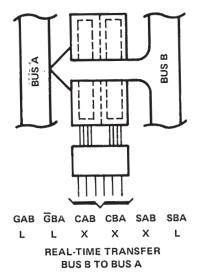
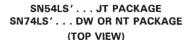
- Bus Transceivers/Registers
- Independent Registers and Enables for A and B Buses
- Multiplexed Real-Time and Stored Data
- Choice of True and Inverting Data Paths
- Choice of 3-State or Open-Collector Outputs to A Bus
- Dependable Texas Instruments Quality and Reliability

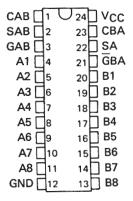
DEVICE	A OUTPUT	B OUTPUT	LOGIC
'LS651	3-State	3-State	Inverting
'LS652	3-State	3-State	True
'LS653	Open-collector	3-State	Inverting

description

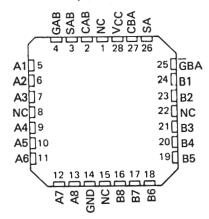
These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Enable GAB and $\overline{G}BA$ are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether realtime or stored data is transferred. A low input level selects real-time data, and a high selects stored data. The following examples demonstrate the four fundamental bus-management functions that can be performed with the 'LS651, 'LS652, and 'LS653.



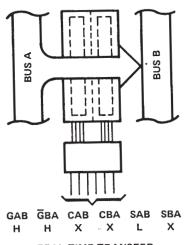




SN54LS'...FK PACKAGE (TOP VIEW)



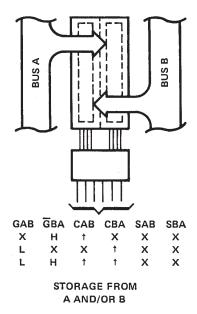
NC - No internal connection

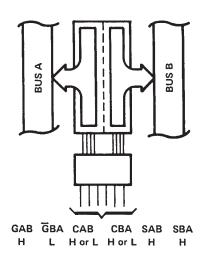


REAL-TIME TRANSFER BUS A TO BUS B



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TRANSFER STORED DATA TO A AND/OR B

Data on the A or B data bus, or both, can be stored in the internal D flip-flop by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB or SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and $\overline{G}BA$. In this configuration each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

The SN54LS651 through SN54LS653 are characterized for operation over the full military temperature range of $-55\,^{\circ}$ C to 125 °C. The SN74LS651 through SN74LS653 are characterized for operation from 0 °C to 70 °C.

FUNCTION TABLE

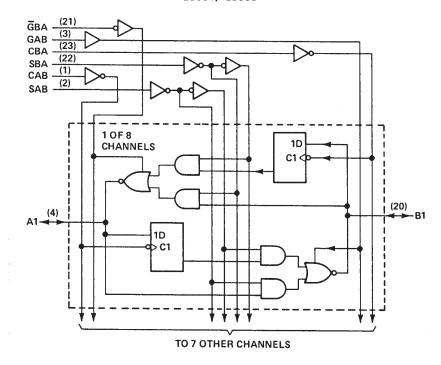
		INP	UTS			DAT	A I/O*	OPERATION C	R FUNCTION
GAB	ĞВА	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	'LS651, 'LS653	'LS652, 'LS654
L	Н	H or L	H or L	Х	Х	1	1	Isolation	Isolation
L	Н	†	1	Х	X	Input	Input	Store A and B Data	Store A and B Data
X	Н	†	H or L	Х	Х	Input	Not specified	Store A, Hold B	Store A, Hold B
Н	Н	1	†	Х	X	Input	Output	Store A in both registers	Store A in both registers
L	Х	H or L	†	Х	Х	Not specified	Input	Hold A, Store B	Hold A, Store B
L	L	†	†	Х	Х	Output	Input	Store B in both registers	Store B in both registers
L	L	Х	X	Х	L	Output	Input	Real-Time B Data to A Bus	Real-Time B Data to A Bus
L	L	Х	H or L	Х	Н	Output	Input	Stored B Data to A Bus	Stored B Data to A Bus
Н	Н	Х	X	L	Х	Input	Output	Real-Time A Data to B Bus	Real-Time A Data to B Bus
Н	Н	HorL	X	Н	Х	Прис	Output	Stored A Data to B Bus	Stored A Data to B Bus
Н.	· L	Horl	H or L	Н	н	Output	Output	Stored A Data to B Bus and	Stored A Data to B Bus and
	-	1101 2				Output	Output	Stored B Data to A Bus	Stored B Data to A Bus

^{*} The data output functions may be enabled or disabled by various signals at the GAB and GBA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

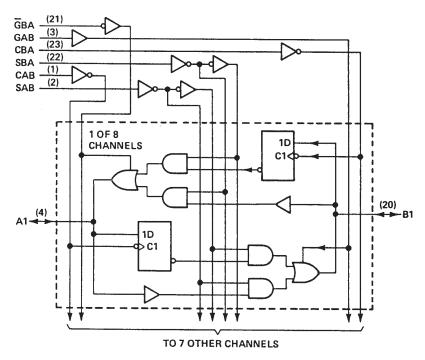


logic diagrams (positive logic)

'LS651, 'LS653



'LS652

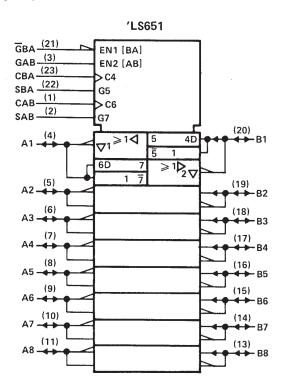


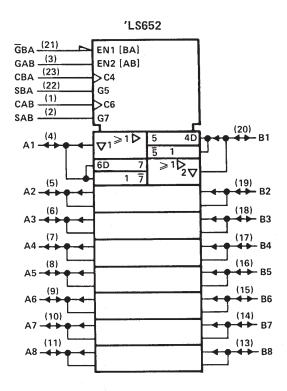
Pin numbers shown are for DW, JT or NT packages.

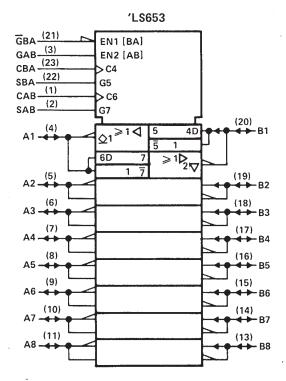


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logic symbols†







[†]This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, JT, or NT packages.



SN54LS651, SN54LS652, SN74LS651, SN74LS652 OCTAL BUS TRANSCEIVERS AND REGISTERS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC	1
Input voltage: Control inputs	1
I/O ports	
Operating free-air temperature range: SN54LS651, SN54LS652 -55° C to 125°	С
SN74LS651, SN74LS652	3
Storage temperature range $\dots - 65^{\circ}C$ to 150°	С

recommended operating conditions

				N54LS6 N54LS6			N74LS6		UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	ONT
Vcc	Supply voltage		4.5	5	5,5	4.75	5	5.25	V
VIH	High-level input voltage	2	-		2			V	
VIL	Low-level input voltage			0.7			0.8	V	
ТОН	High-level output current				- 12			15	mA
loL	Low-level output current				12			24	mA
		CBA or CAB high	15			15			
tw	Pulse duration	CBA or CAB low	15			15			ns
		Data high or low	15			15			
t _{su}	Setup time before CAB† or CBA†	A or B	15			15			ns
th	Hold time after CAB† or CBA†	A or B	0			0			ns
TA	Operating free-air temperature		- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

P.A	ARAMETER	Т	TEST CONDITIONS [†]				51 52 MAX	SN	174LS65	52	UNIT	
Vuc		V MIN	V _{CC} = MIN, I _I = - 18 mA					MIN	TYP‡			
VIK		ACC = INITIA'	11 = - 18 mA		<u> </u>		- 1.5			- 1.5	V	
		V _{CC} = MIN,	V _{1H} = 2 V,	I _{OH} = - 3 mA	2.4	3.4		2.4	3.4			
Vон		$V_{II} = MAX,$	- 111	I _{OH} = - 12 mA	2						V	
		1		l _{OH} = - 15 mA				2				
VOL		V _{CC} = MIN,	$V_{IH} = 2 V$	IOL = 12 mA		0.25	0.4		0.25	0.4	V	
101		VIL = MAX,		IOL = 24 mA					0.35	0.5	1 °	
I _f	Control inputs	V _{CC} = MAX,	V _I = 7 V				0.1			0.1		
''	A or B ports	$V_{CC} = MAX$,	V ₁ = 5.5 V				0.1			0.1	mA	
ΙΉ	Control inputs	V MAY	V = 0.7.V				20			20		
'IH	A or B ports¶	VCC = MAX,	$V_1 = 2.7 \text{ V}$				20			20	μA	
1	Control inputs	VMAY	V = 0.4 V				- 0.4			- 0.4		
IIL	A or B ports¶	V _{CC} = MAX,	V j = 0.4 V				- 0.4			- 0.4	mA	
los§		V _{CC} = MAX,	V _O = 0 V		- 40		- 225	- 40		- 225	mA	
				Outputs high		95	145		95	145		
	LS651			Outputs low		103	165		103	165	1	
las		\/a== MAY		Outputs disabled		103	165		103	165	1 .	
Icc		V _{CC} = MAX		Outputs high		95	145		95	145	mA	
	LS652			Outputs low		103	165		103	165	1	
				Outputs disabled		120	180		120	180	1	

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

 $[\]P$ For I/O ports, the parameters I $_{IH}$ and I $_{IL}$ include the off-state output current.



 $^{^{\}ddagger}$ All typical values are at V_{CC} = 5 V, T_A = 25 °C. $^{\$}$ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

SN54LS651, SN54LS652, SN74LS651, SN74LS652 OCTAL BUS TRANSCEIVERS AND REGISTERS

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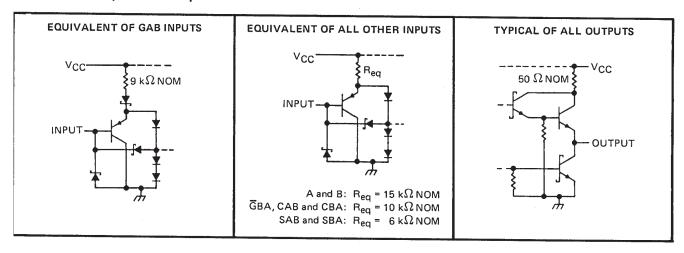
switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

PARAMETER	FROM	то	TEST COME	NITIONS		'LS651			'LS652		
	(INPUT)	(OUTPUT)	TEST CONE	MIN	TYP	MAX	MIN	TYP	MAX	דומט	
^t PLH	Clock	Bus				14	24		15	25	ns
tPHL	GIOCK	bus				23	35		24	36	ns
^t PLH	Bus	Bus				9	18		12	18	ns
^t PHL	Dus	Bus				20	30		13	20	ns
^t PLH	Select, with					31	.47		23	35	ns
^t PHL	bus input high [†]	0	R _L = 667 Ω,	C _L = 45 pF,		22	33		21	32	ns
^t PLH	Select, with	Bus	See Note 2	-		23	35		33	50	ns
^t PHL	low†					19	30		15	23	ns
^t PZH	Ğва	A Bus				29	44		30	45	ns
^t PZL	GBA	A Bus				40	60		36	54	ns
^t PZH	GAB	B Bus				19	29		20	30	ns
^t PZL	GAB	b bus				26	40		25	38	ns
^t PHZ	Ğва	Δ Β			1	25	. 38		25	38	ns
^t PLZ	GBA	A Bus	$R_L = 667 \Omega$,	Cլ = 5 pF,		19	30		19	30	ns
^t PHZ	GAB	P. P. vo	See Note 2			25	38		25	38	ns
^t PLZ	GAB	B Bus				19	30		19	30	ns

tpLH = propagation delay time, low-to-high-level output.

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

schematics of inputs and outputs



tpHL = propagation delay time, high-to-low-level output

tpzH = output enable time to high level

tpzL = output enable time to low level

tpHZ = output disable time from high level

tpLZ = output disable time from low level tpLZ = output disab

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC
Input voltage: All inputs and A I/O ports
B I/O ports
Operating free-air temperature range: SN54LS65355°C to 125°C
SN74LS653 0°C to 70°C
Storage temperature range65°C to 150°C

recommended operating conditions

			s	N54LS6	553	SI	N74LS6	53	UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
Vcc	Supply voltage		4.5	5	5.5	4.75	5	5.25	٧
VIH	High-level input voltage	2			2			V	
VIL	Low-level input voltage			0.7			8.0	V	
Voн	High-level output voltage	A ports			5.5			5.5	V
Іон	High-level output current	B ports		,	- 12			- 15	mA
loL	Low-level output current				12			24	mA
		CBA or CAB high	15			15			
t _W	Pulse duration	CBA or CAB low	30			30			ns
		Data high or low	30			30			
t _{su}	Setup time	A or B	15	-		15			ns
-su	before CAB↑ or CBA↑	7, 6, 5							
t.	Hold time	A or B	0			0			ns
th	after CAB† or CBA†	7013	0						
TA	Operating free-air temperature		- 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		Т	EST CONDITIO	_{NS} †	SI	N54LS6	53	s	N74LS6	553	UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
VIK		V _{CC} = MIN,	I ₁ = - 18 mA				- 1.5			- 1.5	V
		V _{CC} = MIN,	V _{IH} = 2 V,	I _{OH} = - 3 mA	2.4	3.4		2.4	3,4		
Voн	B ports	VIL = MAX		IOH = - 12 mA	2						V
				10H = - 15 mA				2			İ
ЮН	A ports	V _{CC} = MIN,	$V_{OH} = 5.5 V$				0.1			0.1	mA
Val		V _{CC} = MIN,	V _{IH} = 2 V,	IOL = 12 mA		0.25	0.4		0.25	0.4	V
VOL		VIL = MAX		IOL = 24 mA					0.35	0.5	1 *
1 ₁	Control inputs	V _{CC} = MAX,	V _I = 7 V				0.1			0.1	mA
'1	A or B ports	V _{CC} = MAX,	V ₁ = 5.5 V				0.1			0.1	1111/4
Leve	Control inputs	V _{CC} = MAX,	V ₁ = 2.7 V				20			20	μΑ
ΙΗ	A or B ports	VCC - WAX,	V - 2.7 V				20			20	μ^
IL	Control inputs	V _{CC} = MAX,	V ₁ = 0.4 V				- 0.4			- 0.4	mA
11	A or B ports¶	VCC - WAX,					- 0.4			- 0.4]
los§	B ports	V _{CC} = MAX,	V _O = 0 V		- 40		- 225	- 40		- 225	mA
				Outputs high		95	145		95	145	
	LS653			Outputs low		103	165		103	165	
Icc		V _{CC} = MAX	Outputs disabled			103	165		103	165	mA mA
.00		T CC - WAX		Outputs high		95	145		95	145] '''^
	LS654			Outputs low		105	170		105	170	
				Outputs disabled		120	180		120	180	

 $^{^{\}dagger}$ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions. ‡ All typical values are at V_{CC} = 5 V, T_A = 25 °C.

 $[\]P$ For I/O ports, the parameters $I_{\mbox{\scriptsize IH}}$ and $I_{\mbox{\scriptsize IL}}$ include the off-state output current.



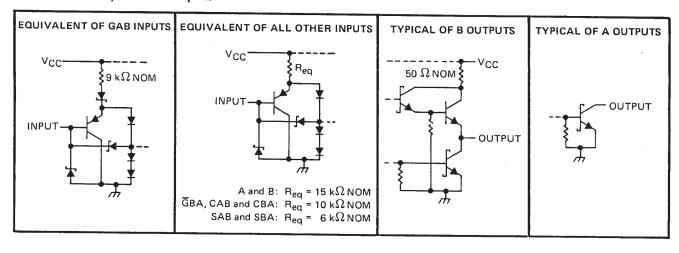
Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25 °C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
^t PLH	СВА	A D			25	38	
tPHL	СВА	A Bus			26	39	ns
tPLH	САВ	B Bus	- -		15	23	
tpHL	CAB	B bus			24	36	ns
^t PLH	A Bus	B Bus	1		10	18	
t _{PHL}	// Dus	D Dus			20	30	กร
^t PLH	B Bus	A Bus			21	32	
^t PHL	5 543	A Dus			16	24	ns
^t PLH	SBA†	A D	$R_L = 667 \Omega$, $C_L = 45 pF$,		38	57	
^t PHL	(with B high)	A Bus	See Note 2		26	39	ns
tplH	SBA [†]		1		34	51	
^t PHL	(with B low)	A Bus			23	35	ns
^t PLH	SAB [†]		1		32	48	
t _{PHL}	(with A high)	B Bus			22	33	ns
tPLH	SAB [†]		-				
tPHL	(with A low)	B Bus			24	36 30	ns
tPLH			1		23	35	
tPHL	Ğва	A Bus			37	55	ns
^t PZH	0.15				19	29	
tPZL	GAB	B Bus	$R_L = 667 \Omega$, $C_L = 5 pF$,		25	38	ns
^t PHZ	CAR	5.5	See Note 2		26	39	
tPLZ	GAB	B Bus			19	29	ns

[†]These parameters are measured with the internal output state of the storage register opposite to that of the bus input. NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

schematics of inputs and outputs







20-Aug-2011

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN74LS651DW	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI	
SN74LS651DWR	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI	
SN74LS651NT	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI	
SN74LS652DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS652DWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS652DWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74LS652NT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	
SN74LS652NTE4	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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20-Aug-2011

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www.ti.com/security