

SN74HC166A-Q1

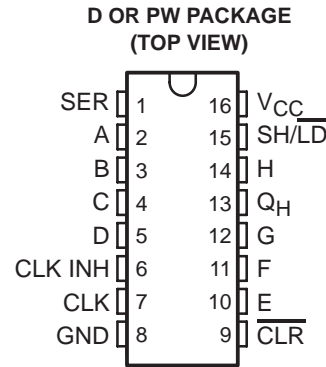
8-BIT PARALLEL-LOAD SHIFT REGISTER

SCLS538A – AUGUST 2003 – REVISED APRIL 2008

- Qualified for Automotive Applications
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 80- μ A Max I_{CC}
- Typical t_{pd} = 13 ns
- ± 4 -mA Output Drive at 5 V
- Low Input Current of 1 μ A Max
- Synchronous Load
- Direct Overriding Clear
- Parallel-to-Serial Conversion

description/ordering information

This parallel-in or serial-in, serial-out register features gated clock (CLK, CLK INH) inputs and an overriding clear (CLR) input. The parallel-in or serial-in modes are established by the shift/load (SH/ \overline{LD}) input. When high, SH/ \overline{LD} enables the serial (SER) data input and couples the eight flip-flops for serial shifting with each clock (CLK) pulse. When low, the parallel (broadside) data inputs are enabled, and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high-level edge of CLK through a 2-input positive-NOR gate, permitting one input to be used as a clock-enable or clock-inhibit function. Holding either CLK or CLK INH high inhibits clocking; holding either low enables the other clock input. This allows the system clock to be free running, and the register can be stopped on command with the other clock input. CLK INH should be changed to the high level only when CLK is high. \overline{CLR} overrides all other inputs, including CLK, and resets all flip-flops to zero.



ORDERING INFORMATION†

T _A	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOIC – D	Tape and reel	SN74HC166AIDRQ1	HC166AI
	TSSOP – PW	Tape and reel	SN74HC166AIPWRQ1	HC166AI

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at <http://www.ti.com>.

‡ Package drawings, thermal data, and symbolization are available at <http://www.ti.com/packaging>.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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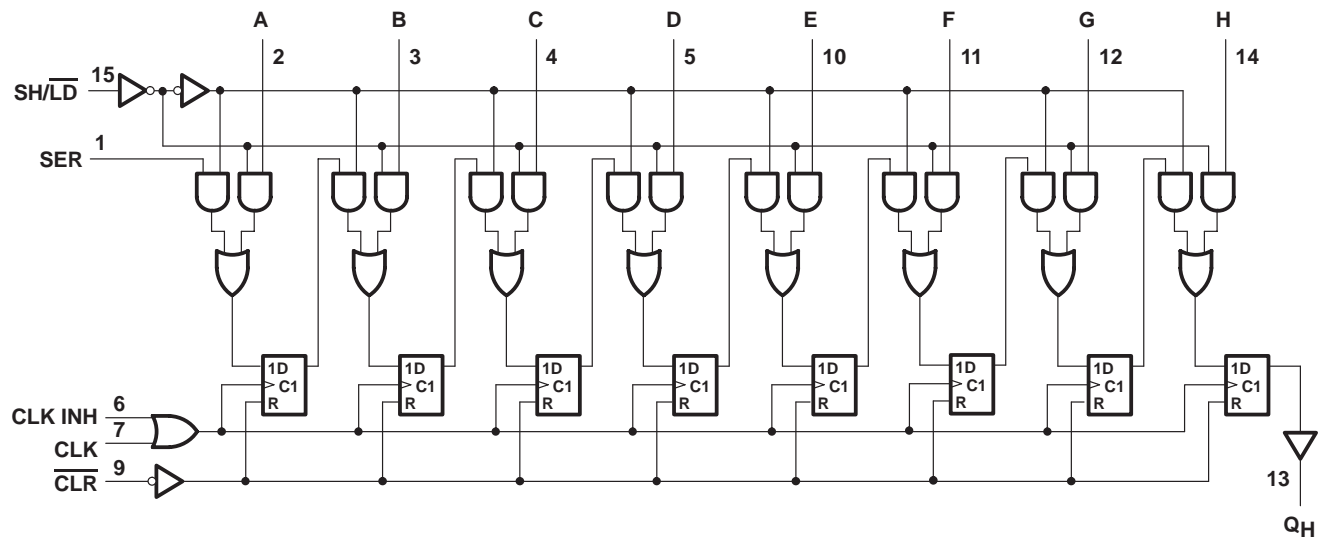
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FUNCTION TABLE

INPUTS						OUTPUTS		
						INTERNAL		QH
CLR	SH/LD	CLK INH	CLK	SER	PARALLEL A . . . H	QA	QB	
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	QA0	QB0	QH0
H	L	L	↑	X	a . . . h	a	b	h
H	H	L	↑	H	X	H	QAn	QGn
H	H	L	↑	L	X	L	QAn	QGn
H	X	H	↑	X	X	QA0	QB0	QH0

logic diagram (positive logic)

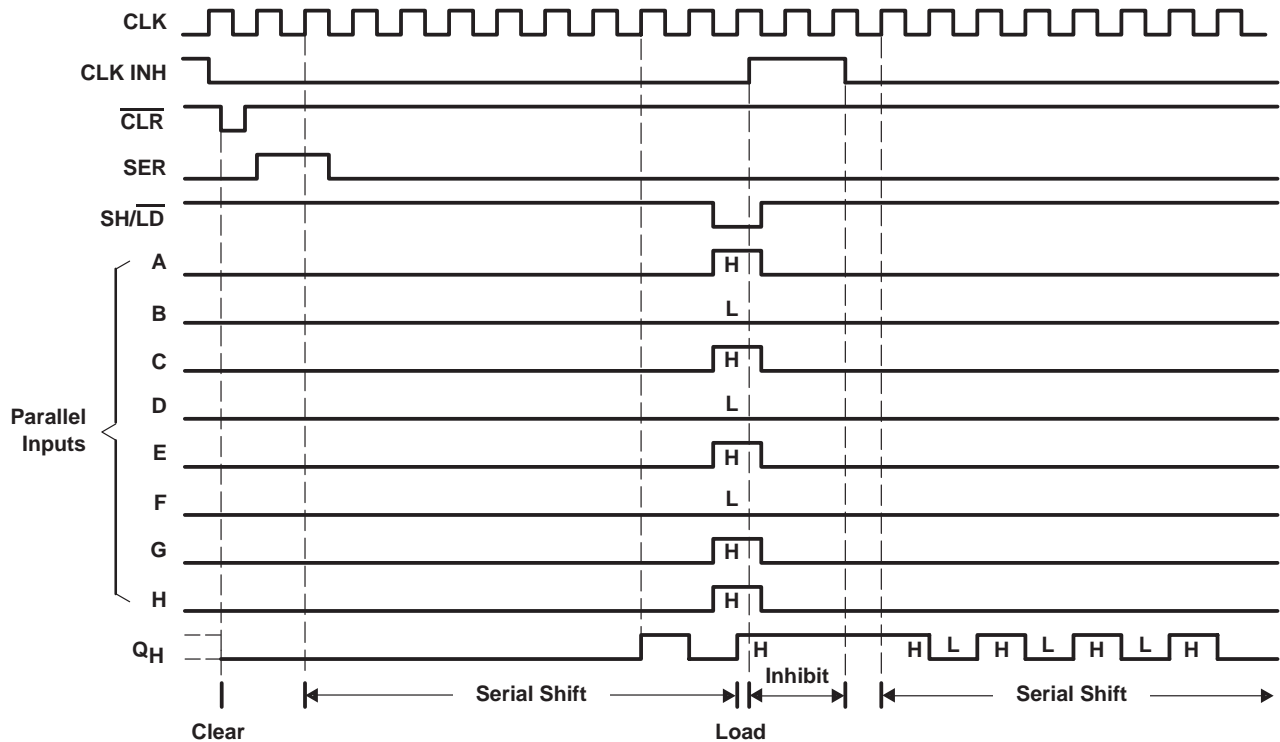


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typical clear, shift, load, inhibit, and shift sequence



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package	73°C/W
PW package	108°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51-7.

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recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	2	5	6	V
V_{IH}	High-level input voltage	$V_{CC} = 2\text{ V}$	1.5		V
		$V_{CC} = 4.5\text{ V}$	3.15		
		$V_{CC} = 6\text{ V}$	4.2		
V_{IL}	Low-level input voltage	$V_{CC} = 2\text{ V}$		0.5	V
		$V_{CC} = 4.5\text{ V}$		1.35	
		$V_{CC} = 6\text{ V}$		1.8	
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
$\Delta t/\Delta v^\dagger$	Input transition rise/fall time	$V_{CC} = 2\text{ V}$		1000	ns
		$V_{CC} = 4.5\text{ V}$		500	
		$V_{CC} = 6\text{ V}$		400	
T_A	Operating free-air temperature	-40		85	°C

[†] If this device is used in the threshold region (from $V_{IL\text{max}} = 0.5\text{ V}$ to $V_{IH\text{min}} = 1.5\text{ V}$), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at $t_t = 1000\text{ ns}$ and $V_{CC} = 2\text{ V}$ does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	$V_I = V_{IH}\text{ or }V_{IL}$	$I_{OH} = -20\text{ }\mu\text{A}$	2 V	1.9	1.998	1.9		V
			4.5 V	4.4	4.499	4.4		
			6 V	5.9	5.999	5.9		
		$I_{OH} = -4\text{ mA}$	4.5 V	3.98	4.3	3.84		
		$I_{OH} = -5.2\text{ mA}$	6 V	5.48	5.8	5.34		
V_{OL}	$V_I = V_{IH}\text{ or }V_{IL}$	$I_{OL} = 20\text{ }\mu\text{A}$	2 V		0.002	0.1	0.1	V
			4.5 V		0.001	0.1	0.1	
			6 V		0.001	0.1	0.1	
		$I_{OL} = 4\text{ mA}$	4.5 V		0.17	0.26	0.33	
		$I_{OL} = 5.2\text{ mA}$	6 V		0.15	0.26	0.33	
I_I	$V_I = V_{CC}\text{ or }0$	6 V		± 0.1	± 100		± 1000	nA
I_{CC}	$V_I = V_{CC}\text{ or }0, I_O = 0$	6 V			8		80	μA
C_i		2 V to 6 V		3	10		10	pF

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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V _{CC}	T _A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f _{clock}	Clock frequency	2 V	6		5		MHz
		4.5 V	31		25		
		6 V	36		29		
t _w	$\overline{\text{CLR}}$ low	2 V	100		125		ns
		4.5 V	20		25		
		6 V	17		21		
	CLK high or low	2 V	80		100		
		4.5 V	16		20		
		6 V	14		17		
t _{su}	SH/ $\overline{\text{LD}}$ high before CLK↑	2 V	145		180		ns
		4.5 V	29		36		
		6 V	25		31		
	SER before CLK↑	2 V	80		100		
		4.5 V	16		20		
		6 V	14		17		
	CLK INH low before CLK↑	2 V	100		125		
		4.5 V	20		25		
		6 V	17		21		
	Data before CLK↑	2 V	80		100		
		4.5 V	16		20		
		6 V	14		17		
$\overline{\text{CLR}}$ inactive before CLK↑	2 V	40		50			
	4.5 V	8		10			
	6 V	7		9			
t _h	SH/ $\overline{\text{LD}}$ high after CLK↑	2 V	0		0		ns
		4.5 V	0		0		
		6 V	0		0		
	SER after CLK↑	2 V	5		5		
		4.5 V	5		5		
		6 V	5		5		
	CLK INH high after CLK↑	2 V	0		0		
		4.5 V	0		0		
		6 V	0		0		
Data after CLK↑	2 V	5		5			
	4.5 V	5		5			
	6 V	5		5			

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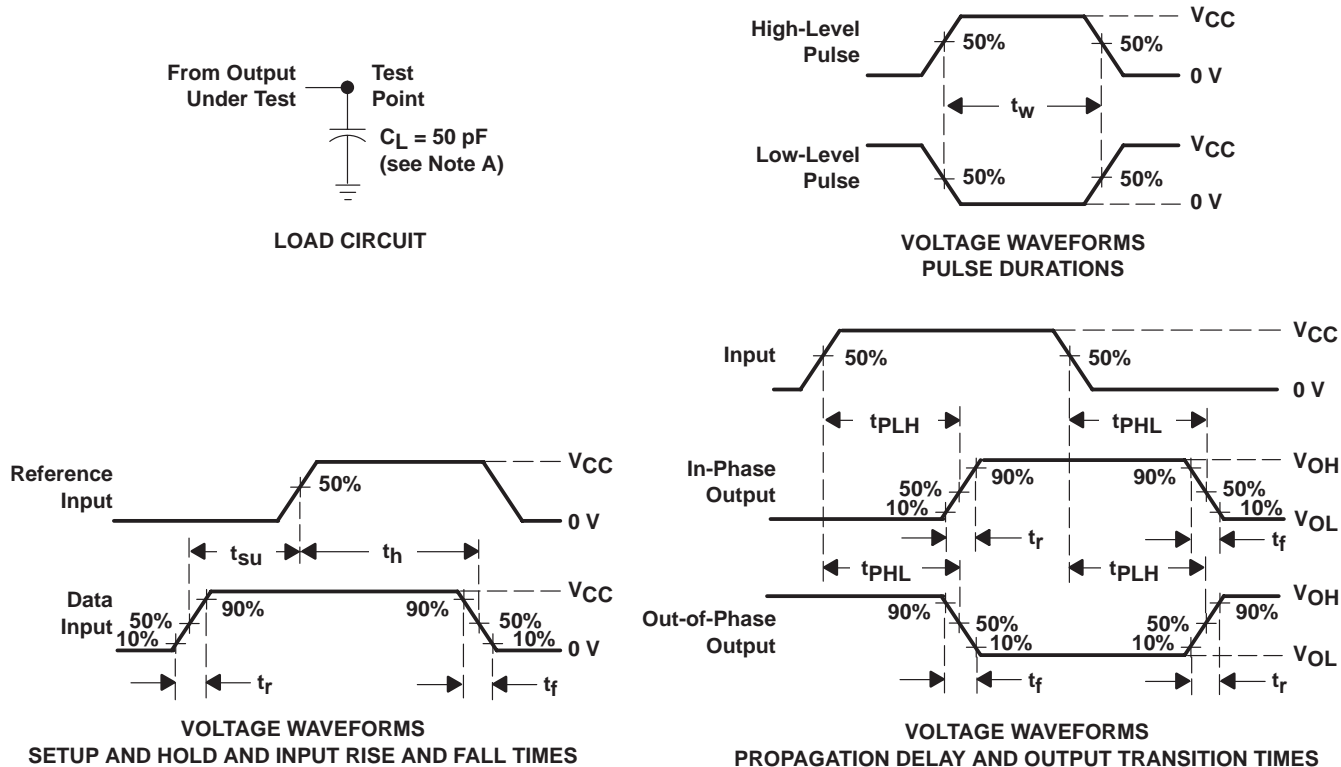
switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
f_{\max}			2 V	6	11		5		MHz
			4.5 V	31	36		25		
			6 V	36	45		29		
t_{PHL}	\overline{CLR}	Q_H	2 V		62	120		150	ns
			4.5 V		18	24		30	
			6 V		13	20		26	
t_{pd}	CLK	Q_H	2 V		75	150		190	ns
			4.5 V		15	30		38	
			6 V		13	26		32	
t_t		Any	2 V		38	75		95	ns
			4.5 V		8	15		19	
			6 V		6	13		16	

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	50	pF

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and test-fixture capacitance.
 - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 6 \text{ ns}$, $t_f = 6 \text{ ns}$.
 - C. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
 - D. The outputs are measured one at a time with one input transition per measurement.
 - E. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
SN74HC166AIDRQ1	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
SN74HC166AIPWRG4Q1	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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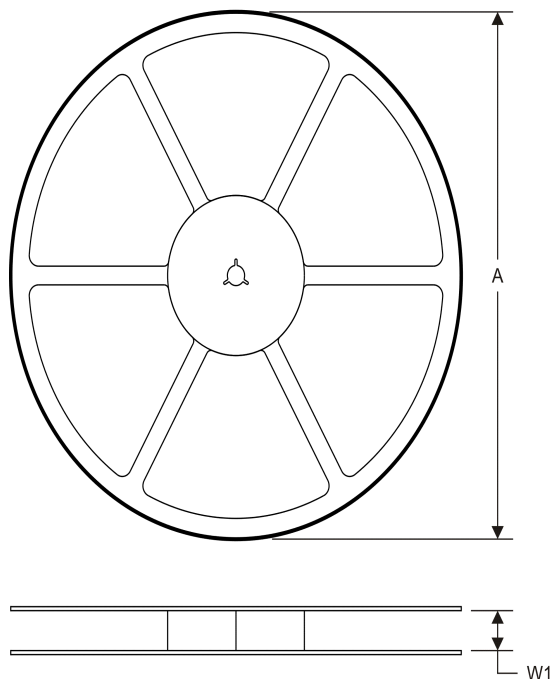
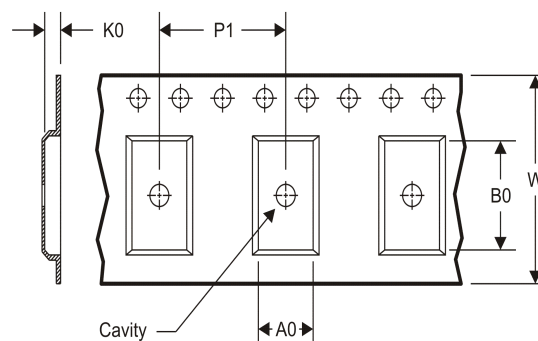
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OTHER QUALIFIED VERSIONS OF SN74HC166A-Q1 :

- Enhanced Product: [SN74HC166A-EP](#)

NOTE: Qualified Version Definitions:

-
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC166AIPWRG4Q1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

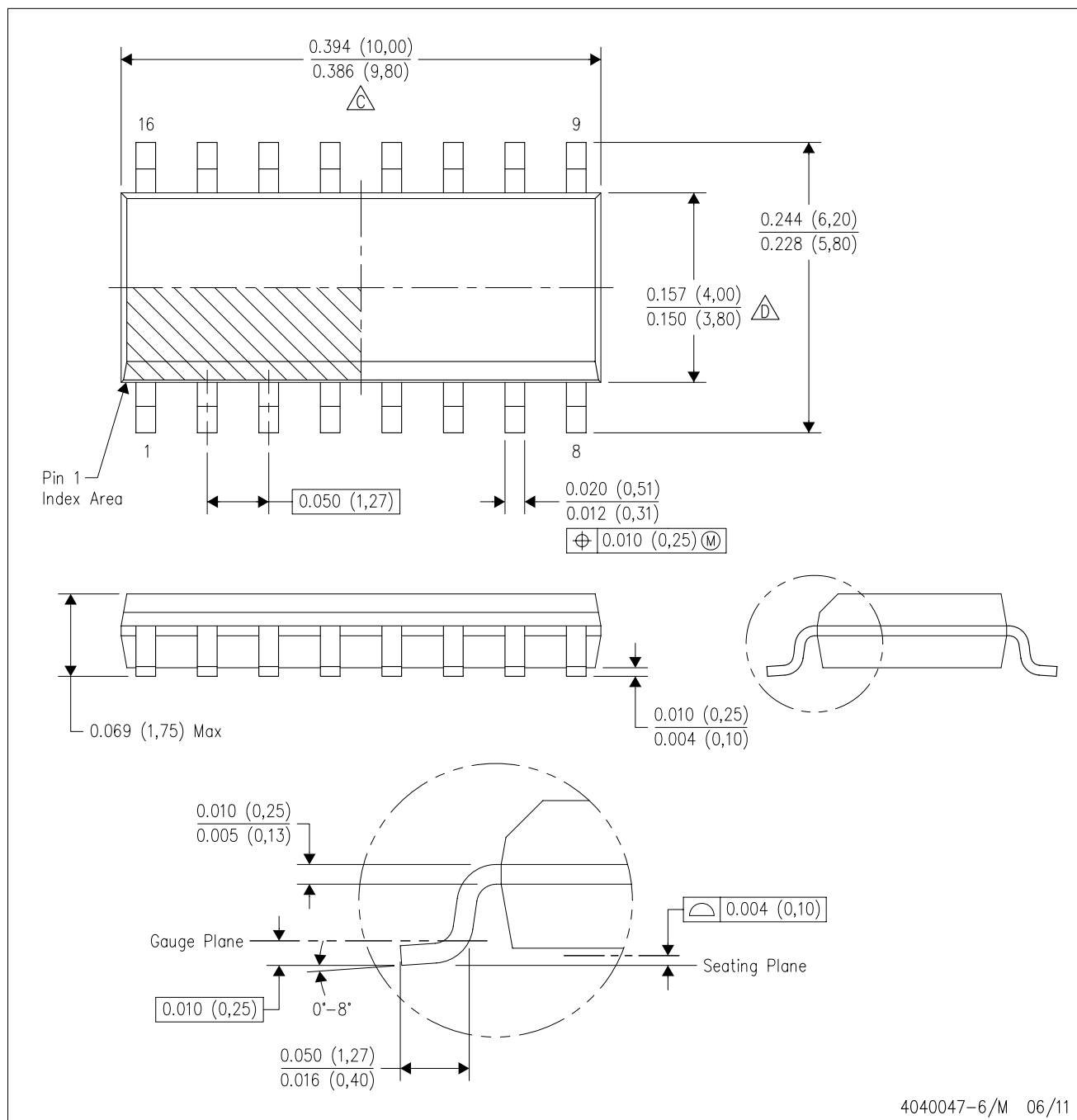


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC166AIPWRG4Q1	TSSOP	PW	16	2000	367.0	367.0	35.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE

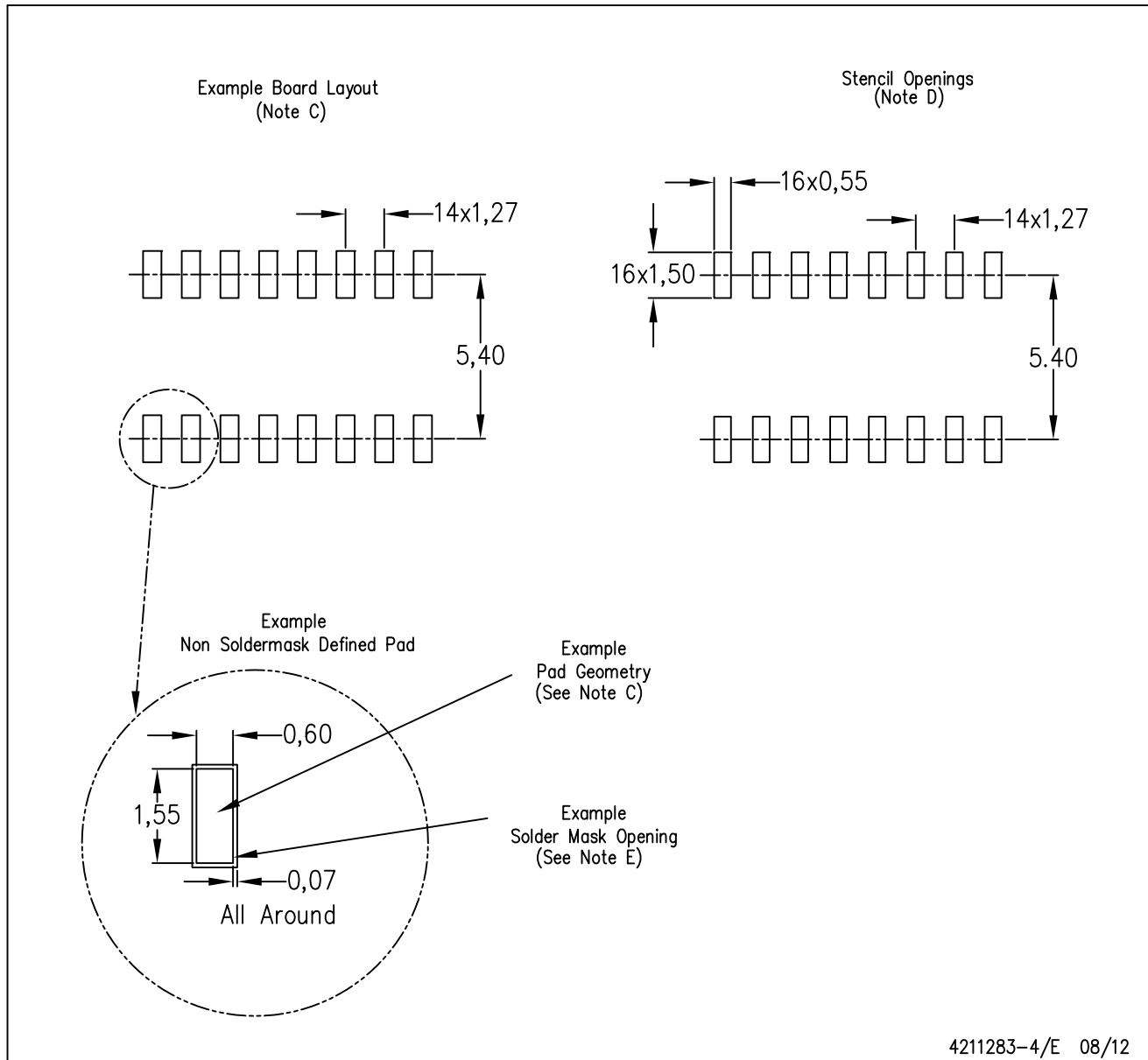


NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

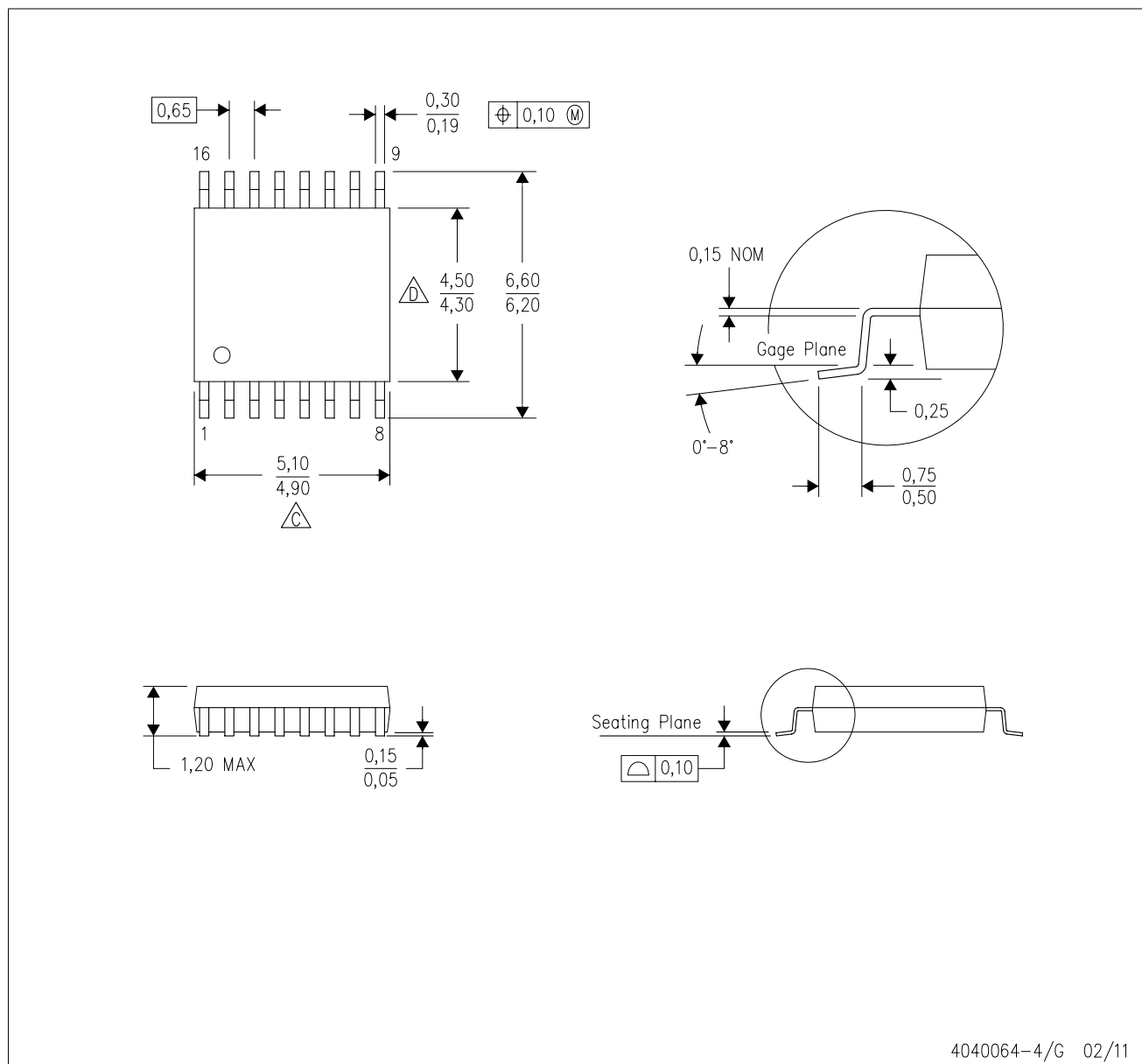
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G16)

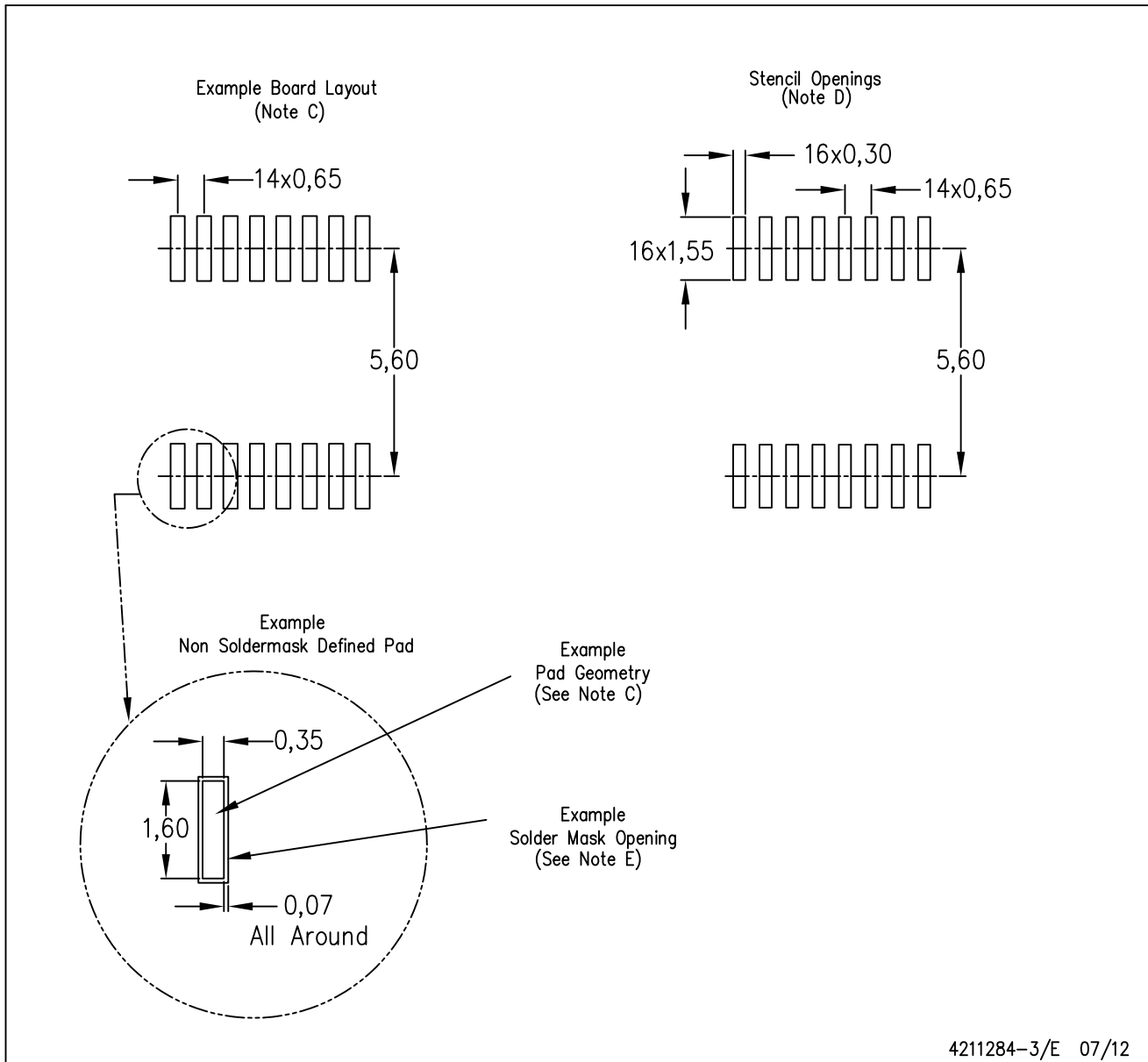
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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