

SN54AS250A, SN74AS250A 1-OF-16 DATA GENERATORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

SDAS137A – DECEMBER 1983 – REVISED DECEMBER 1994

- 4-Line to 1-Line Multiplexers That Can Select 1-of-16 Data Inputs
- Applications:
 - Boolean Function Generator
 - Parallel-to-Serial Converter
 - Data Source Selector
- Buffered 3-State Bus Driver Inputs Permit Multiplexing From n Lines to One Line
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (NT) and Ceramic (JT) 300-mil DIPs

description

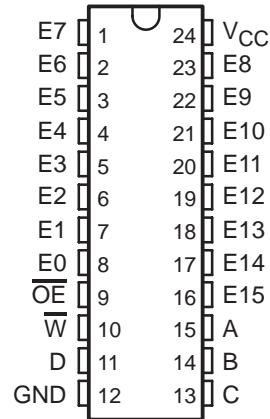
The 'AS250A devices provide full binary decoding to select 1-of-16 data inputs or use sources as an input with an inverting \overline{W} output. The selected sources are buffered with symmetrical propagation delay times. This reduces the possibility of transients occurring at the output.

A buffered output-enable (\overline{OE}) input can be used for n-line to 1-line cascading. Taking \overline{OE} high places the output in the high-impedance state. In the high-impedance state, the output neither loads nor drives the bus lines significantly.

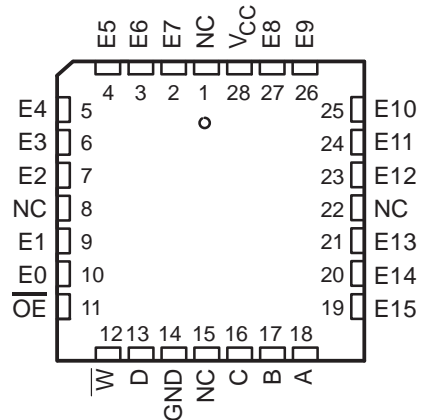
\overline{OE} does not affect the internal operations of the data selector/multiplexer. New data can be set up while the outputs are disabled.

The SN54AS250A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74AS250A is characterized for operation from 0°C to 70°C .

SN54AS250A . . . JT PACKAGE
SN74AS250A . . . DW OR NT PACKAGE
(TOP VIEW)



SN54AS250A . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

SN54AS250A, SN74AS250A

1-OF-16 DATA GENERATORS/MULTIPLEXERS

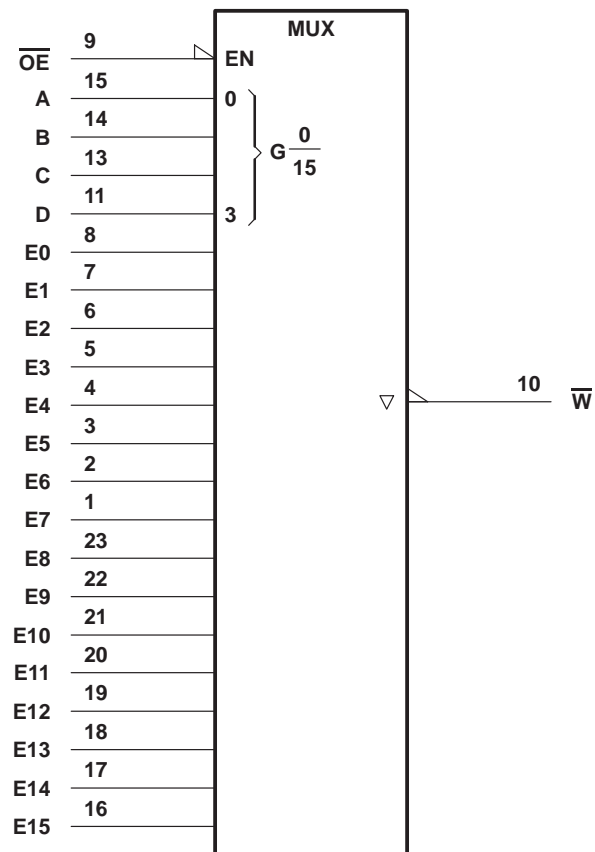
WITH 3-STATE OUTPUTS

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FUNCTION TABLE

INPUTS						OUTPUT \overline{W}
\overline{OE}	A	B	C	D	Ei	
L	L	L	L	L	E0	$\overline{E0}$
L	H	L	L	L	E1	$\overline{E1}$
L	L	H	L	L	E2	$\overline{E2}$
L	H	H	L	L	E3	$\overline{E3}$
L	L	L	H	L	E4	$\overline{E4}$
L	H	L	H	L	E5	$\overline{E5}$
L	L	H	H	L	E6	$\overline{E6}$
L	H	H	H	L	E7	$\overline{E7}$
L	L	L	L	H	E8	$\overline{E8}$
L	H	L	L	H	E9	$\overline{E9}$
L	L	H	L	H	E10	$\overline{E10}$
L	H	H	L	H	E11	$\overline{E11}$
L	L	L	H	H	E12	$\overline{E12}$
L	H	L	H	H	E13	$\overline{E13}$
L	L	H	H	H	E14	$\overline{E14}$
L	H	H	H	H	E15	$\overline{E15}$
H	X	X	X	X	X	Z

logic symbol†



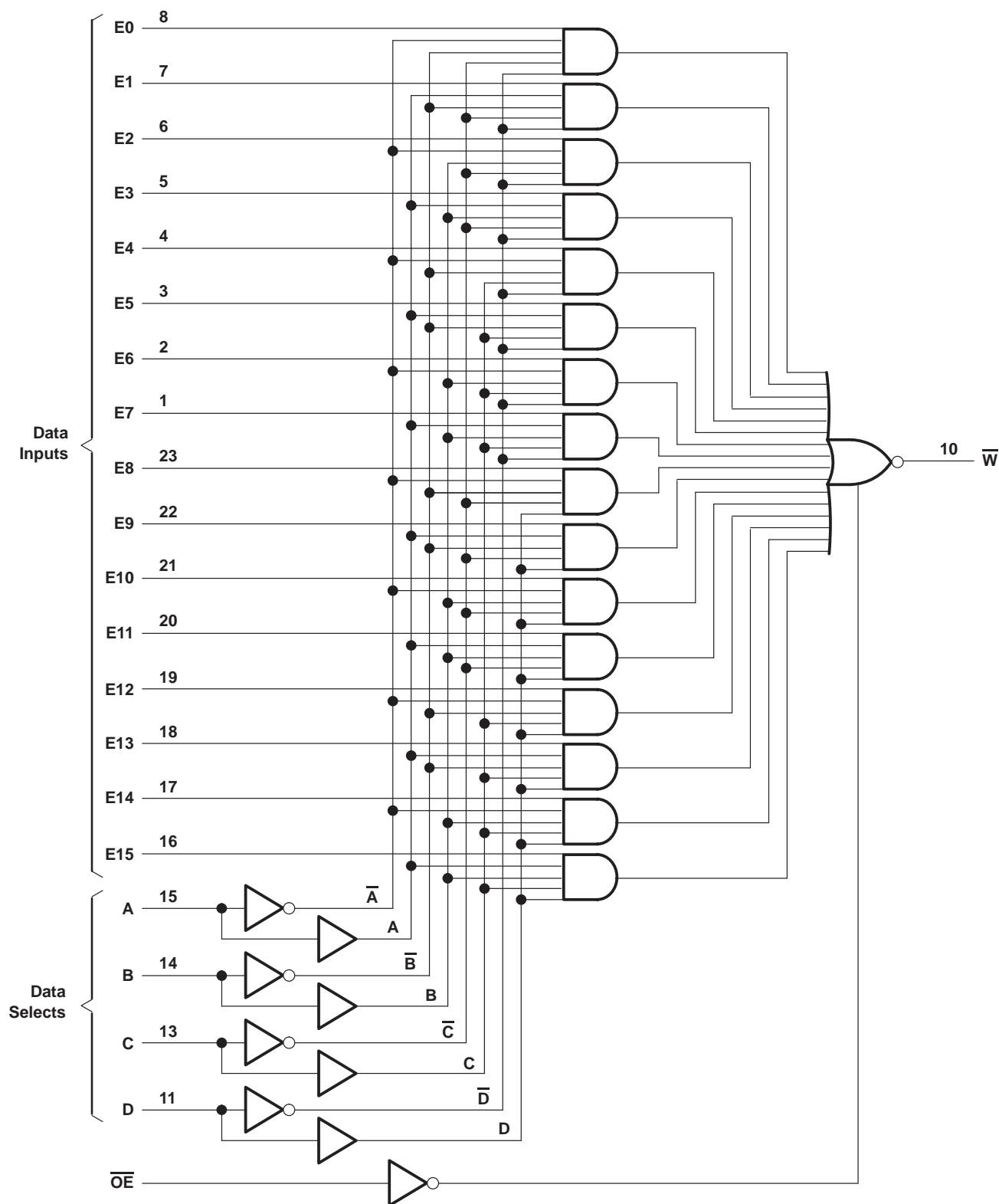
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the DW, JT, and NT packages.

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logic diagram (positive logic)



Pin numbers shown are for the DW, JT, and NT packages.



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Operating free-air temperature range, T_A : SN54AS250A	–55°C to 125°C
SN74AS250A	0°C to 70°C
Storage temperature range	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54AS250A			SN74AS250A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			–12			–15	mA
I_{OL}	Low-level output current			32			48	mA
T_A	Operating free-air temperature	–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS250A			SN74AS250A			UNIT
			MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V_{IK}	$V_{CC} = 4.5$ V,	$I_I = -18$ mA			–1.2			–1.2	V
V_{OH}	$V_{CC} = 4.5$ V to 5.5 V,	$I_{OH} = -2$ mA	$V_{CC} - 2$			$V_{CC} - 2$			V
	$V_{CC} = 4.5$ V	$I_{OH} = -12$ mA	2.4	3.3					
		$I_{OH} = -15$ mA				2.4	3.3		
V_{OL}	$V_{CC} = 4.5$ V	$I_{OL} = 32$ mA		0.35	0.5				V
		$I_{OL} = 48$ mA					0.35	0.5	
I_{OZH}	$V_{CC} = 5.5$ V,	$V_O = 2.7$ V			50			50	μA
I_{OZL}	$V_{CC} = 5.5$ V,	$V_O = 0.4$ V			–50			–50	μA
I_I	$V_{CC} = 5.5$ V,	$V_I = 7$ V			0.1			0.1	mA
I_{IH}	$V_{CC} = 5.5$ V,	$V_I = 2.7$ V			20			20	μA
I_{IL}	$V_{CC} = 5.5$ V,	$V_I = 0.4$ V			–0.5			–0.5	mA
I_O^{\S}	$V_{CC} = 5.5$ V,	$V_O = 2.25$ V	–30		–112	–30		–112	mA
I_{CC}	$V_{CC} = 5.5$ V	Outputs high		26	42		26	42	mA
		Outputs low		31	50		31	50	
		Outputs disabled		30	48		30	48	

[‡] All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

^{\S} The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

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switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX†				UNIT
			SN54AS250A		SN74AS250A		
			MIN	MAX	MIN	MAX	
t _{PLH}	Data	\overline{W}	2	9.5	2	8	ns
t _{PHL}			2	8.5	2	7	
t _{PLH}	A, B, C, D	\overline{W}	4	15.5	4	13	ns
t _{PHL}			4	12	4	10.5	
t _{PZH}	\overline{OE}	\overline{W}	2	7.5	2	7	ns
t _{PZL}			2	10	2	9	
t _{PHZ}	\overline{OE}	\overline{W}	1.5	6.5	1.5	6	ns
t _{PLZ}			2	8.5	2	6.5	

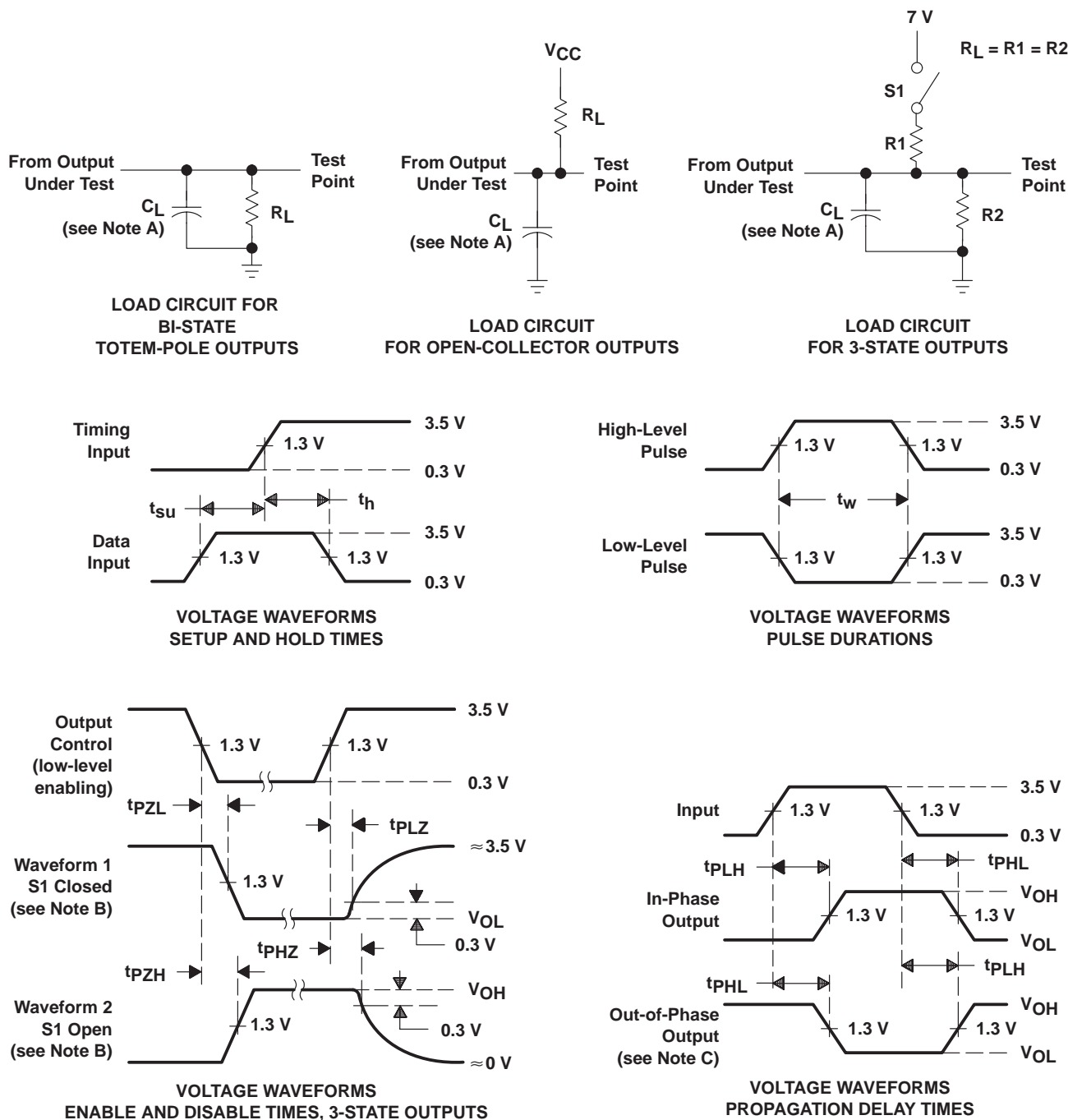
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.



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PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 D. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9056201LA	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9056201LA SNJ54AS250AJT	Samples
SN74AS250ANT	NRND	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74AS250ANT	
SN74AS250ANT3	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI	0 to 70		
SN74AS250ANTE4	NRND	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74AS250ANT	
SNJ54AS250AJT	ACTIVE	CDIP	JT	24	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9056201LA SNJ54AS250AJT	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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OTHER QUALIFIED VERSIONS OF SN54AS250A, SN74AS250A :

- Catalog: [SN74AS250A](#)
- Military: [SN54AS250A](#)

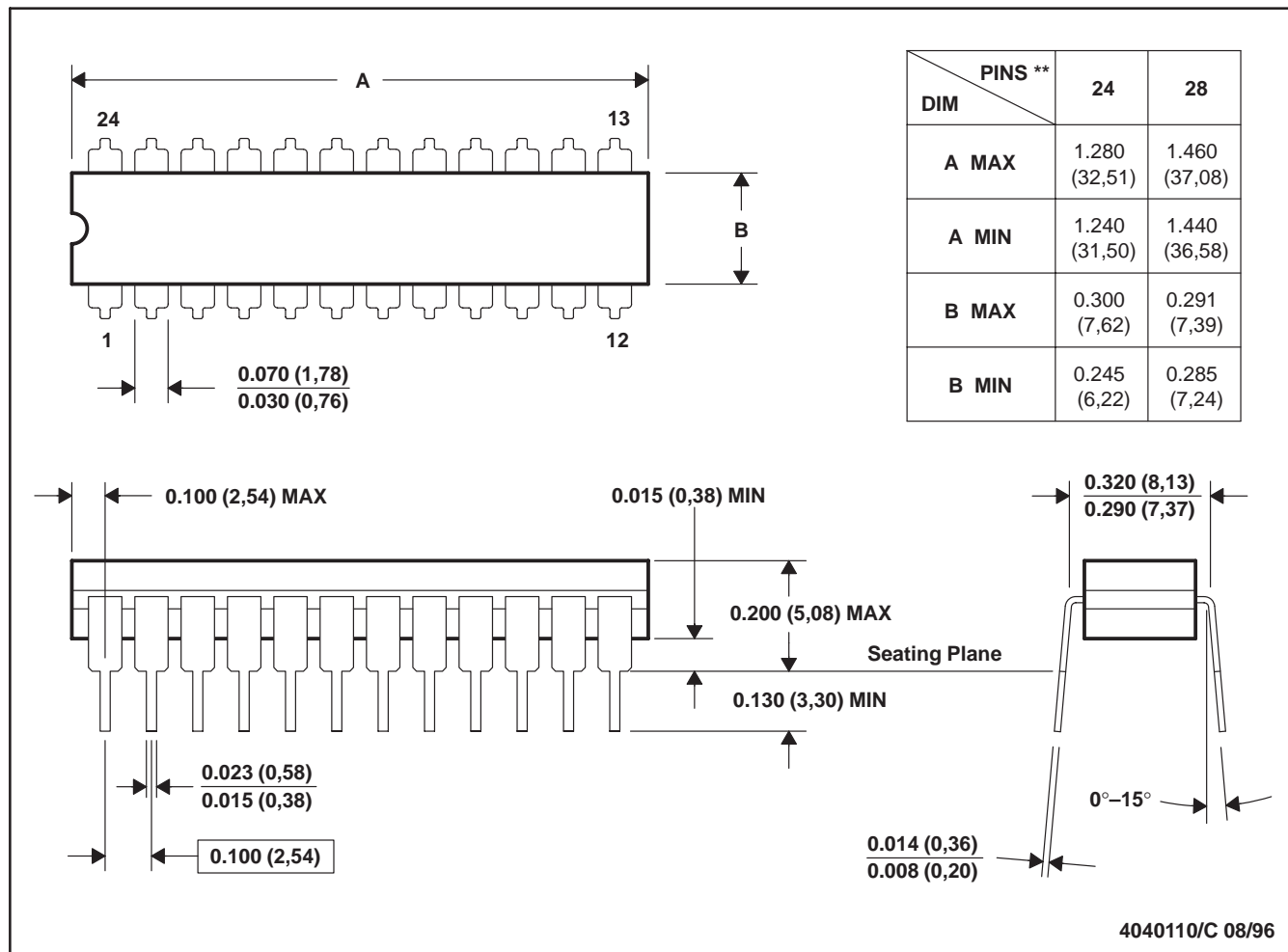
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

JT (R-GDIP-T**)

CERAMIC DUAL-IN-LINE

24 LEADS SHOWN



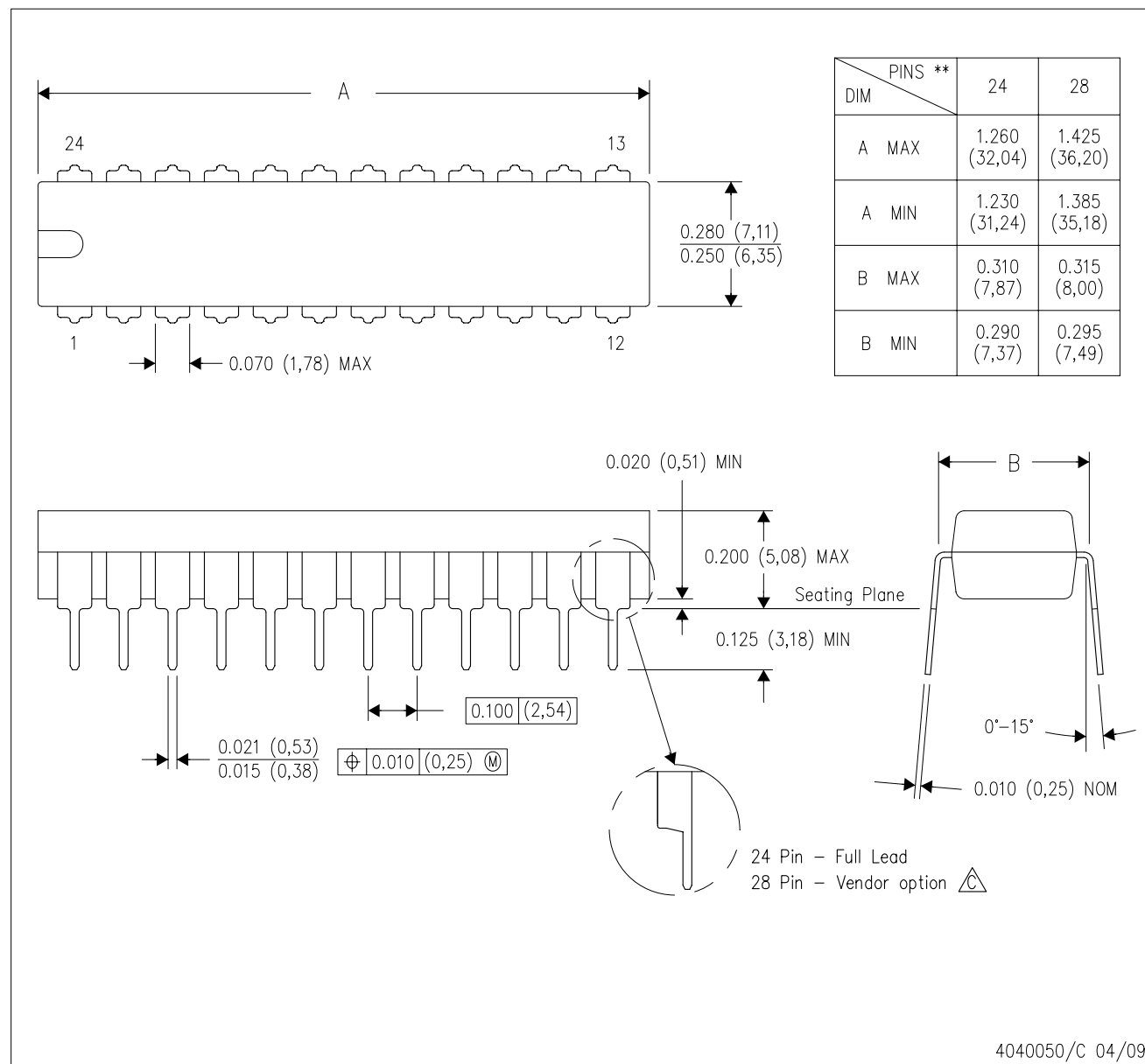
- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification.
 E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

MECHANICAL DATA

NT (R-PDIP-T**)

24 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - The 28 pin end lead shoulder width is a vendor option, either half or full width.

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