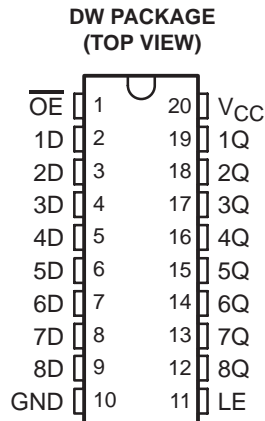


# SN74AHCT573-Q1 OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

SCLS541A – SEPTEMBER 2003 – REVISED APRIL 2008

- Qualified for Automotive Applications
- ESD Protection Exceeds 1500 V Per MIL-STD-883, Method 3015; Exceeds 150 V Using Machine Model (C = 200 pF, R = 0)
- Inputs Are TTL-Voltage Compatible
- Latch-Up Performance Exceeds 250 mA Per JESD 17



## description/ordering information

The SN74AHCT573 is an octal transparent D-type latch. When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is low, the Q outputs are latched at the logic levels of the D inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

$\overline{OE}$  does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

## ORDERING INFORMATION†

T <sub>A</sub>	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SOIC – DW	Tape and reel	SN74AHCT573QDWRQ1	AHCT573QQ1

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at <http://www.ti.com>.

‡ Package drawings, thermal data, and symbolization are available at <http://www.ti.com/packaging>.

## FUNCTION TABLE (each latch)

INPUTS			OUTPUT Q
$\overline{OE}$	LE	D	
L	H	H	H
L	H	L	L
L	L	X	Q <sub>0</sub>
H	X	X	Z



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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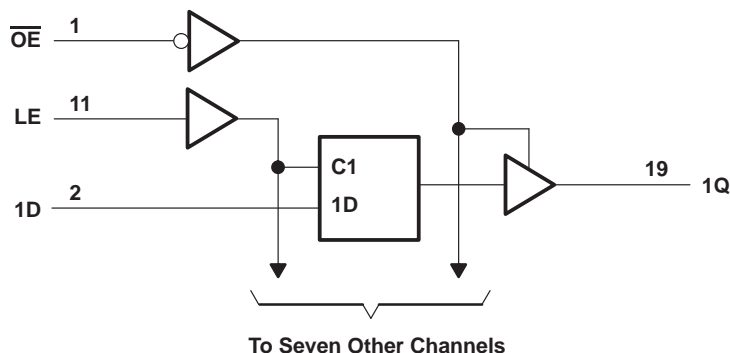
# SN74AHCT573-Q1

## OCTAL TRANSPARENT D-TYPE LATCH

### WITH 3-STATE OUTPUTS

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#### logic diagram (positive logic)



#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through $V_{CC}$ or GND	±75 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2)	58°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

#### recommended operating conditions (see Note 3)

	MIN	MAX	UNIT
$V_{CC}$ Supply voltage	4.5	5.5	V
$V_{IH}$ High-level input voltage	2		V
$V_{IL}$ Low-level input voltage		0.8	V
$V_I$ Input voltage	0	5.5	V
$V_O$ Output voltage	0	$V_{CC}$	V
$I_{OH}$ High-level output current		–8	mA
$I_{OL}$ Low-level output current		8	mA
$\Delta t/\Delta v$ Input transition rise or fall rate		20	ns/V
$T_A$ Operating free-air temperature	–40	125	°C

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V <sub>OH</sub>	I <sub>OH</sub> = -50 µA	4.5 V	4.4	4.5		4.4		V
	I <sub>OH</sub> = -8 mA		3.94			3.8		
V <sub>OL</sub>	I <sub>OL</sub> = 50 µA	4.5 V			0.1		0.1	V
	I <sub>OL</sub> = 8 mA				0.36		0.44	
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 V to 5.5 V			±0.1		±1	µA
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V			±0.25		±2.5	µA
I <sub>CC</sub>	V <sub>I</sub> = 5.5 V or GND, I <sub>O</sub> = 0	5.5 V			4		40	µA
ΔI <sub>CC</sub> <sup>†</sup>	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	5.5 V			1.35		1.5	mA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		2.5	10			pF
C <sub>o</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5 V		3				pF

<sup>†</sup> This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V<sub>CC</sub>.

**timing requirements over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

		T <sub>A</sub> = 25°C		MIN	MAX	UNIT
		MIN	MAX			
t <sub>w</sub>	Pulse duration, LE high	5		5		ns
t <sub>su</sub>	Setup time, data before LE↓	3.5		3.5		ns
t <sub>h</sub>	Hold time, data after LE↓	1.5		1.5		ns

**switching characteristics over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t <sub>PLH</sub>	D	Q	C <sub>L</sub> = 15 pF		4.2	6	1	6.5	ns
t <sub>PHL</sub>					5.1	7	1	9	
t <sub>PLH</sub>	LE	Q	C <sub>L</sub> = 15 pF		4.7	6.5	1	7.5	ns
t <sub>PHL</sub>					5.6	7.5	1	9	
t <sub>PZH</sub>	$\overline{\text{OE}}$	Q	C <sub>L</sub> = 15 pF		4.1	6.5	1	7	ns
t <sub>PZL</sub>					5.5	7.5	1	10	
t <sub>PHZ</sub>	$\overline{\text{OE}}$	Q	C <sub>L</sub> = 15 pF		5.5	8	1	11	ns
t <sub>PLZ</sub>					5.4	8	1	9.5	
t <sub>PLH</sub>	D	Q	C <sub>L</sub> = 50 pF		5.2	7	1	7.5	ns
t <sub>PHL</sub>					6.1	8	1	10	
t <sub>PLH</sub>	LE	Q	C <sub>L</sub> = 50 pF		5.7	7.5	1	8.5	ns
t <sub>PHL</sub>					6.6	8.5	1	10	
t <sub>PZH</sub>	$\overline{\text{OE}}$	Q	C <sub>L</sub> = 50 pF		5.1	7.5	1	8	ns
t <sub>PZL</sub>					6.5	8.5	1	11	
t <sub>PHZ</sub>	$\overline{\text{OE}}$	Q	C <sub>L</sub> = 50 pF		6.7	9	1	12	ns
t <sub>PLZ</sub>					6.4	9	1	10.5	
t <sub>sk(o)</sub>			C <sub>L</sub> = 50 pF			1.5			ns

# SN74AHCT573-Q1

## OCTAL TRANSPARENT D-TYPE LATCH

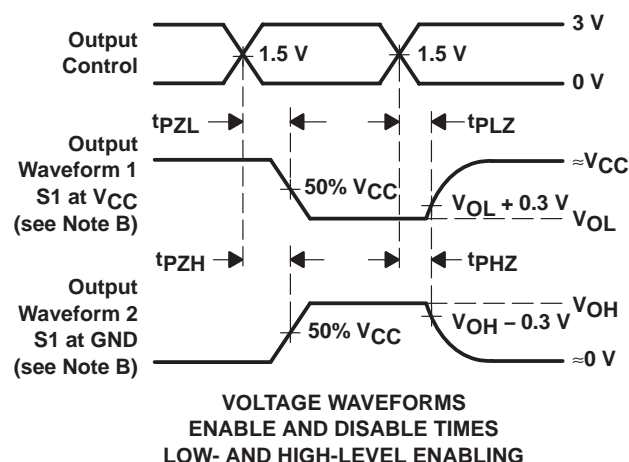
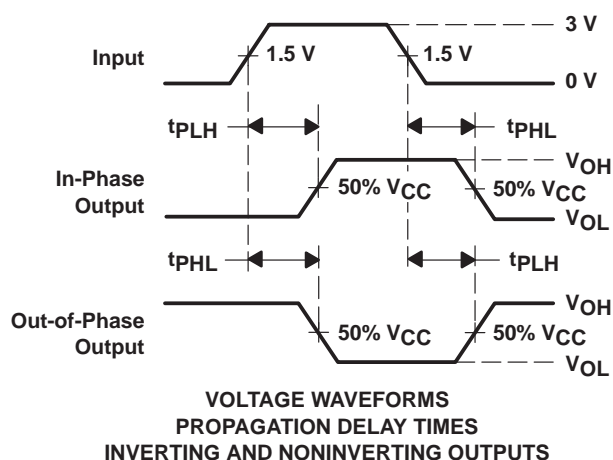
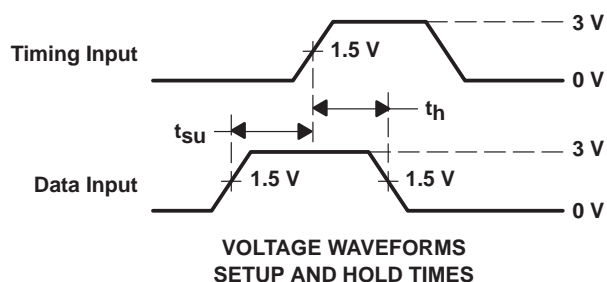
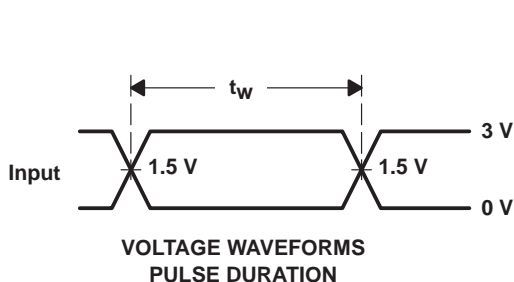
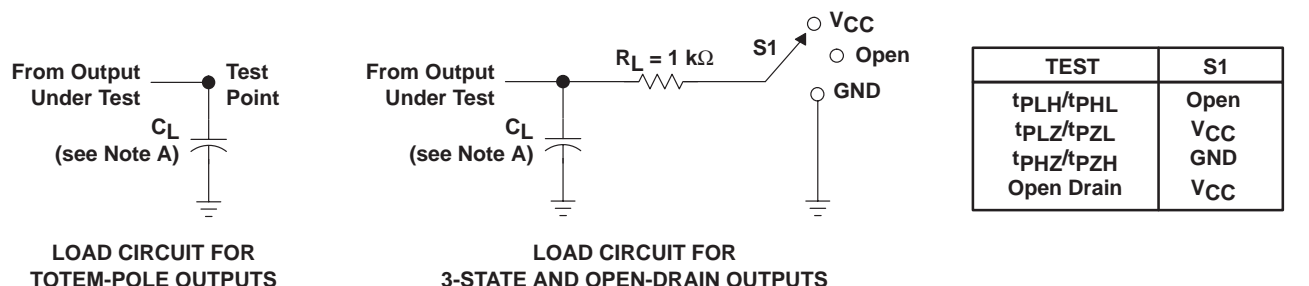
### WITH 3-STATE OUTPUTS

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operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	No load, $f = 1\text{ MHz}$	16	pF

#### PARAMETER MEASUREMENT INFORMATION



- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .
  - The outputs are measured one at a time with one input transition per measurement.
  - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AHCT573QDWRQ1	OBSOLETE	SOIC	DW	20		Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT573QQ1	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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**OTHER QUALIFIED VERSIONS OF SN74AHCT573-Q1 :**

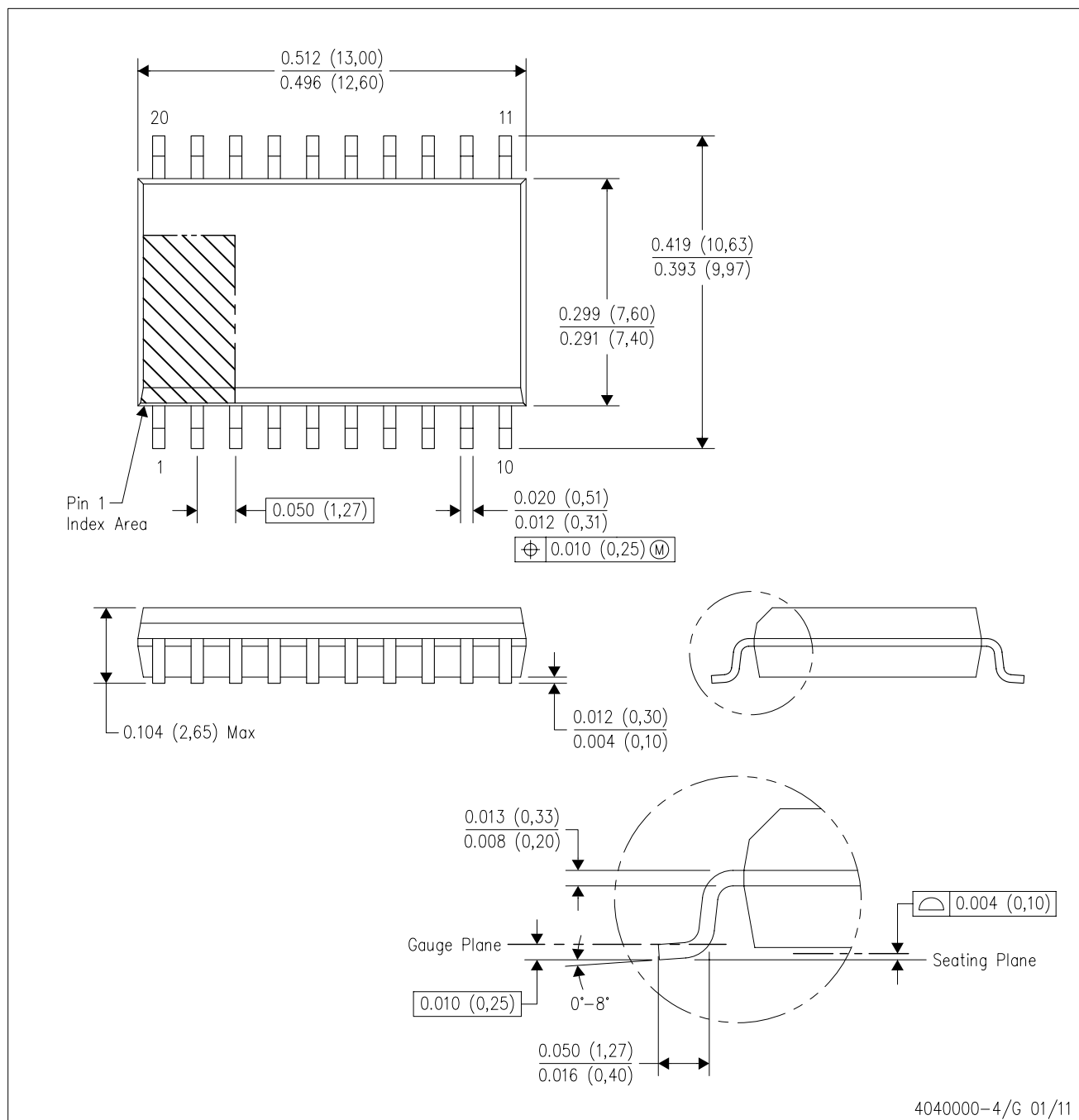
- Catalog: [SN74AHCT573](#)
- Military: [SN54AHCT573](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MS-013 variation AC.

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