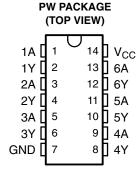
- Qualified for Automotive Applications
- 2-V to 6-V V<sub>CC</sub> Operation
- Inputs Accept Voltages to 6 V
- Max t<sub>pd</sub> of 7 ns at 5 V

## description/ordering information

The SN74AC04 device contains six independent inverters. The device performs the Boolean function  $Y = \overline{A}$ .



#### **ORDERING INFORMATION<sup>†</sup>**

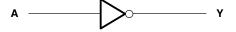
T <sub>A</sub>	PACKAGE	‡	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 125°C	TSSOP – PW	Reel of 2000	SN74AC04QPWRQ1	AC04Q
-40°C to 85°C	TSSOP – PW	Reel of 2000	SN74AC04IPWRQ1	AC04I

<sup>&</sup>lt;sup>†</sup> For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

## FUNCTION TABLE (each inverter)

INPUT A	OUTPUT Y
Н	L
L	Н

## logic diagram, each inverter (positive logic)





Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



<sup>&</sup>lt;sup>‡</sup> Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>	
Input voltage range, V <sub>I</sub> (see Note 1)	–0.5 V to V <sub>CC</sub> + 0.5 V
Output voltage range, V <sub>O</sub> (see Note 1)	–0.5 V to V <sub>CC</sub> + 0.5 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	±20 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> )	±20 mA
Continuous output current, $I_O(V_O = 0 \text{ to } V_{CC})$	±50 mA
Continuous current through V <sub>CC</sub> or GND	±200 mA
Package thermal impedance, θ <sub>JA</sub> (see Note 2)	113°C/W
Storage temperature range, T <sub>stq</sub>	65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage		2	6	V
		V <sub>CC</sub> = 3 V	2.1		
$V_{IH}$	High-level input voltage	V <sub>CC</sub> = 4.5 V	3.15		V
		V <sub>CC</sub> = 5.5 V	3.85		
		V <sub>CC</sub> = 3 V		0.9	
$V_{IL}$	Low-level input voltage	$V_{CC} = 4.5 \text{ V}$		1.35	V
		V <sub>CC</sub> = 5.5 V		1.65	
VI	Input voltage		0	$V_{CC}$	V
Vo	Output voltage		0	$V_{CC}$	V
		V <sub>CC</sub> = 3 V		-12	
l <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 4.5 V		-24	mA
		V <sub>CC</sub> = 5.5 V		-24	
		V <sub>CC</sub> = 3 V		12	
$I_{OL}$	Low-level output current	V <sub>CC</sub> = 4.5 V		24	mA
		V <sub>CC</sub> = 5.5 V		24	
Δt/Δν	Input transition rise or fall rate			8	ns/V
_	Operation for a six temperature	Q-suffix devices	-40	125	- °C
$T_A$	Operating free-air temperature	I-suffix devices	-40	85	C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

<sup>2.</sup> The package thermal impedance is calculated in accordance with JESD 51-7.

# electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	Т	<sub>A</sub> = 25°C	;	T <sub>A</sub> = -		T <sub>A</sub> = -		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
		3 V	2.9	2.99		2.9		2.9		
	I <sub>OH</sub> = -50 μA	4.5 V	4.4	4.49		4.4		4.4		
$V_{OH}$		5.5 V	5.4	5.49		5.4		5.4		.,
VOH	I <sub>OH</sub> = -12 mA	3 V	2.56			2.4		2.46		V
		4.5 V	3.86			3.7		3.76		
	I <sub>OH</sub> = -24 mA	5.5 V	4.86			4.7		4.76		
		3 V		0.002	0.1		0.1		0.1	
	I <sub>OL</sub> = 50 μA	4.5 V		0.001	0.1		0.1		0.1	
,,		5.5 V		0.001	0.1		0.1		0.1	.,
V <sub>OL</sub>	I <sub>OL</sub> = 12 mA	3 V			0.36		0.5		0.44	V
		4.5 V			0.36		0.5		0.44	
	I <sub>OL</sub> = 24 mA	5.5 V			0.36		0.5		0.44	
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V			±0.1		±1		±1	μΑ
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			2		40		20	μΑ
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND			2.8						pF

# switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V $\pm$ 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	TO (OUTPUT)	T,	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C TO 125°C		T <sub>A</sub> = -40°C TO 85°C	
	(INPUT)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	Λ.	V	1.5	4.5	9	1	11	1	10	no
t <sub>PHL</sub>	Α	Ť	1.5	4.5	8.5	1	10	1	9.5	ns

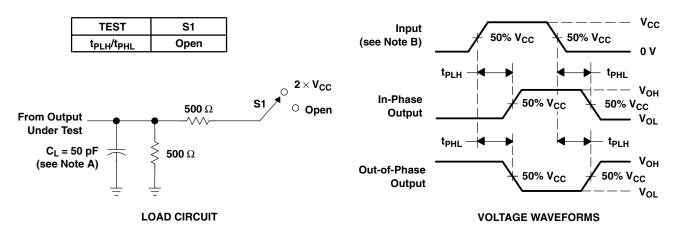
# switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T,	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C TO 125°C		T <sub>A</sub> = -40°C TO 85°C	
	(INPOT)	(001701)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	Δ.	V	1.5	4	7	1	8.5	1	7.5	no
t <sub>PHL</sub>	А	Ť	1.5	3.5	6.5	1	7.5	1	7	ns

## operating characteristics, $V_{CC} = 5 \text{ V}$ , $T_A = 25^{\circ}\text{C}$

PARAMETER	TEST CO	TYP	UNIT		
C <sub>pd</sub> Power dissipation capacitance		$C_L = 50 \text{ pF},$	f = 1 MHz	45	pF

## PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_0 = 50 \ \Omega$ ,  $t_r \leq 2.5 \ ns$ ,  $t_f \leq 2.5 \ ns$ .
- C. The outputs are measured one at a time, with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms







11-Apr-2013

#### PACKAGING INFORMATION

	Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Top-Side Markings	Samples
-	SN74AC04QPWRG4Q1	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC04Q	Samples
	SN74AC04QPWRQ1	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AC04Q	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

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#### OTHER QUALIFIED VERSIONS OF SN74AC04-Q1:

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.



## **PACKAGE OPTION ADDENDUM**

11-Apr-2013

• Catalog: SN74AC04

● Enhanced Product: SN74AC04-EP

• Military: SN54AC04

#### NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Enhanced Product Supports Defense, Aerospace and Medical Applications
- Military QML certified for Military and Defense Applications

## PACKAGE MATERIALS INFORMATION

www.ti.com 14-Mar-2013

## TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

## QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AC04QPWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AC04QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

## **PACKAGE MATERIALS INFORMATION**

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#### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AC04QPWRG4Q1	TSSOP	PW	14	2000	367.0	367.0	35.0
SN74AC04QPWRQ1	TSSOP	PW	14	2000	367.0	367.0	35.0

PW (R-PDSO-G14)

## PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
  - Sody length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153



## PW (R-PDSO-G14)

## PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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