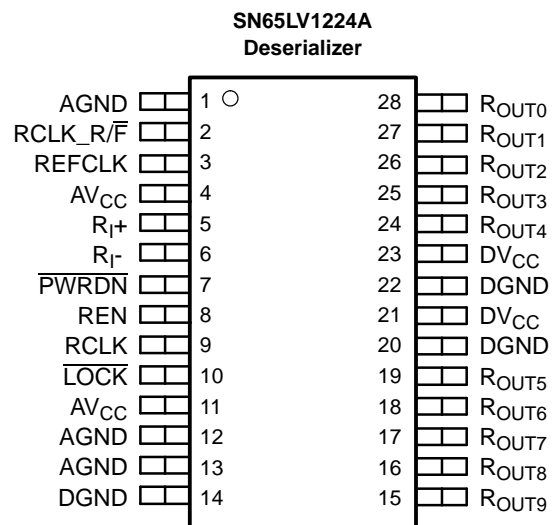
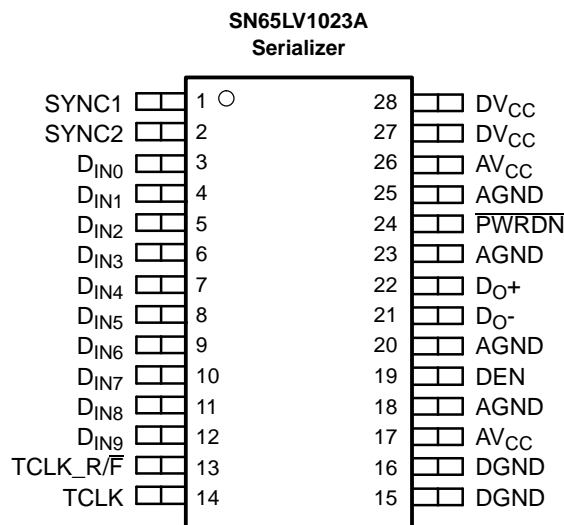


10-MHz TO 66-MHz, 10:1 LVDS SERIALIZER/DESERIALIZER

FEATURES

- 100-Mbps to 660-Mbps Serial LVDS Data Payload Bandwidth at 10-MHz to 66-MHz System Clock
- Pin-Compatible Superset of NSM DS92LV1023/DS92LV1224
- Chipset (Serializer/Deserializer) Power Consumption <450 mW (Typ) at 66 MHz
- Synchronization Mode for Faster Lock
- Lock Indicator
- No External Components Required for PLL
- Low-Cost 28-Pin SSOP Package
- Industrial Temperature Qualified, $T_A = -40^{\circ}\text{C}$ to 85°C
- Programmable Edge Trigger on Clock
- Flow-Through Pinout for Easy PCB Layout



DESCRIPTION

The SN65LV1023A serializer and SN65LV1224A deserializer comprise a 10-bit serdes chipset designed to transmit and receive serial data over LVDS differential backplanes at equivalent parallel word rates from 10 MHz to 66 MHz. Including overhead, this translates into a serial data rate between 120-Mbps and 792-Mbps payload encoded throughput.

Upon power up, the chipset link can be initialized via a synchronization mode with internally generated SYNC patterns, or the deserializer can be allowed to synchronize to random data. By using the synchronization mode, the deserializer establishes lock within specified, shorter time parameters.

The device can be entered into a power-down state when no data transfer is required. Alternatively, a mode is available to place the output pins in the high-impedance state without losing PLL lock.

The SN65LV1023A and SN65LV1224A are characterized for operation over ambient air temperature of -40°C to 85°C .

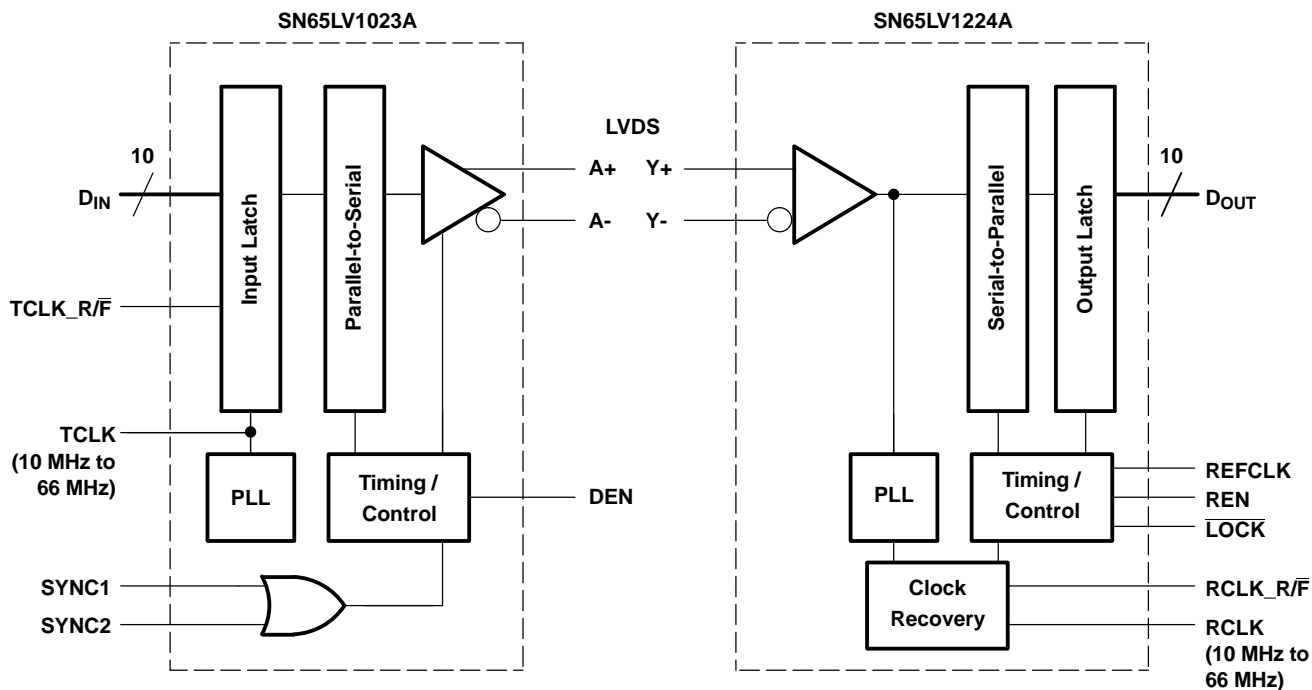
ORDERING INFORMATION

| DEVICE | PART NUMBER |
|--------------|---------------|
| Serializer | SN65LV1023ADB |
| Deserializer | SN65LV1224ADB |



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

BLOCK DIAGRAMS



FUNCTIONAL DESCRIPTION

The SN65LV1023A and SN65LV1224A are a 10-bit serializer/deserializer chipset designed to transmit data over differential backplanes or unshielded twisted pair (UTP) at clock speeds from 10 MHz to 66 MHz. The chipset has five states of operation: initialization mode, synchronization mode, data transmission mode, power-down mode, and high-impedance mode. The following sections describe each state of operation.

Initialization Mode

Initialization of both devices must occur before data transmission can commence. Initialization refers to synchronization of the serializer and deserializer PLLs to local clocks.

When V_{CC} is applied to the serializer and/or deserializer, the respective outputs enter the high-impedance state, while on-chip power-on circuitry disables internal circuitry. When V_{CC} reaches 2.45 V, the PLL in each device begins locking to a local clock. For the serializer, the local clock is the transmit clock (TCLK) provided by an external source. For the deserializer, a local clock must be applied to the REFCLK pin. The serializer outputs remain in the high-impedance state, while the PLL locks to the TCLK.

FUNCTIONAL DESCRIPTION (continued)

Synchronization Mode

The deserializer PLL must synchronize to the serializer in order to receive valid data. Synchronization can be accomplished in one of two ways:

- Rapid Synchronization:** The serializer has the capability to send specific SYNC patterns consisting of six ones and six zeros switching at the input clock rate. The transmission of SYNC patterns enables the deserializer to lock to the serializer signal within a deterministic time frame. This transmission of SYNC patterns is selected via the SYNC1 and SYNC2 inputs on the serializer. Upon receiving valid SYNC1 or SYNC2 pulse (wider than 6 clock cycles), 1026 cycles of SYNC pattern are sent.

When the deserializer detects edge transitions at the LVDS input, it attempts to lock to the embedded clock information. The deserializer $\overline{\text{LOCK}}$ output remains high while its PLL locks to the incoming data or SYNC patterns present on the serial input. When the deserializer locks to the LVDS data, the $\overline{\text{LOCK}}$ output goes low. When $\overline{\text{LOCK}}$ is low, the deserializer outputs represent incoming LVDS data. One approach is to tie the deserializer $\overline{\text{LOCK}}$ output directly to SYNC1 or SYNC2.

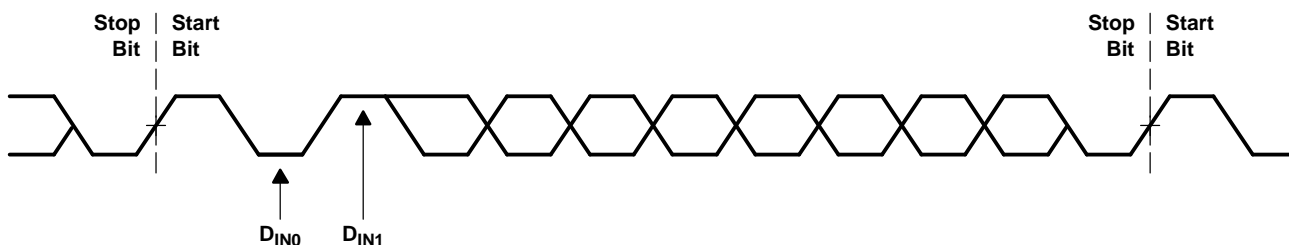
- Random-Lock Synchronization:** The deserializer can attain lock to a data stream without requiring the serializer to send special SYNC patterns. This allows the SN65LV1224A to operate in open-loop applications. Equally important is the deserializer's ability to support hot insertion into a running backplane. In the open-loop or hot-insertion case, it is assumed the data stream is essentially random. Therefore, because lock time varies due to data stream characteristics, the exact lock time cannot be predicted. The primary constraint on the random lock time is the initial phase relation between the incoming data and the REFCLK when the deserializer powers up.

The data contained in the data stream can also affect lock time. If a specific pattern is repetitive, the deserializer could enter false lock – falsely recognizing the data pattern as the start/stop bits. This is referred to as repetitive multitransition (RMT); see [Figure 1](#) for RMT examples. This occurs when more than one low-high transition takes place per clock cycle over multiple cycles. In the worst case, the deserializer could become locked to the data pattern rather than the clock. Circuitry within the deserializer can detect that the possibility of false lock exists. Upon detection, the circuitry prevents the $\overline{\text{LOCK}}$ output from becoming active until the potential false lock pattern changes. Notice that the RMT pattern only affects the deserializer lock time, and once the deserializer is in lock, the RMT pattern does not affect the deserializer state as long as the same data boundary happens each cycle. The deserializer does not go into lock until it finds a unique four consecutive cycles of data boundary (stop/start bits) at the same position.

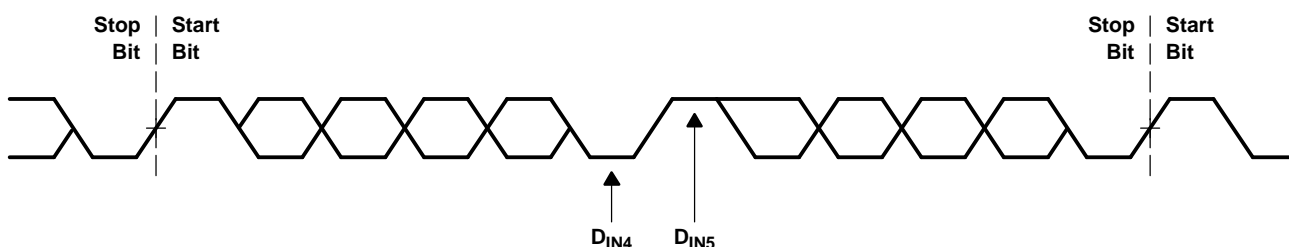
The deserializer stays in lock until it cannot detect the same data boundary (stop/start bits) for four consecutive cycles. Then the deserializer goes out of lock and hunts for the new data boundary (stop/start bits). In the event of loss of synchronization, the $\overline{\text{LOCK}}$ pin output goes high and the outputs (including RCLK) enter a high-impedance state. The user's system should monitor the $\overline{\text{LOCK}}$ pin in order to detect a loss of synchronization. Upon detection of loss of lock, sending sync patterns for resynchronization is desirable if reestablishing lock within a specific time is critical. However, the deserializer can lock to random data as previously noted.

FUNCTIONAL DESCRIPTION (continued)

D_{IN0} Held Low and D_{IN1} Held High



D_{IN4} Held Low and D_{IN5} Held High



D_{IN8} Held Low and D_{IN9} Held High

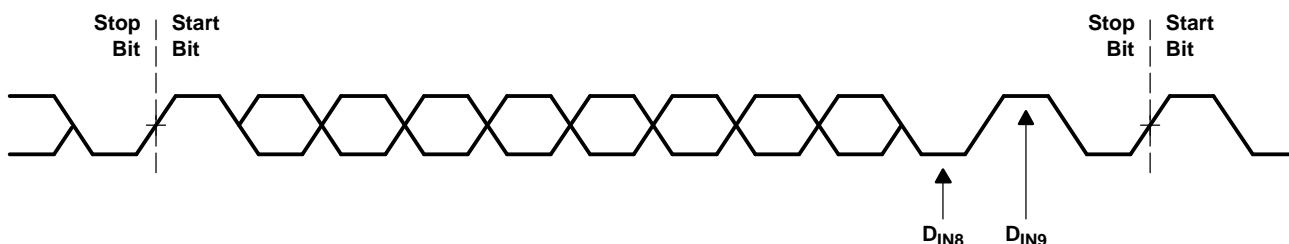


Figure 1. RMT Pattern Examples

Data Transmission Mode

After initialization and synchronization, the serializer accepts parallel data from inputs D_{IN0} – D_{IN9} . The serializer uses the TCLK input to latch the incoming data. The TCLK_R/ \bar{F} pin selects which edge the serializer uses to strobe incoming data. If either of the SYNC inputs is high for six TCLK cycles, the data at D_{IN0} – D_{IN9} is ignored regardless of the clock edge selected and 1026 cycles of SYNC pattern are sent.

After determining which clock edge to use, a start and stop bit, appended internally, frames the data bits in the register. The start bit is always high and the stop bit is always low. The start and stop bits function as the embedded clock bits in the serial stream.

The serializer transmits serialized data and appended clock bits (10+2 bits) from the serial data output (DO_{\pm}) at 12 times the TCLK frequency. For example, if TCLK is 66 MHz, the serial rate is $66 \times 12 = 792$ Mbps. Because only 10 bits are input data, the useful data rate is 10 times the TCLK frequency. For instance, if TCLK = 66 MHz, the useful data rate is $66 \times 10 = 660$ Mbps. The data source, which provides TCLK, must be in the range of 10 MHz to 66 MHz.

The serializer outputs (DO_{\pm}) can drive point-to-point connections or limited multipoint or multidrop backplanes. The outputs transmit data when the enable pin (DEN) is high, PWRDN = high, and SYNC1 and SYNC2 are low. When DEN is driven low, the serializer output pins enter the high-impedance state.

FUNCTIONAL DESCRIPTION (continued)

Once the deserializer has synchronized to the serializer, the $\overline{\text{LOCK}}$ pin transitions low. The deserializer locks to the embedded clock and uses it to recover the serialized data. R_{OUT} data is valid when $\overline{\text{LOCK}}$ is low, otherwise $\text{R}_{\text{OUT}0}\text{--}\text{R}_{\text{OUT}9}$ is invalid. The $\text{R}_{\text{OUT}0}\text{--}\text{R}_{\text{OUT}9}$ data is strobed out by RCLK. The specific RCLK edge polarity to be used is selected by the RCLK_R/F input. The $\text{R}_{\text{OUT}0}\text{--}\text{R}_{\text{OUT}9}$, $\overline{\text{LOCK}}$ and RCLK outputs can drive a maximum of three CMOS input gates (15-pF load, total for all three) with a 66-MHz clock.

Power Down

When no data transfer is required, the power-down mode can be used. The serializer and deserializer use the power-down state, a low-power sleep mode, to reduce power consumption. The deserializer enters power down when you drive $\overline{\text{PWRDN}}$ and REN low. The serializer enters power down when you drive $\overline{\text{PWRDN}}$ low. In power down, the PLL stops and the outputs enter a high-impedance state, which disables load current and reduces supply current to the milliampere range. To exit power down, you must drive the $\overline{\text{PWRDN}}$ pin high.

Before valid data exchanges between the serializer and deserializer can resume, you must reinitialize and resynchronize the devices to each other. Initialization of the serializer takes 1026 TCLK cycles. The deserializer initialize and drives $\overline{\text{LOCK}}$ high until lock to the LVDS clock occurs.

High-Impedance Mode

The serializer enters the high-impedance mode when the DEN pin is driven low. This puts both driver output pins (DO+ and DO–) into a high-impedance state. When you drive DEN high, the serializer returns to the previous state, as long as all other control pins remain static ($\overline{\text{SYNC1}}$, $\overline{\text{SYNC2}}$, $\overline{\text{PWRDN}}$, TCLK_R/F). When the REN pin is driven low, the deserializer enters high-impedance mode. Consequently, the receiver output pins ($\text{R}_{\text{OUT}0}\text{--}\text{R}_{\text{OUT}9}$) and RCLK are placed into the high-impedance state. The $\overline{\text{LOCK}}$ output remains active, reflecting the state of the PLL.

Deserializer Truth Table

| INPUTS | | OUTPUTS | | |
|---------------------------|-----|--------------------------|--------------------------------|---------------------|
| $\overline{\text{PWRDN}}$ | REN | $\text{ROUT}[0:9]^{(1)}$ | $\overline{\text{LOCK}}^{(2)}$ | RCLK ⁽³⁾ |
| H | H | Z | H | Z |
| H | H | Active | L | Active |
| L | X | Z | Z | Z |
| H | L | Z | Active | Z |

(1) ROUT and RCLK are 3-stated when $\overline{\text{LOCK}}$ is asserted high.

(2) $\overline{\text{LOCK}}$ output reflects the state of the deserializer with regard to the selected data stream.

(3) RCLK active indicates the RCLK is running if the deserializer is locked. The timing of RCLK with respect to ROUT is determined by RCLK_R/F.

Failsafe Biasing for the SN65LV1224A

The SN65LV1224A has an input threshold sensitivity of ± 50 mV. This allows for greater differential noise margin in the SN65LV1224A. However, in cases where the receiver input is not being actively driven, the increased sensitivity of the SN65LV1224A can pickup noise as a signal and cause unintentional locking. This may occur when the input cable is disconnected. SN65LV1224A has an on-chip fail-safe circuit that drives the serial input and $\overline{\text{LOCK}}$ Signal high. The response time of the fail-safe circuit depends on interconnect characteristics.

Terminal Functions

| SERIALIZER | | |
|----------------|--------------------------------------|---|
| PIN | NAME | DESCRIPTION |
| 18, 20, 23, 25 | AGND | Analog circuit ground (PLL and analog circuits) |
| 17, 26 | AV _{CC} | Analog circuit power supply (PLL and analog circuits) |
| 19 | DEN | LVTTL logic input. Low puts the LVDS serial output into the high-impedance state. High enables serial data output. |
| 15, 16 | DGND | Digital circuit ground |
| 3-12 | D _{IN0} –D _{IN9} | Parallel LVTTL data inputs |
| 21 | D _{O–} | Inverting LVDS differential output |
| 22 | D _{O+} | Noninverting LVDS differential output |
| 27, 28 | DV _{CC} | Digital circuit power supply |
| 24 | PWRDN | LVTTL logic input. Asserting this pin low turns off the PLL and places the outputs into the high-impedance state, putting the device into a low-power mode. |
| 1, 2 | SYNC1, SYNC2 | LVTTL logic inputs SYNC1 and SYNC2 are ORed together. When at least one of the two pins is asserted high for 6 cycles of TCLK, the serializer initiates transmission of a minimum 1026 SYNC patterns. If after completion of the transmission of 1026 patterns SYNC continues to be asserted, then the transmission continues until SYNC is driven low and if the time SYNC holds > 6 cycles, another 1026 SYNC pattern transmission initiates. |
| 13 | TCLK_R/ \overline{F} | LVTTL logic input. Low selects a TCLK falling-edge data strobe; high selects a TCLK rising-edge data strobe. |
| 14 | TCLK | LVTTL-level reference clock input. The SN65LV1023A accepts a 10-MHz to 66-MHz clock. TCLK strobes parallel data into the input latch and provides a reference frequency to the PLL. |
| DESERIALIZER | | |
| 1, 12, 13 | AGND | Analog circuit ground (PLL and analog circuits) |
| 4, 11 | AV _{CC} | Analog circuit power supply (PLL and analog circuits) |
| 14, 20, 22 | DGND | Digital circuit ground |
| 21, 23 | DV _{CC} | Digital circuit power supply |
| 10 | LOCK | LVTTL level output. LOCK goes low when the deserializer PLL locks onto the embedded clock edge. |
| 7 | PWRDN | LVTTL logic input. Asserting this pin low turns off the PLL and places outputs into a high-impedance state, putting the device into a low-power mode. To initiate power down, this pin is held low for a minimum of 16 ns. As long as PWRDN is held low, the device is in the power down state. |
| 2 | RCLK_R/ \overline{F} | LVTTL logic input. Low selects an RCLK falling-edge data strobe; high selects an RCLK rising-edge data strobe. |
| 9 | RCLK | LVTTL level output recovered clock. Use RCLK to strobe R _{OUTx} . |
| 3 | REFCLK | LVTTL logic input. Use this pin to supply a REFCLK signal for the internal PLL frequency. |
| 8 | REN | LVTTL logic input. Low places R _{OUT0} –R _{OUT9} and RCLK in the high-impedance state. |
| 5 | R _{I+} | Serial data input. Noninverting LVDS differential input |
| 6 | R _{I–} | Serial data input. Inverting LVDS differential input |
| 15-19, 24–28 | R _{OUT0} –R _{OUT9} | Parallel LVTTL data outputs |

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | UNIT |
|---|-----|-------------------------------|
| V_{CC} to GND | | –0.3 V to 4 V |
| LVTTL input voltage | | –0.3 V to ($V_{CC} + 0.3$ V) |
| LVTTL output voltage | | –0.3 V to ($V_{CC} + 0.3$ V) |
| LVDS receiver input voltage | | –0.3 V to 3.9 V |
| LVDS driver output voltage | | –0.3 V to 3.9 V |
| LVDS output short circuit duration | | 10 ms |
| Electrostatic discharge | HBM | Up to 6 kV |
| | MM | Up to 200 V |
| Junction temperature | | 150°C |
| Storage temperature | | –65°C to 150°C |
| Lead temperature (soldering, 4 seconds) | | 260°C |
| Maximum package power dissipation, $T_A = 25^\circ\text{C}$ | | 1.27 W |
| Package derating | | 10.3 mW/°C above 25°C |

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

| | | MIN | NOM | MAX | UNIT |
|----------|----------------------------------|--------------------|---------------------------------------|-----|-------------------|
| V_{CC} | Supply voltage ⁽¹⁾ | 3 | 3.3 | 3.6 | V |
| | Receiver input voltage range | 0 | | 2.4 | V |
| V_{CM} | Receiver input common mode range | $\frac{V_{ID}}{2}$ | $2.4 - \left(\frac{V_{ID}}{2}\right)$ | | V |
| | Supply noise voltage | | | 100 | mV _{P-P} |
| T_A | Operating free-air temperature | –40 | 25 | 85 | °C |

- (1) By design, DVCC and AVCC are separated internally and does not matter what the difference is for |DVCC–AVCC|, as long as both are within 3 V to 3.6 V.

ELECTRICAL CHARACTERISTICS

over recommended operating supply and temperature ranges (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|---|---|------------|-------|-----------------|------|
| SERIALIZER LVCMOS/LVTTL DC SPECIFICATIONS ⁽¹⁾ | | | | | | |
| V _{IH} | High-level input voltage | | 2 | | V _{CC} | V |
| V _{IL} | Low-level input voltage | | GND | | 0.8 | V |
| V _{CL} | Input clamp voltage | I _{CL} = –18 mA | | –0.86 | –1.5 | V |
| I _{IN} | Input current ⁽²⁾ | V _{IN} = 0 V or 3.6 V | –200 | ±100 | 200 | μA |
| DESERIALIZER LVCMOS/LVTTL DC SPECIFICATIONS ⁽³⁾ | | | | | | |
| V _{IH} | High-level input voltage | | 2 | | V _{CC} | V |
| V _{IL} | Low-level input voltage | | GND | | 0.8 | V |
| V _{CL} | Input clamp voltage | I _{CL} = –18 mA | | –0.62 | –1.5 | V |
| I _{IN} | Input current (pull-up and pull-down resistors on inputs) | V _{IN} = 0 V or 3.6 V | –200 | | 200 | μA |
| V _{OH} | High-level output voltage | I _{OH} = –5 mA | 2.2 | 3 | V _{CC} | V |
| V _{OL} | Low-level output voltage | I _{OL} = 5 mA | GND | 0.25 | 0.5 | V |
| I _{OS} | Output short-circuit current | V _{OUT} = 0 V | –15 | –47 | –85 | mA |
| I _{OZ} | High-impedance output current | $\overline{\text{PWRDN}}$ or REN = 0.8 V, V _{OUT} = 0 V or V _{CC} | –10 | ±1 | 10 | μA |
| SERIALIZER LVDS DC SPECIFICATIONS (APPLY TO PINS DO+ AND DO–) | | | | | | |
| V _{OD} | Output differential voltage (DO+)–(DO–) | R _L = 27 Ω, See Figure 19 | 350 | 450 | | mV |
| ΔV _{OD} | Output differential voltage unbalance | | | | 35 | mV |
| V _{OS} | Offset voltage | | 1.1 | 1.2 | 1.3 | V |
| ΔV _{OS} | Offset voltage unbalance | | | 4.8 | 35 | mV |
| I _{OS} | Output short circuit current | D0 = 0 V, D _{INx} = high, $\overline{\text{PWRDN}}$ and DEN = 2.4 V | | –10 | –90 | mA |
| I _{OZ} | High-impedance output current | $\overline{\text{PWRDN}}$ or DEN = 0.8 V, DO = 0 V or V _{CC} | –10 | ±1 | 10 | μA |
| I _{OX} | Power-off output current | V _{CC} = 0 V, DO = 0 V or 3.6 V | –20 | ±1 | 25 | μA |
| C _O | Output single-ended capacitance | | | | 1±20% | pF |
| DESERIALIZER LVDS DC SPECIFICATIONS (APPLY TO PINS RI+ AND RI–) | | | | | | |
| V _{TH} | Differential threshold high voltage | V _{CM} = 1.1 V | | | 50 | mV |
| V _{TL} | Differential threshold low voltage | | –50 | | | mV |
| I _{IN} | Input current | V _{IN} = 2.4 V, V _{CC} = 3.6 V or 0 V | –10 | ±1 | 15 | μA |
| | | V _{IN} = 0 V, V _{CC} = 3.6 V or 0 V | –10 | ±0.05 | 10 | |
| C _I | Input single-ended capacitance | | | | 0.5±20% | pF |
| SERIALIZER SUPPLY CURRENT (APPLIES TO PINS DVCC AND AVCC) | | | | | | |
| I _{CCD} | Serializer supply current worst case | R _L = 27 Ω, See Figure 4 | f = 10 MHz | 20 | 25 | mA |
| | | | f = 66 MHz | 55 | 70 | |
| I _{CCXD} | Serializer supply current | $\overline{\text{PWRDN}}$ = 0.8 V | | 200 | 500 | μA |
| DESERIALIZER SUPPLY CURRENT (APPLIES TO PINS DVCC AND AVCC) | | | | | | |
| I _{CCR} | Deserializer supply current, worst case | C _L = 15 pF, See Figure 4 | f = 10 MHz | 15 | 35 | mA |
| | | | f = 66 MHz | 80 | 95 | |
| I _{CCXR} | Deserializer supply current, power down | $\overline{\text{PWRDN}}$ = 0.8 V, REN = 0.8 V | | 0.36 | 1 | mA |

(1) Apply to D_{IN0}–D_{IN9}, TCLK, $\overline{\text{PWRDN}}$, TCLK_R/F, SYNC1, SYNC2, DEN

(2) High I_{IN} values are due to pullup and pulldown resistors on the inputs.

(3) Apply to pins $\overline{\text{PWRDN}}$, RCLK_R/F, REN, REFCLK = inputs; apply to pins R_{OUTx}, RCLK, $\overline{\text{LOCK}}$ = outputs

SERIALIZER TIMING REQUIREMENTS FOR TCLK

over recommended operating supply and temperature ranges (unless otherwise specified)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------|----------------------------|-----------------|-------|------|------|----------|
| t_{TCP} | Transmit clock period | | 15.15 | T | 100 | ns |
| t_{TCIH} | Transmit clock high time | | 0.4T | 0.5T | 0.6T | ns |
| t_{TCIL} | Transmit clock low time | | 0.4T | 0.5T | 0.6T | ns |
| $t_{i(CLK)}$ | TCLK input transition time | | | 3 | 6 | ns |
| t_{JIT} | TCLK input jitter | See Figure 18 | | | 150 | ps (RMS) |
| | Frequency Tolerance | | –100 | | 100 | ppm |

SERIALIZER SWITCHING CHARACTERISTICS

over recommended operating supply and temperature ranges (unless otherwise specified)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------|--|---|-----------------------|-------------|-------------|----------|
| $t_{TLH(L)}$ | LVDS low-to-high transition time | $R_L = 27\ \Omega$, $C_L = 10\ \text{pF}$ to GND, See Figure 5 | | 0.2 | 0.4 | ns |
| $t_{LTH(L)}$ | LVDS high-to-low transition time | | | 0.25 | 0.4 | ns |
| $t_{su(DI)}$ | D_{IN0} – D_{IN9} setup to TCLK | $R_L = 27\ \Omega$, $C_L = 10\ \text{pF}$ to GND, See Figure 8 | 0.5 | | | ns |
| $t_{su(DI)}$ | D_{IN0} – D_{IN9} hold from TCLK | | 4 | | | ns |
| $t_{d(HZ)}$ | DO± high-to-high-impedance-state delay | $R_L = 27\ \Omega$, $C_L = 10\ \text{pF}$ to GND, See Figure 9 | | 2.5 | 5 | ns |
| $t_{d(LZ)}$ | DO± low-to-high-impedance-state delay | | | 2.5 | 5 | |
| $t_{d(ZH)}$ | DO± high-to-high-impedance-state-to-high delay | | | 5 | 10 | |
| $t_{d(ZL)}$ | DO± high-to-high-impedance-state-to-low delay | | | 6.5 | 10 | |
| $t_{w(SPW)}$ | SYNC pulse duration | $R_L = 27\ \Omega$, See Figure 11 | $6 \times t_{TCP}$ | | | ns |
| t_{PLD} | Serializer PLL lock time | | $1026 \times t_{TCP}$ | | | ns |
| $t_{d(S)}$ | Serializer delay | $R_L = 27\ \Omega$, See Figure 12 | $t_{TCP}+1$ | $t_{TCP}+2$ | $t_{TCP}+3$ | ns |
| t_{DJIT} | Deterministic jitter | $R_L = 27\ \Omega$, $C_L = 10\ \text{pF}$ to GND | | | 230 | ps |
| | | | | | 150 | |
| t_{RJIT} | Random jitter | $R_L = 2.7\ \Omega$, $C_L = 10\ \text{pF}$ to GND | | 10 | 19 | ps (RMS) |

DESERIALIZER TIMING REQUIREMENTS FOR REFCLK

over recommended operating supply and temperature ranges (unless otherwise specified)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------|------------------------|-----------------|-----------|-----|------|------|
| t_{RFCP} | REFCLK period | | 15.1 5 | T | 100 | ns |
| t_{RFDC} | REFCLK duty cycle | | 30% | 50% | 70% | |
| $t_{i(RF)}$ | REFCLK transition time | | | 3 | 6 | ns |
| | Frequency tolerance | | 100 | | +100 | ppm |

DESERIALIZER SWITCHING CHARACTERISTICS

over recommended operating supply and temperature ranges (unless otherwise specified)

| PARAMETER | | TEST CONDITIONS | PIN/FREQ | MIN | TYP | MAX | UNIT | |
|----------------------------------|--|---|--|----------------------------|-----------------------|-----------------------------|------|--|
| t _(RCP) | Receiver out clockperiod | t _(RCP) = t _(TCP) , See Figure 12 | RCLK | 15.15 | | 100 | ns | |
| t _{TLH(C)} | CMOS/TTL low-to-high transition time | C _L = 15 pF, See Figure 6 | R _{OUT0} –R _{OUT9} , LOCK, RCLK | 1.2 | | 2.5 | ns | |
| t _{THL(C)} | CMOS/TTL high-to-low transition time | | | 1.1 | | 2.5 | | |
| t _{d(D)} ⁽¹⁾ | Deserializer delay, See Figure 13 | Room temperature, 3.3 V | 10 MHz | 1.75×t _{RCP} +4.2 | | 1.75×t _{RCP} +12.6 | ns | |
| | | | 66 MHz | 1.75×t _{RCP} +7.4 | | 1.75×t _{RCP} +9.7 | | |
| t _(ROS) | R _{OUTx} data valid before RCLK | See Figure 14 | RCLK 10 MHz | 0.4×t _{RCP} | 0.5×t _{RCP} | ns | | |
| | RCLK 66 MHz | | 0.4×t _{RCP} | 0.5×t _{RCP} | | | | |
| t _(ROH) | R _{OUTx} data valid after RCLK | | 10 MHz | –0.4×t _{RCP} | –0.5×t _{RCP} | | | |
| | | | 66 MHz | –0.4×t _{RCP} | –0.5×t _{RCP} | | | |
| t _(RDC) | RCLK duty cycle | | | 40% | 50% | 60% | | |
| t _{d(HZ)} | High-to-high-impedance state delay | See Figure 15 | R _{OUT0} –R _{OUT9} | 6.5 | | 8 | ns | |
| t _{d(LZ)} | Low-to-high-impedance state delay | | | 4.7 | | 8 | ns | |
| t _{d(HR)} | High-impedance state-to-high delay | | | 5.3 | | 8 | ns | |
| t _{d(ZL)} | High-impedance-state-to-low delay | | | 4.7 | | 8 | ns | |
| t _(DSR1) | Deserializer PLL lock time from PWRDN(with SYNCPAT) | See Figure 16 , Figure 17 , and ⁽²⁾ | 10 MHz | 815 x t _{RFCP} | | μs | | |
| | | | 66 MHz | 815 x t _{RFCP} | | | | |
| t _(DSR2) | Deserializer PLL lock time from SYNCPAT | | 10 MHz | 0.7 | | | | |
| | | | 66 MHz | 0.2 | | | | |
| t _{d(ZHLK)} | High-impedance-state to-high delay(power up) | | LOCK | 3 | | ns | | |
| t _{RNM} | Deserializer noise margin | | See Figure 18 and ⁽³⁾ | 10 MHz | 3680 | | ps | |
| | | | | 66 MHz | 540 | | | |

(1) The deserializer delay time for all frequencies does not exceed 2 serial bit times.

(2) $t_{(DSR1)}$ represents the time required for the deserializer to register that a lock has occurred upon powerup or when leaving the powerdown mode. $t_{(DSR2)}$ represents the time required to register that a lock has occurred for the powered up and enabled deserializer when the input (RI±) conditions change from not receiving data to receiving synchronization patterns (SYNCPATs). In order to specify deserializer PLL performance $t_{(DSR1)}$ and $t_{(DSR2)}$ are specified with REFCLK active and stable and specific conditions of SYNCPATs.

(3) t_{RNM} represents the phase noise or jitter that the deserializer can withstand in the incoming data stream before bit errors occur.

TIMING DIAGRAMS AND TEST CIRCUITS

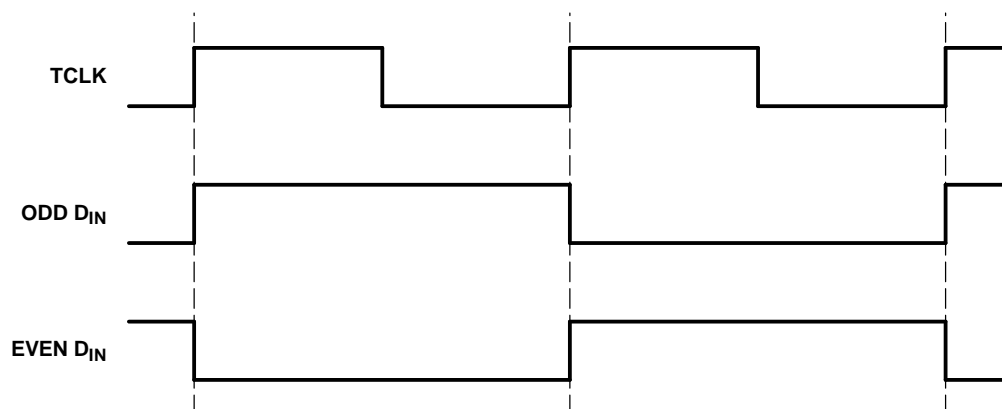


Figure 2. Worst-Case Serializer I_{CC} Test Pattern

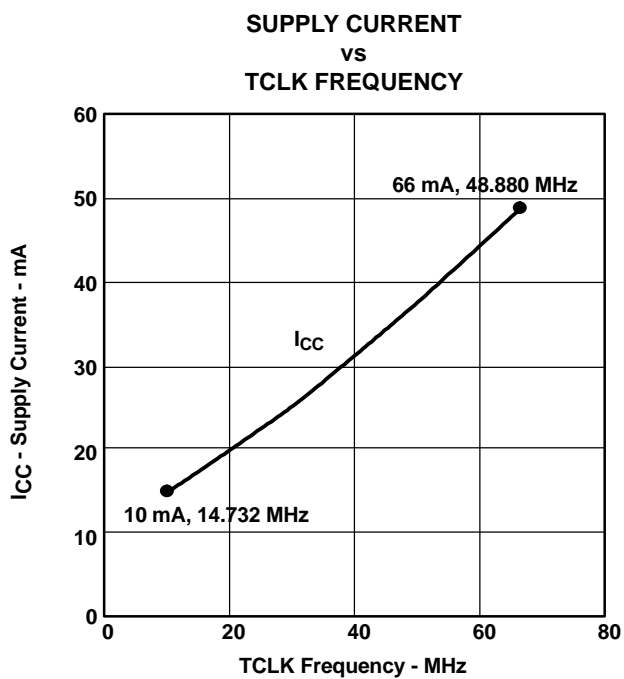


Figure 3.

TIMING DIAGRAMS AND TEST CIRCUITS (continued)

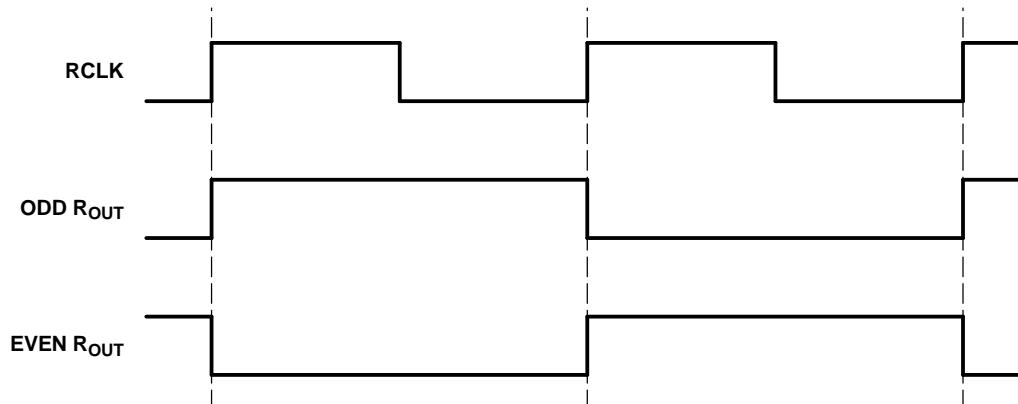


Figure 4. Worst-Case Deserializer I_{CC} Test Pattern

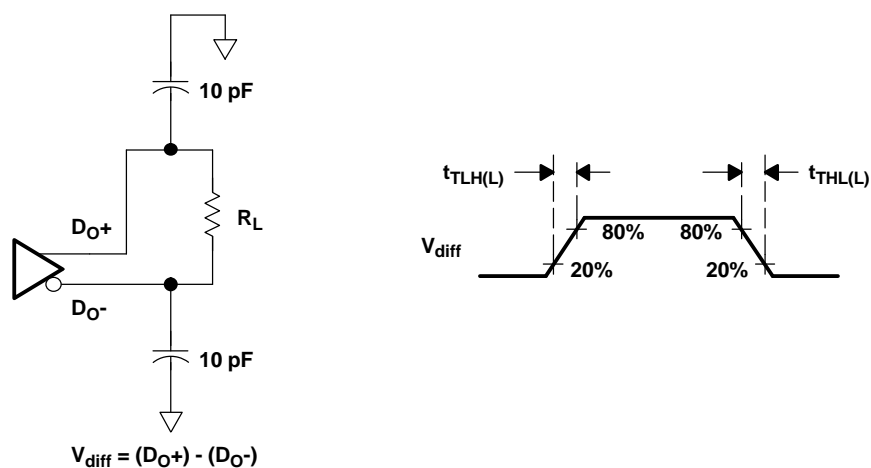


Figure 5. Serializer LVDS Output Load and Transition Times

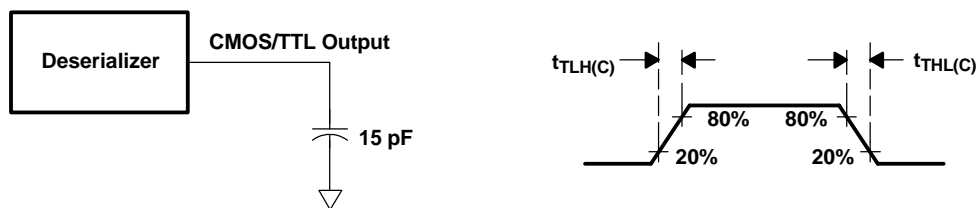


Figure 6. Deserializer CMOS/TTL Output Load and Transition Times

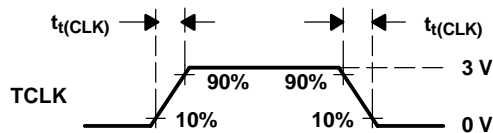


Figure 7. Serializer Input Clock Transition Time

TIMING DIAGRAMS AND TEST CIRCUITS (continued)

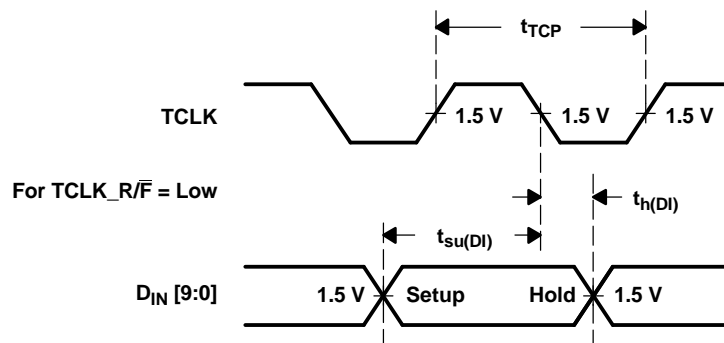


Figure 8. Serializer Setup/Hold Times

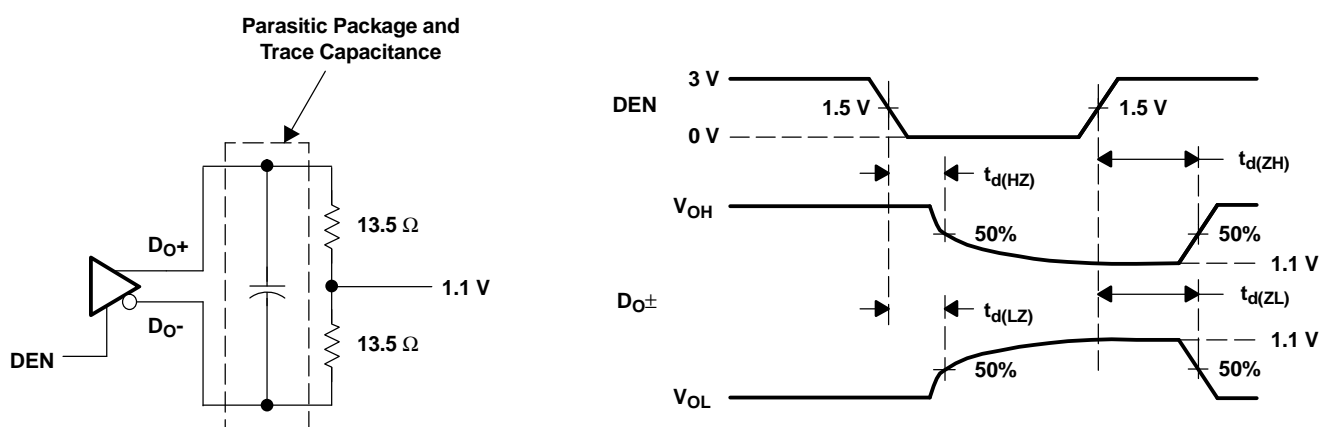


Figure 9. Serializer High-Impedance-State Test Circuit and Timing

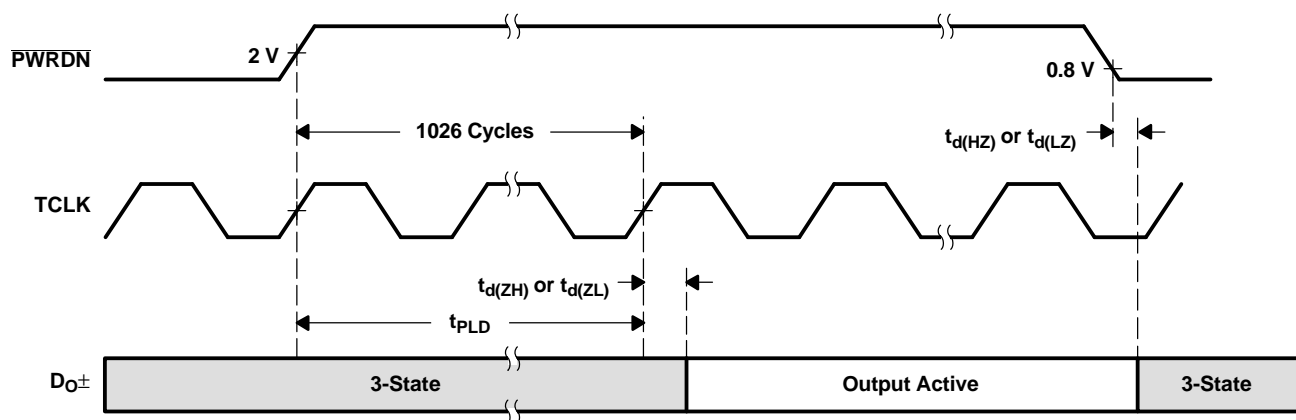


Figure 10. Serializer PLL Lock Time and $\overline{\text{PWRDN}}$ High-Impedance-State Delays

TIMING DIAGRAMS AND TEST CIRCUITS (continued)

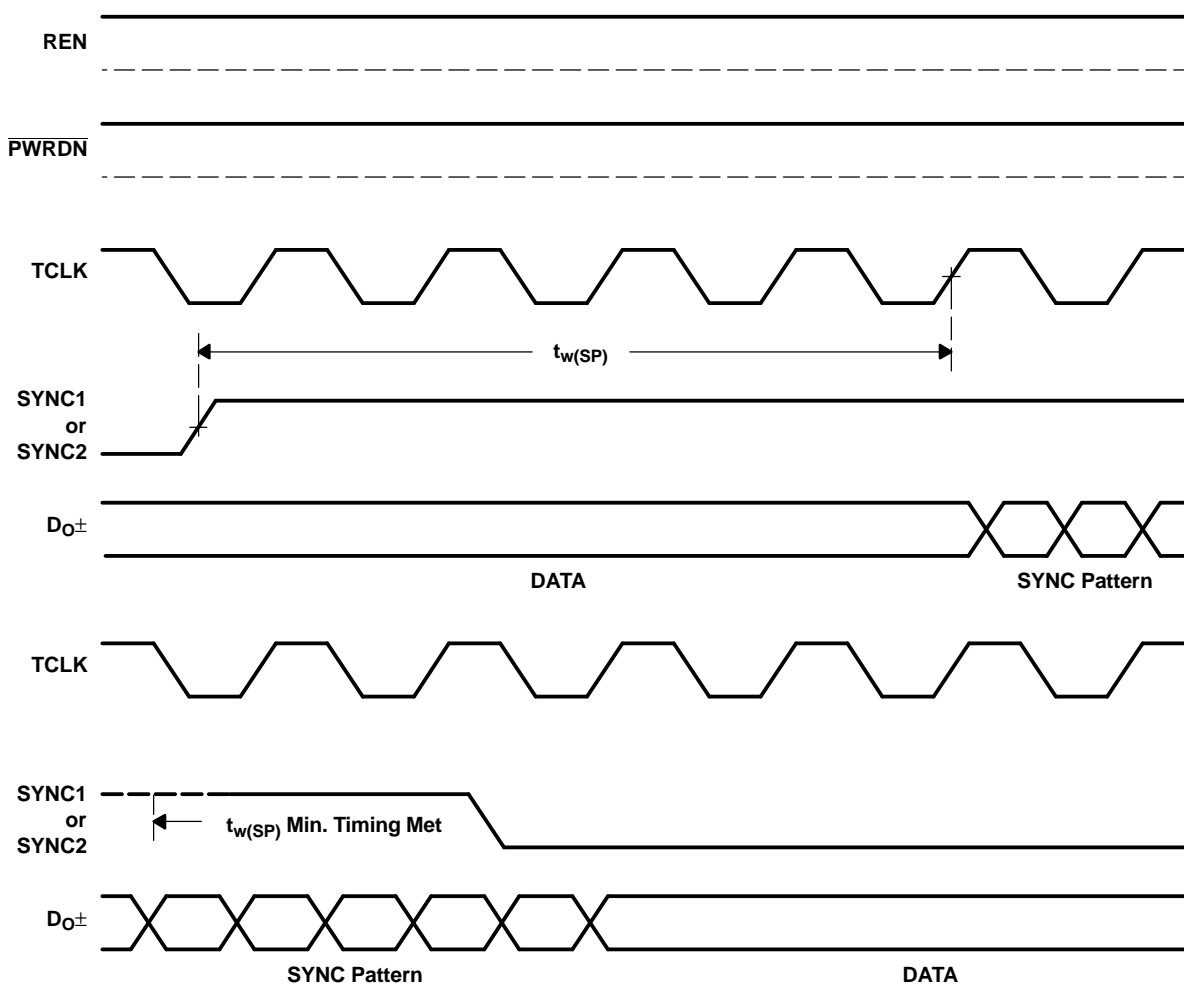


Figure 11. SYNC Timing Delays

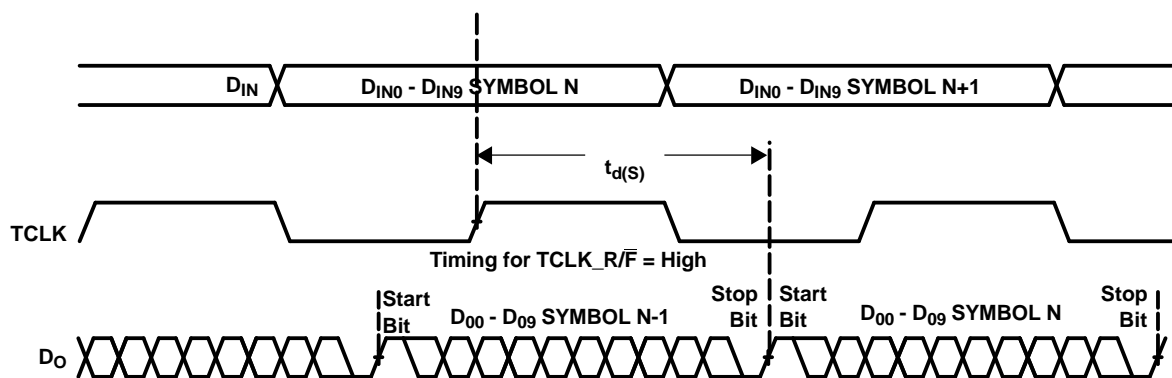


Figure 12. Serializer Delay

TIMING DIAGRAMS AND TEST CIRCUITS (continued)

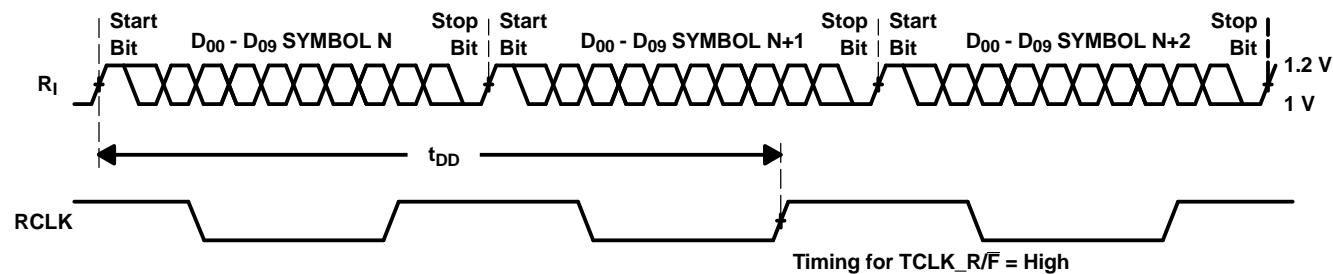


Figure 13. Deserializer Delay

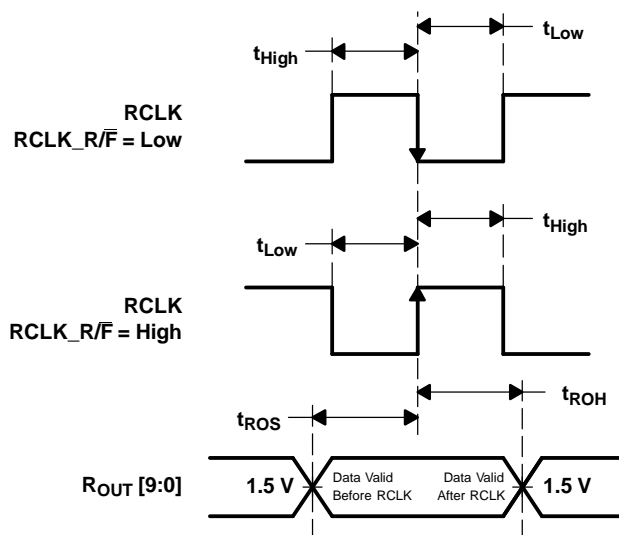


Figure 14. Deserializer Data Valid Out Times

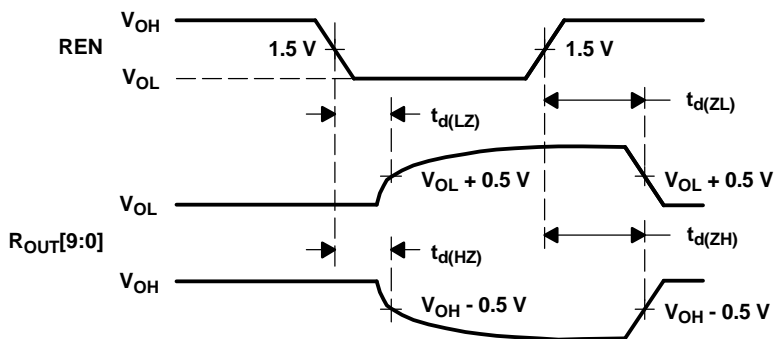
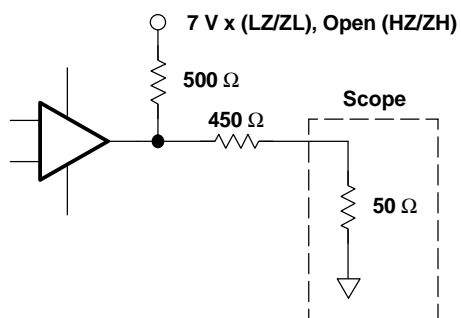


Figure 15. Deserializer High-Impedance-State Test Circuit and Timing

TIMING DIAGRAMS AND TEST CIRCUITS (continued)

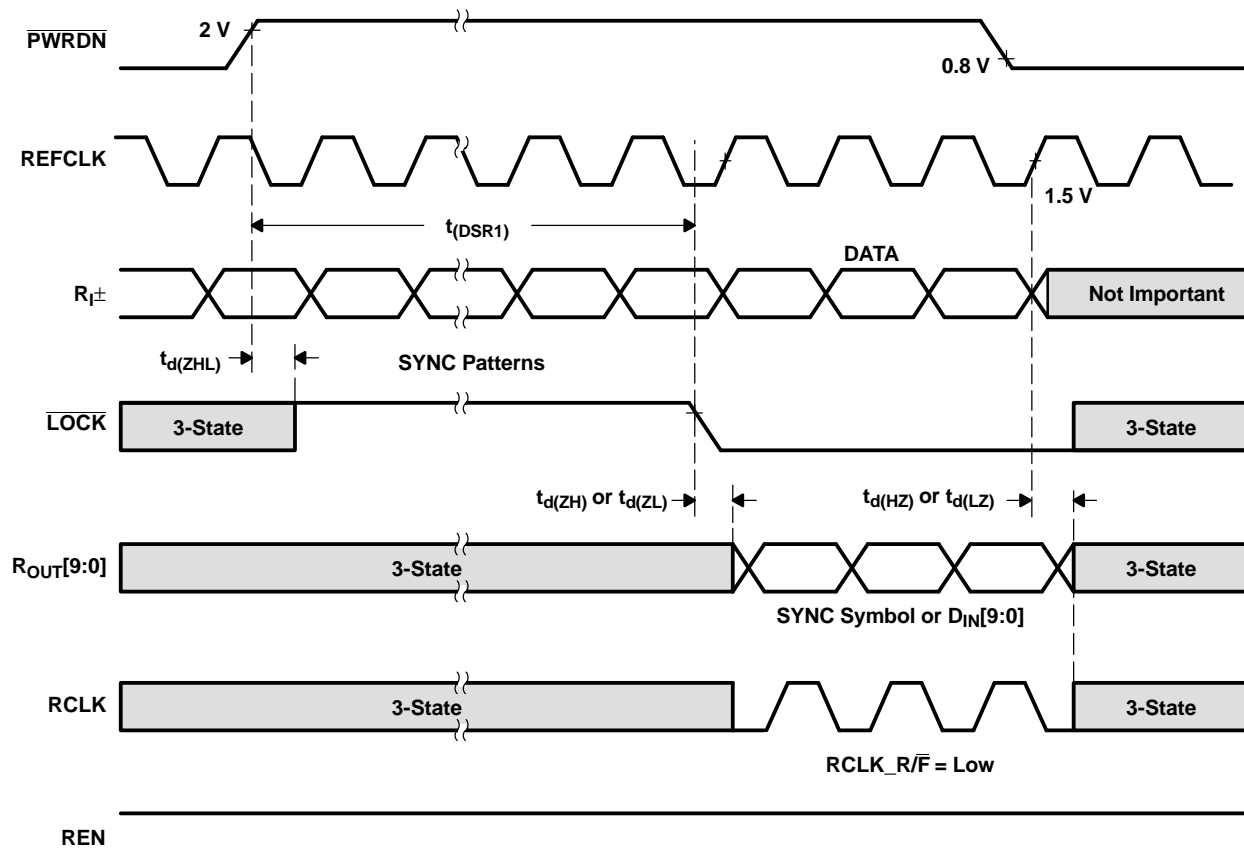


Figure 16. Deserializer PLL Lock Times and $\overline{\text{PWRDN}}$ 3-State Delays

TIMING DIAGRAMS AND TEST CIRCUITS (continued)

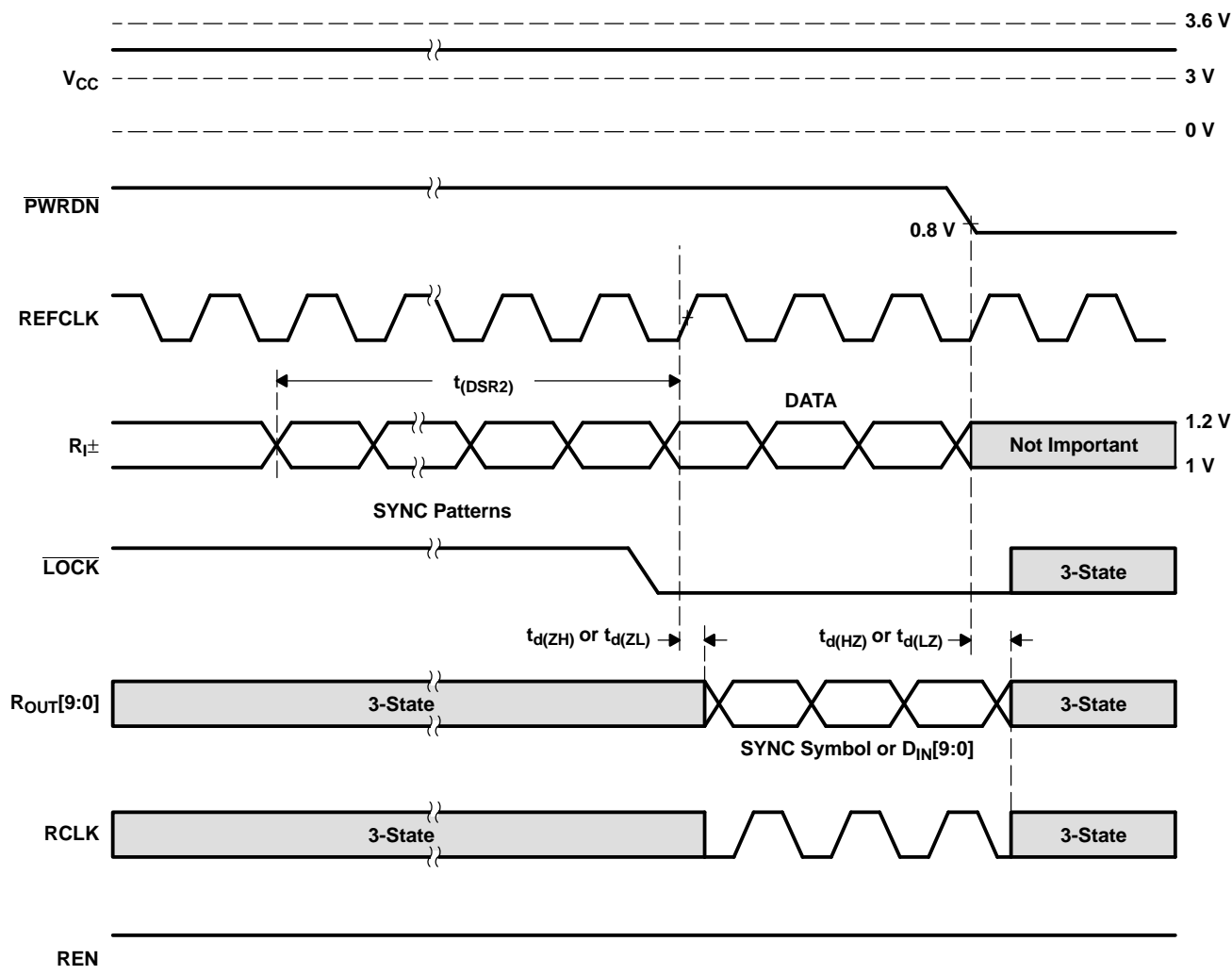
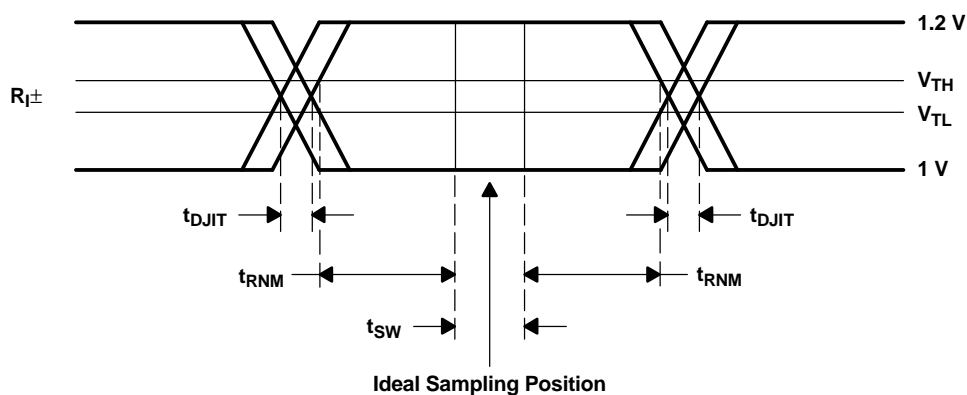


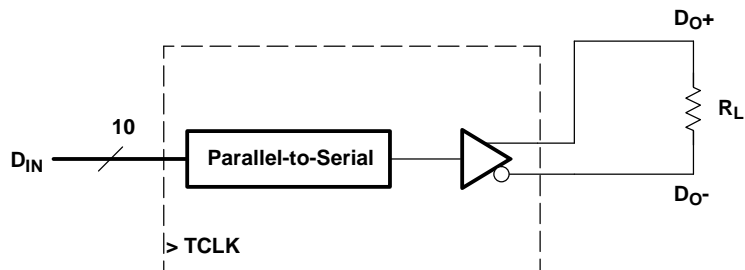
Figure 17. Deserializer PLL Lock Time From SyncPAT



t_{SW} : Setup and Hold Time (Internal Data Sampling Window)
 t_{DJIT} : Serializer Output Bit Position Jitter That Results From Jitter on TCLK
 t_{RNM} : Receiver Noise Margin Time

Figure 18. Receiver LVDS Input Skew Margin

TIMING DIAGRAMS AND TEST CIRCUITS (continued)



$V_{OD} = (D_{O+}) - (D_{O-})$
Differential Output Signal Is Shown as $(D_{O+}) - (D_{O-})$

Figure 19. V_{OD} Diagram

APPLICATION INFORMATION

DIFFERENTIAL TRACES AND TERMINATION

The performance of the SN65LV1023A/SN65LV1224A is affected by the characteristics of the transmission medium. Use controlled-impedance media and termination at the receiving end of the transmission line with the media's characteristics impedance.

Use balanced cables such as twisted pair or differential traces that are ran close together. A balanced cable picks up noise together and appears to the receiver as common mode. Differential receivers reject common-mode noise. Keep cables or traces matched in length to help reduce skew.

Running the differential traces close together helps cancel the external magnetic field, as well as maintain a constant impedance. Avoiding sharp turns and reducing the number of vias also helps.

TOPOLOGIES

There are several topologies that the serializers can operate. Three common examples are shown below.

Figure 20 shows an example of a single-terminated point-to-point connection. Here a single termination resistor is located at the deserializer end. The resistor value should match that of the characteristic impedance of the cable or PC board traces. The total load seen by the serializer is $100\ \Omega$. Double termination can be used and typically reduces reflections compared with single termination. However, it also reduces the differential output voltage swing.

AC-coupling is only recommended if the parallel TX data stream is encoded to achieve a dc-balanced data stream. Otherwise the AC-caps can induce common mode voltage drift due to the dc-unbalanced data stream.

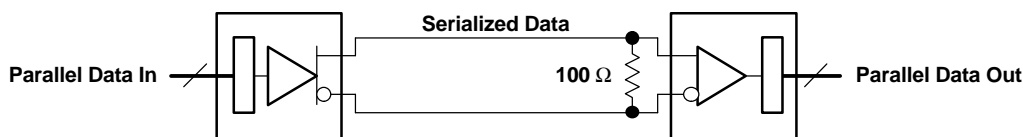


Figure 20. Single-Terminated Point-to-Point Connection

Figure 21 shows an example of a multidrop configuration. Here there is one transmitter broadcasting data to multiple receivers. A $50\text{-k}\Omega$ resistor at the far end terminates the bus.

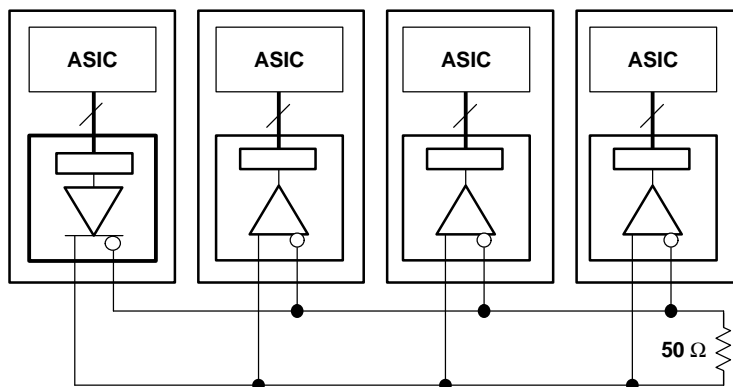


Figure 21. Multidrop Configuration

Figure 22 shows an example of multiple serializers and deserializers on the same differential bus, such as in a backplane. This is a multipoint configuration. In this situation, the characteristic impedance of the bus can be significantly less due to loading. Termination resistors that match the loaded characteristic impedance are required at each end of the bus. The total load seen by the serializer in this example is $27\ \Omega$.

TOPOLOGIES (continued)

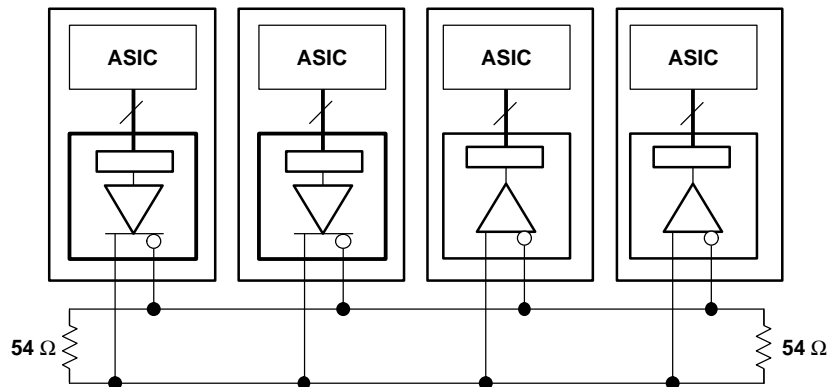


Figure 22. Multiple Serializers and Deserializers on the Same Differential Bus

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|-------------------|---------------|--------------|--------------------|------|----------------|----------------------------|------------------|----------------------|--------------|-------------------------|-------------------------|
| SN65LV1023ADB | ACTIVE | SSOP | DB | 28 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV1023A | Samples |
| SN65LV1023ADBG4 | ACTIVE | SSOP | DB | 28 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV1023A | Samples |
| SN65LV1023ADBR | ACTIVE | SSOP | DB | 28 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV1023A | Samples |
| SN65LV1023ADBRG4 | ACTIVE | SSOP | DB | 28 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV1023A | Samples |
| SN65LV1023ARHBR | ACTIVE | VQFN | RHB | 32 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | SN65LV 1023A | Samples |
| SN65LV1023ARHBRG4 | ACTIVE | VQFN | RHB | 32 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | SN65LV 1023A | Samples |
| SN65LV1023ARHBT | ACTIVE | VQFN | RHB | 32 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | SN65LV 1023A | Samples |
| SN65LV1224ADB | NRND | SSOP | DB | 28 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV1224A | |
| SN65LV1224ADBG4 | NRND | SSOP | DB | 28 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV1224A | |
| SNLV1023ARHBTG4 | ACTIVE | VQFN | RHB | 32 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | SN65LV 1023A | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN65LV1023A :

- Enhanced Product: [SN65LV1023A-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN65LV1023ADBR | SSOP | DB | 28 | 2000 | 330.0 | 16.4 | 8.1 | 10.4 | 2.5 | 12.0 | 16.0 | Q1 |
| SN65LV1023ARHBR | VQFN | RHB | 32 | 3000 | 330.0 | 12.4 | 5.3 | 5.3 | 1.5 | 8.0 | 12.0 | Q2 |
| SN65LV1023ARHBT | VQFN | RHB | 32 | 250 | 180.0 | 12.4 | 5.3 | 5.3 | 1.5 | 8.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN65LV1023ADBR | SSOP | DB | 28 | 2000 | 367.0 | 367.0 | 38.0 |
| SN65LV1023ARHBR | VQFN | RHB | 32 | 3000 | 338.1 | 338.1 | 20.6 |
| SN65LV1023ARHBT | VQFN | RHB | 32 | 250 | 210.0 | 185.0 | 35.0 |

RHB (S-PVQFN-N32)

PLASTIC QUAD FLATPACK NO-LEAD



4204326/D 06/11

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) Package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Falls within JEDEC MO-220.

RHB (S-PVQFN-N32)

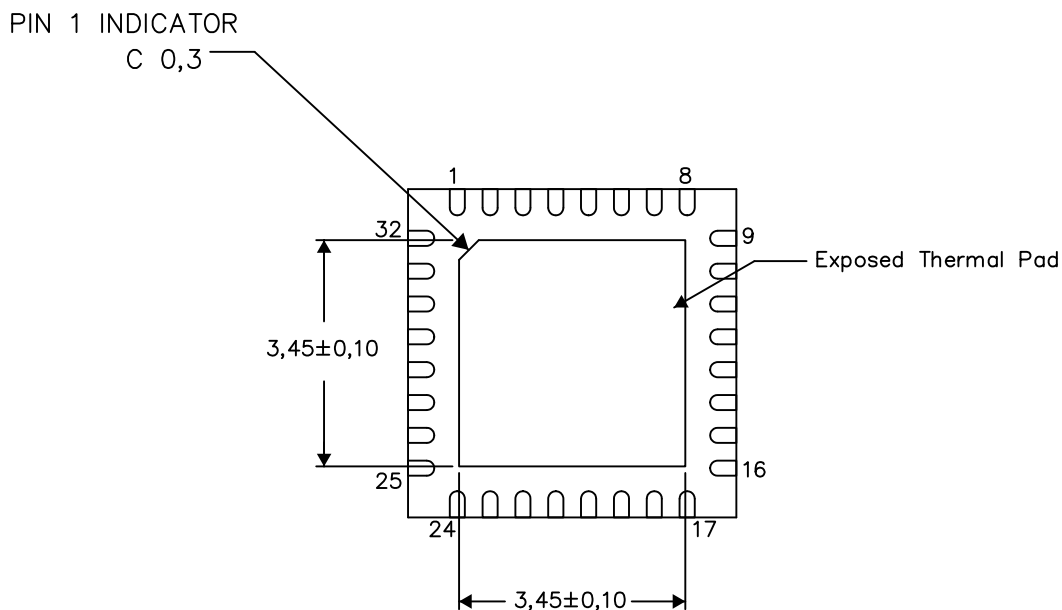
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

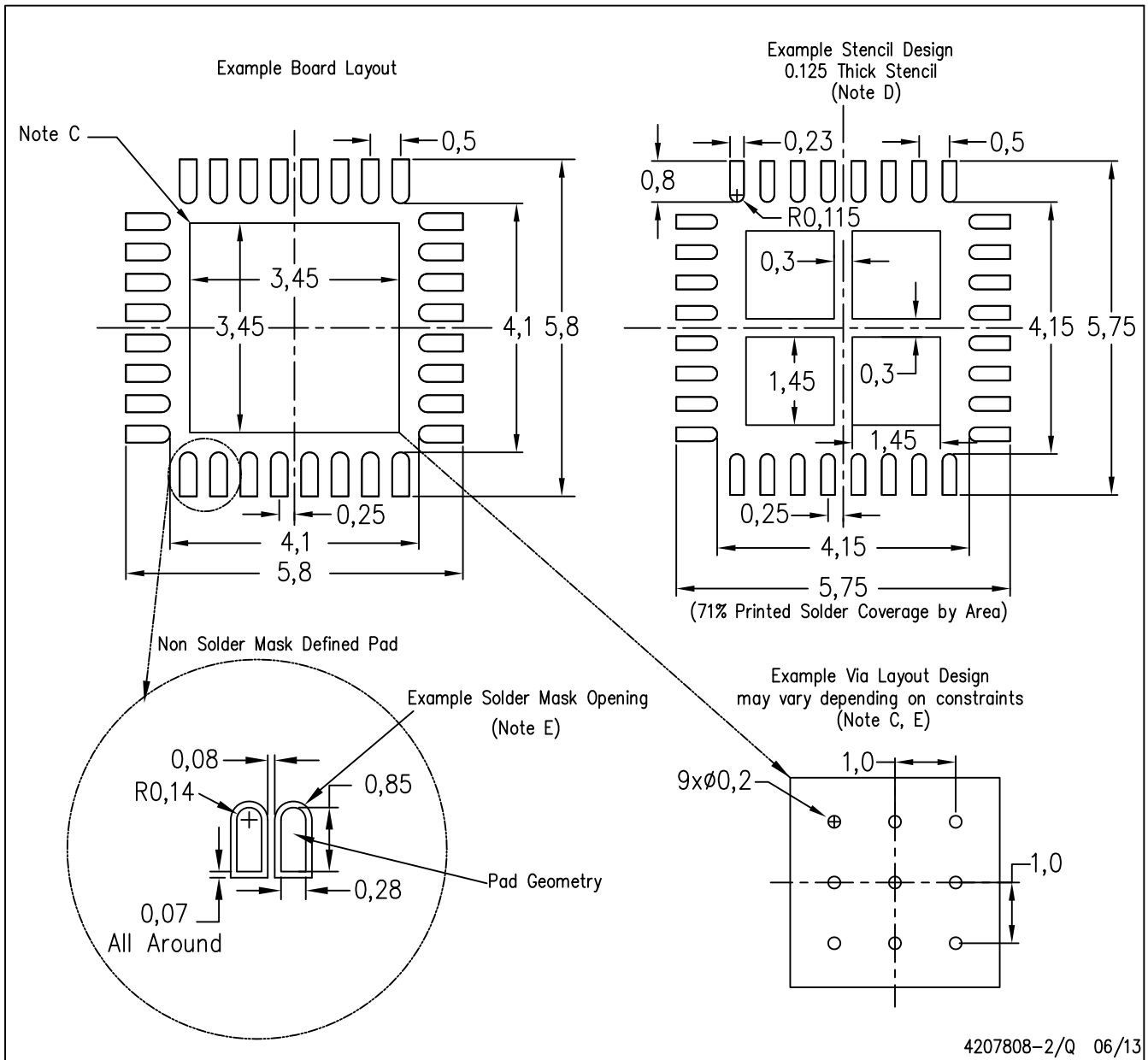
Exposed Thermal Pad Dimensions

4206356-2/Y 06/13

NOTE: A. All linear dimensions are in millimeters

RHB (S-PVQFN-N32)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

| | |
|------------------------------|--|
| Audio | www.ti.com/audio |
| Amplifiers | amplifier.ti.com |
| Data Converters | dataconverter.ti.com |
| DLP® Products | www.dlp.com |
| DSP | dsp.ti.com |
| Clocks and Timers | www.ti.com/clocks |
| Interface | interface.ti.com |
| Logic | logic.ti.com |
| Power Mgmt | power.ti.com |
| Microcontrollers | microcontroller.ti.com |
| RFID | www.ti-rfid.com |
| OMAP Applications Processors | www.ti.com/omap |
| Wireless Connectivity | www.ti.com/wirelessconnectivity |

Applications

| | |
|-------------------------------|--|
| Automotive and Transportation | www.ti.com/automotive |
| Communications and Telecom | www.ti.com/communications |
| Computers and Peripherals | www.ti.com/computers |
| Consumer Electronics | www.ti.com/consumer-apps |
| Energy and Lighting | www.ti.com/energy |
| Industrial | www.ti.com/industrial |
| Medical | www.ti.com/medical |
| Security | www.ti.com/security |
| Space, Avionics and Defense | www.ti.com/space-avionics-defense |
| Video and Imaging | www.ti.com/video |

TI E2E Community

e2e.ti.com