

## **TPS65053EVM-389**

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## **1 Introduction**

The Texas Instruments TPS65053EVM-389 evaluation module (EVM) enables designers to evaluate the operation and performance of the TPS65053 Power Management Integrate Circuit (PMIC) for applications that require multiple power rails and are powered from a single Lithium Ion or Lithium Polymer cell. The TPS65053 contains two efficient step-down switching converters, three low dropout (LDO) linear regulators and a voltage monitor RESET output.

The TPS65053EVM-389 is setup according to the power requirements of the Freescale™ i.MX27 processor.

## 2 Setup

This chapter describes the jumpers and connectors on the EVM, as well as how to properly connect, setup, and use the TPS65053EVM-389.

### 2.1 Input/Output Connector Descriptions

#### J1 - VLDO1

This header is the positive output of LDO1 linear regulator. This output is externally adjustable for the TPS65053 and is programmed to a value of 1.8 V on the EVM. The VLDO1 output is capable of supplying up to 400-mA. A load can be connected between J1 and J2 (GND). Applications using Freescale™ i.MX27 can utilize J1-VLDO1 to power the NVDD\_DDR, analog, and FUSEVDD rails of the i.MX27 processor.

#### J2 - GND

J2 is the return connection of VLDO1 output rail. A load can be connected between J2 and J1 (VLDO1).

#### J3 - VLDO2

This header is the positive output of LDO2 linear regulator. This output is externally adjustable for the TPS65053 and is programmed to a value of 1.4 V on the EVM. The VLDO2 output is capable of supplying up to 200 mA. A load can be connected between J3 and J4 (GND). Applications using Freescale™ i.MX27 can utilize J3-VLDO2 to power the RTCVDD and OSC32VDD rails of the i.MX27 processor.

#### J4 - GND

J4 is the return connection of VLDO2 output rail. A load can be connected between J4 and J3 (VLDO2).

#### J5 - VLDO3

This header is the positive output of LDO3 linear regulator. This output is fixed at 1.3 V for the TPS65053. The VLDO3 output is capable of supplying up to 200-mA. A load can be connected between J5 and J6 (GND).

#### J6 - GND

J6 is the return connection of VLDO3 output rail. A load can be connected between J6 and J5 (VLDO3).

#### J7 - RESET

This header allows the user to monitor the RESET output. The RESET output goes high 100-ms after the THRESHOLD input exceeds 1.0-V. RESET goes low when the THRESHOLD input falls below 1.0-V. On the EVM, the RESET circuitry monitors the outputs VOUT DCDC1 and VOUT DCDC2.

#### J8 - VOUT DCDC1

This header is the positive output of VDCDC1 step-down converter. This output is externally adjustable for the TPS65053 and is programmed to a value of 2.7-V on the EVM. VDCDC1 is capable of sourcing up to 1.0-A. A load can be connected between J8 and J9 (GND). Applications using Freescale™ i.MX27 can utilize J8-VOUT DCDC1 to power NVDD\_FAST, NVDD\_SLOW, and OSC26VDD of the i.MX27 processor.

#### J9 - GND

J9 is the return connection of VOUT VDCDC1 output rail. A load can be connected between J9 and J8 (VOUT DCDC1).

#### J10 - VIN

This header is the positive connection to the input power supply. The power supply must be connected between J10 and J11 (GND). The leads to the input supply should be twisted and kept as short as possible. The input voltage has to be between 2.5-V and 6-V.

#### J11 - GND

This header is the return connection to the input power supply. Connect the power supply between J11 and J10 (VIN). The leads to the input supply should be twisted and kept as short as possible. The input voltage has to be between 2.5-V and 6-V.

**J12 - VOUT DCDC2**

This header is the positive output of VDCDC2 step-down converter. This output is externally adjustable for the TPS65053 and is programmed to a value of 1.8-V on the EVM. VDCDC2 is capable of sourcing up to 600-mA. A load can be connected between J12 and J13 (GND). Applications using Freescale™ i.MX27 can utilize J12-VOUT DCDC2 to power the QVDD rail of the i.MX27 processor.

**J13 - GND**

J13 is the return connection of VOUT VDCDC2 output rail. A load can be connected between J13 and J12 (VOUT DCDC2).

**JP1 - VIN\_LDO1**

JP1 selects the input voltage source for LDO1.

Place a shorting bar in the VOUT\_DCDC1 position to select the output of VDCDC1 converter as input voltage source for LDO1.

Place a shorting bar in the VIN position to select the input voltage as input source for LDO1.

**JP2 - VIN\_LDO2/3**

JP2 selects the input voltage source for LDO2 and LDO3.

Place a shorting bar in the VOUT\_DCDC1 position to select the output of VDCDC1 converter as input voltage source for LDO2 and LDO3.

Place a shorting bar in the VIN position to select the input voltage as input source for LDO2 and LDO3.

**JP3 - EN\_LDO1**

Placing a shorting bar between EN LDO1 and ON ties the EN pin of LDO1 to VIN, thereby enabling LDO1. Placing a shorting bar between EN LDO1 and OFF ties the EN pin of LDO1 to GND, thereby disabling LDO1.

**JP4 - EN\_DCDC2**

Placing a shorting bar between EN\_DCDC2 and ON ties the EN pin of DCDC2 to VIN, thereby enabling DCDC2. Placing a shorting bar between EN\_DCDC2 and OFF ties the EN pin of DCDC2 to GND, thereby disabling DCDC2.

**JP5 - EN\_DCDC1**

Placing a shorting bar between EN\_DCDC1 and ON ties the EN pin of DCDC1 to VIN, thereby enabling DCDC1. Placing a shorting bar between EN\_DCDC1 and OFF ties the EN pin of DCDC1 to GND, thereby disabling DCDC1.

**JP6 - MODE Input**

JP6 selects the forced PWM or Power Save Mode (PSM) operation for the switching converters DCDC1 and DCDC2.

Placing a shorting bar between MODE and PWM ties the MODE pin of TPS65053 to VIN, thereby selecting forced PWM operating mode for the DCDC converters. Placing a shorting bar between MODE and PSM (Power Save Mode) ties the MODE pin of TPS65053 to GND, thereby selecting Power Save Mode operating mode for the DCDC converters at light-load conditions. If Power Save Mode is selected the DCDC converters will automatically switch to PWM mode at heavier load conditions.

**JP7 - EN\_LDO2**

Placing a shorting bar between EN LDO2 and ON ties the EN pin of LDO2 to VIN, thereby enabling LDO2. Placing a shorting bar between EN LDO2 and OFF ties the EN pin of LDO2 to GND, thereby disabling LDO2.

**JP8 - EN\_LDO3**

Placing a shorting bar between EN LDO3 and ON ties the EN pin of LDO3 to VIN, thereby enabling LDO3. Placing a shorting bar between EN LDO3 and OFF ties the EN pin of LDO3 to GND, thereby disabling LDO3.

## 2.2 EVM Setup

### 2.2.1 EVM Factory Configuration

The EVM is configured to provide the following nominal operating conditions:

- Input Voltage: 2.5-V to 6.0-V
- Output Voltage: See [Table 1](#)
- Maximum Load Current: See [Table 2](#)

**Table 1. EVM Preset Output Voltage**

Preset Output Voltage	TPS65053EVM
VDCDC1	2.7 V
VDCDC2	1.4 V
VLD01	1.8 V
VLD02	1.4 V
VLD03	1.3 V

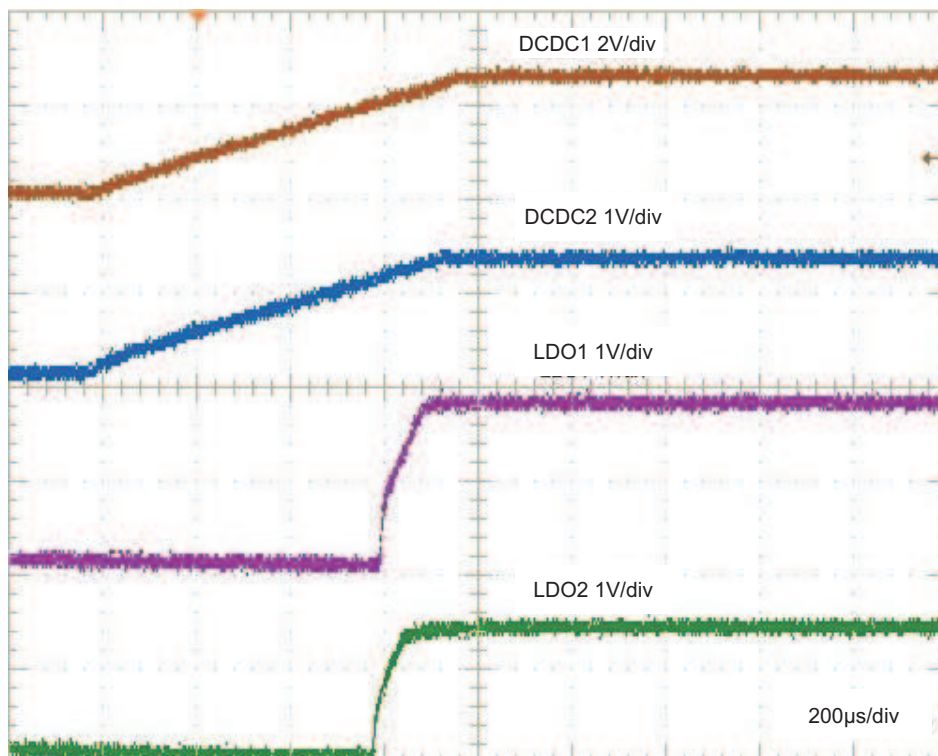
**Table 2. Maximum Load Current**

Maximum Load Current	TPS65053EVM
VDCDC1	1 A
VDCDC2	600 mA
VLD01	400 mA
VLD02	200 mA
VLD03	200 mA

## 2.3 Power Up Sequence

The TPS65053EVM-389 is set up to meet the Power Up requirements of the Freescale™ i.MX27 processor.

The step down converters DCDC1 and DCDC2 start up first, followed by the low drop out (LDO) regulators LDO1, LDO2 and LDO3 as shown in [Figure 1](#).



**Figure 1.**

## 2.4 Operation

1. Configure all EVM jumpers to factory settings shown in [Table 3](#).
2. Connect the input voltage return to J11.
3. Connect the positive input voltage to J10.
4. Connect all loads to the outputs.
5. Turn on input voltage.

**Table 3. Factory EVM Jumper Settings**

Jumper	Shunt Location
	TPS65053EVM
JP1	Between VOUT_DCDC1 and VIN_LDO1
JP2	Between VOUT_DCDC1 and VIN_LDO2
JP3	Between ON and EN_LDO1
JP4	Between ON and EN_DCDC2
JP5	Between ON and EN_DCDC1
JP6	Between PWM and MODE
JP7	Between ON and EN_LDO2
JP8	Between ON and EN_LDO3

### 3 Board Layout

This chapter provides the TPS65053EVM-389 board layout and illustrations.

#### 3.1 Layout

Figure 2 and Figure 3 show the board layout for the TPS65053EVM-389 PWB.

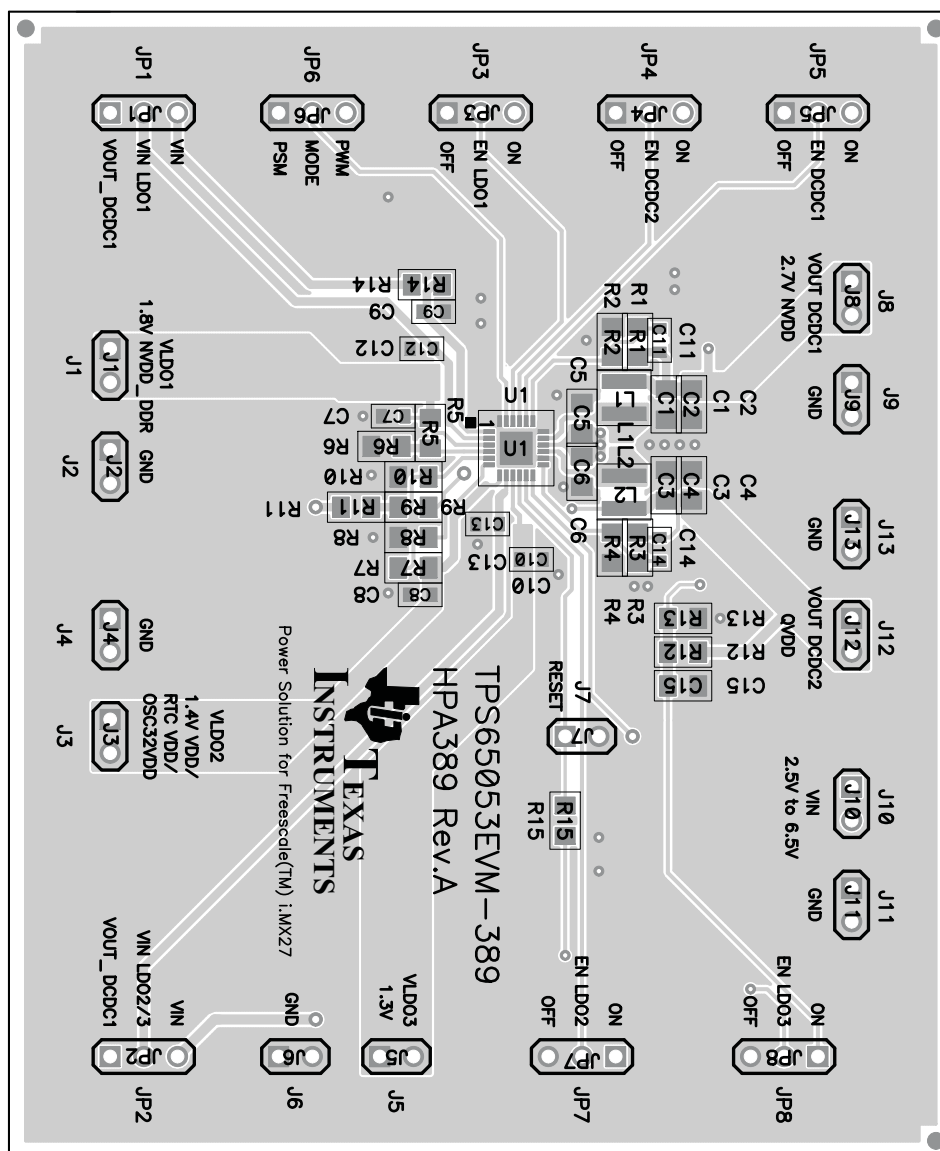
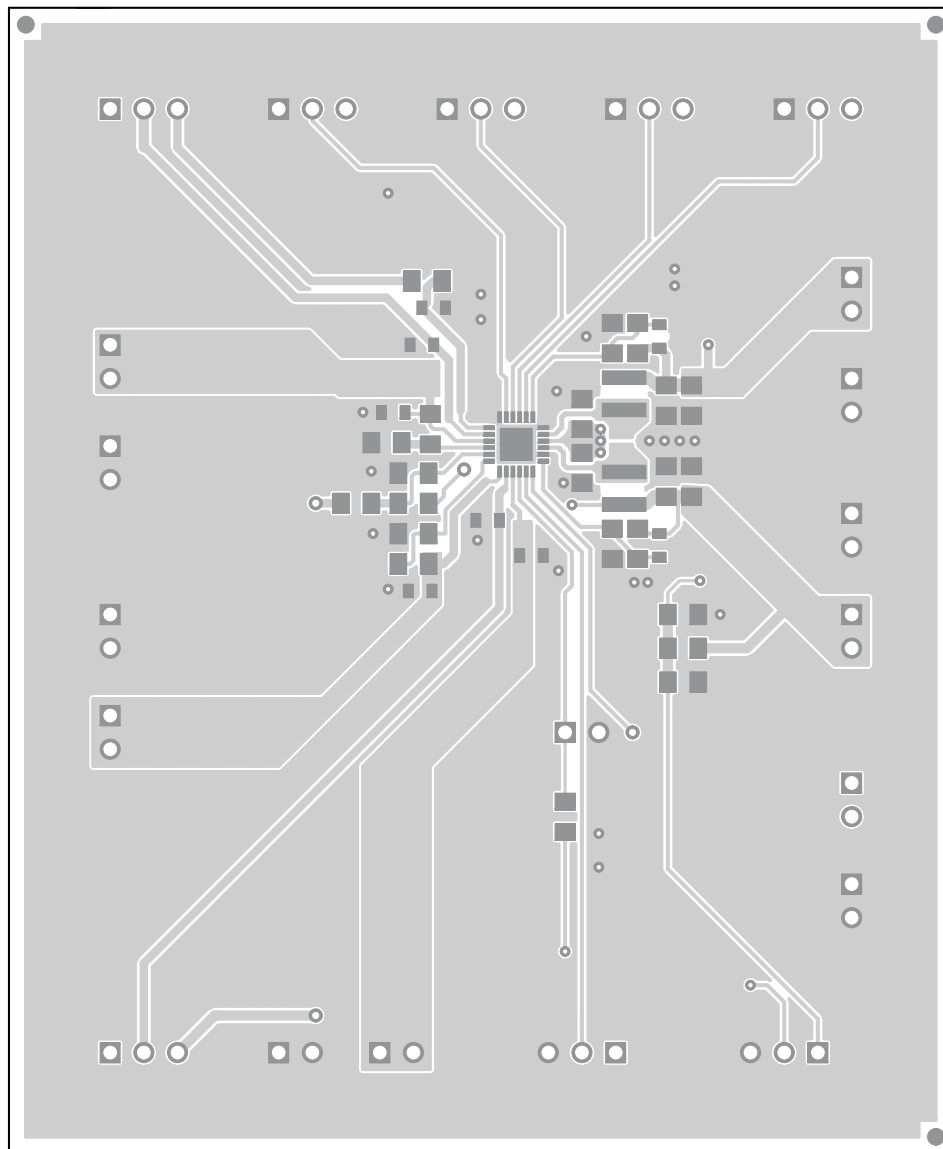
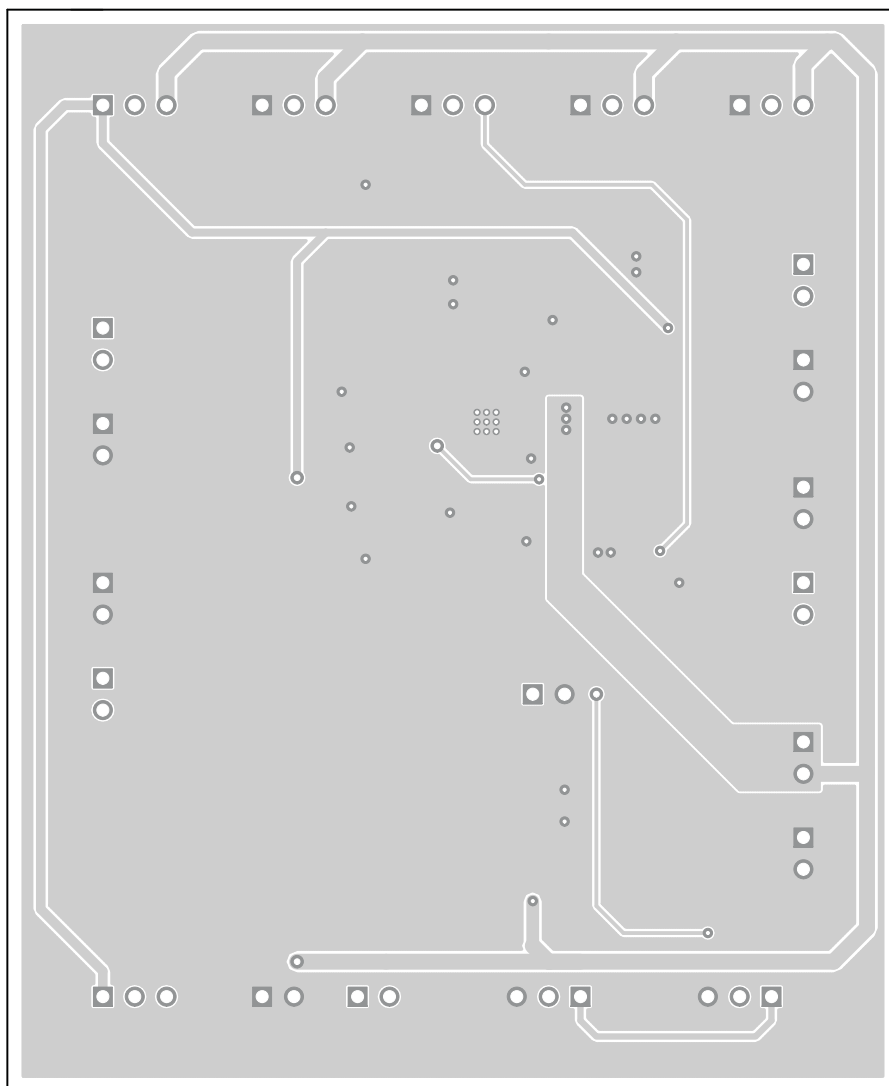


Figure 2. Assembly Layer



**Figure 3. Top Layer Routing**



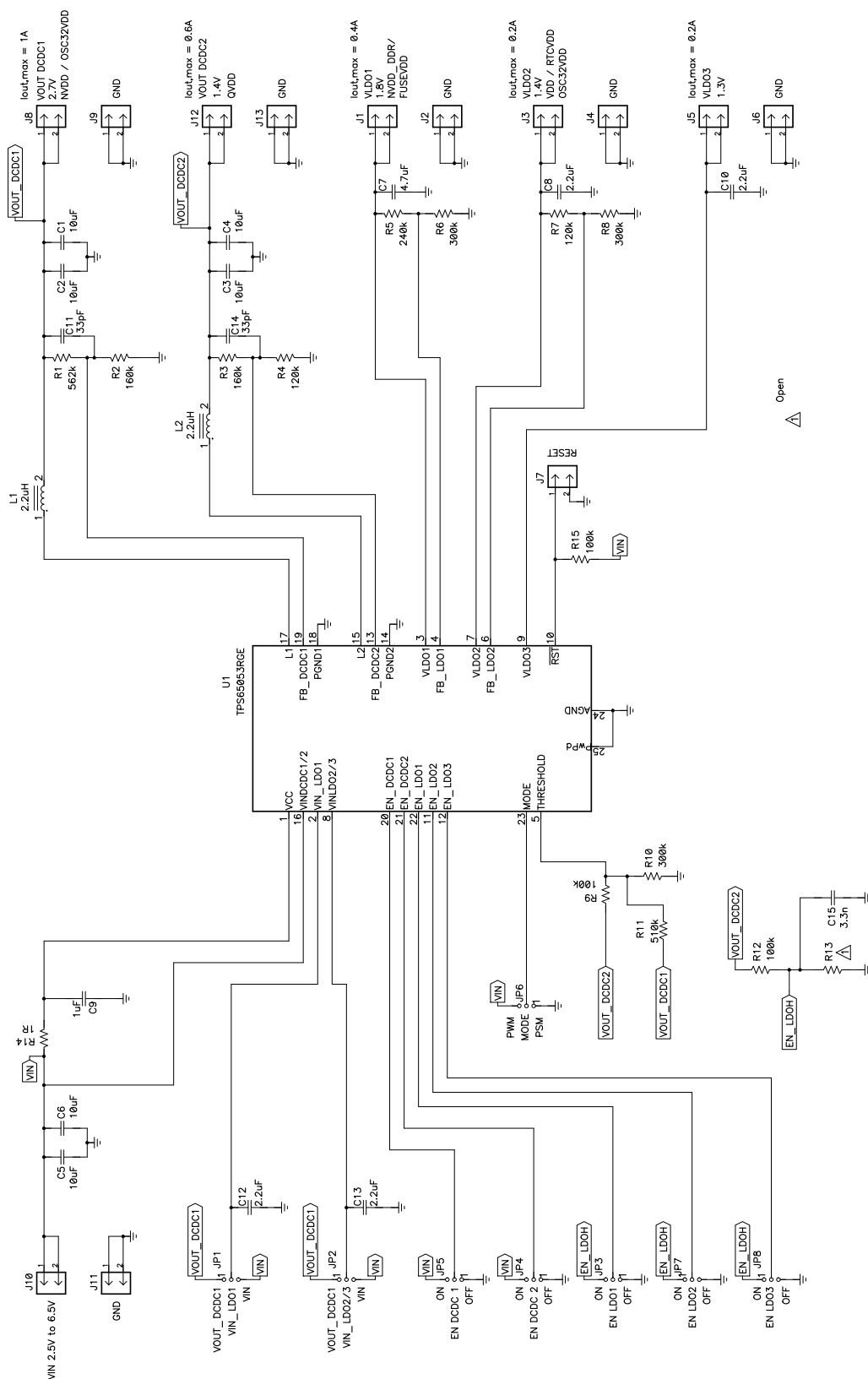
**Figure 4. Bottom Layer Routing**

## 4 Schematic and Bill of Materials

This chapter provides the TPS65053EVM-389 schematic and bill of materials.



### 4.1 Schematic



**Figure 5. TPS65053EVM-389 Schematic**

## 4.2 Bill of Materials

**Table 4. TPS65053EVM-389 Bill of Materials**

Count	RefDes	Value	Description	Size	Part Number	MFR
6	C1, C2, C3, C4, C5, C6	10uF	Capacitor, Ceramic, 10V, X5R, 10%	0805	GRM21BR61A106KE19L	muRata
2	C11, C14	33pF	Capacitor, Ceramic, 50V, C0G, 5%	0603	C1608C0G1H330J	TDK
1	C15	3.3nF	Capacitor, Ceramic, 6.3V, X5R, 10%	0805	Std	Std
1	C7	4.7uF	Capacitor, Ceramic, 6.3V, X5R, 20%	0603	GRM188R60J475ME19D	muRata
4	C8, C10, C12, C13	2.2uF	Capacitor, Ceramic, 10V, X5R, 10%	0603	GRM188R61A225KE34D	muRata
1	C9	1uF	Capacitor, Ceramic, 16V, X7R, 10%	0603	C1608X7R1C105K	TDK
12	J1, J2, J3, J4, J5, J6, J8, J9, J10, J11, J12, J13		Header, Male 2-pin, 100mil spacing	0.100 inch x 2		Any
1	J7		Header, 2-pin, 100mil spacing	0.100 inch x 2		Any
8	JP1, JP2, JP3, JP4, JP5, JP6, JP7, JP8		Header, 3-pin, 100mil spacing	0.100 inch x 3		Any
2	L1**, L2**	2.2uH	Inductor, SMT, 1.5A, 110milliohm	0.118 x 0.118 inch	LPS3015-222ML	Coilcraft
1	R1	562kΩ	Resistor, Chip, 1/10W, 1%	0805	Std	Std
1	R11	510kΩ	Resistor, Chip, 1/10W, 1%	0805	Std	Std
0	R13	open	Resistor, Chip, 1/10W, 1%	0805	Std	Std
1	R14	1R	Resistor, Chip, 1/10W, 1%	0805	Std	Std
2	R2, R3	160kΩ	Resistor, Chip, 1/10W, 1%	0805	Std	Std
2	R4, R7	120kΩ	Resistor, Chip, 1/10W, 1%	0805	Std	Std
1	R5	240kΩ	Resistor, Chip, 1/10W, 1%	0805	Std	Std
3	R6, R8, R10	300kΩ	Resistor, Chip, 1/10W, 1%	0805	Std	Std
3	R9, R12, R15	100kΩ	Resistor, Chip, 1/10W, 1%	0805	Std	Std
1	U1**	TPS65053RGE	IC, 2.25 MHz Dual Step-down Converter With 3 Low Input Voltage LDOs	QFN24	TPS65053RGE	TI
1	--		PCB, 3.4 In x 2.8 In x 0.062 In		HPA389	Any
8	--		Shunt, 100-mil, Black	0.100		Any

## Related Documentation From Texas Instruments

TPS65053 data sheet (SLVS754)

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### EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 2.5 V to 6 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 100°C. The EVM is designed to operate properly with certain components above 100°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
Optical Networking	<a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
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