

DEM-DAI1802 EVM

PCM1802 With Digital Audio Transmitter

User's Guide

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

EVM IMPORTANT NOTICE

Texas Instruments (TI) provides the enclosed product(s) under the following conditions:

This evaluation kit being sold by TI is intended for use for **ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY** and is not considered by TI to be fit for commercial use. As such, the goods being provided may not be complete in terms of required design-, marketing-, and/or manufacturing-related protective considerations, including product safety measures typically found in the end product incorporating the goods. As a prototype, this product does not fall within the scope of the European Union directive on electromagnetic compatibility and therefore may not meet the technical requirements of the directive.

Should this evaluation kit not meet the specifications indicated in the EVM User's Guide, the kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE.

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods. Please be aware that the products received may not be regulatory compliant or agency certified (FCC, UL, CE, etc.). Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge.

EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

TI currently deals with a variety of customers for products, and therefore our arrangement with the user is **not exclusive**.

TI assumes **no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein**.

Please read the EVM User's Guide and, specifically, the EVM Warnings and Restrictions notice in the EVM User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact the TI application engineer.

Persons handling the product must have electronics training and observe good laboratory practice standards.

No license is granted under any patent right or other intellectual property right of TI covering or relating to any machine, process, or combination in which such TI products or services might be or are used.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of ± 15 V and the output voltage range of ± 15 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 55°C. The EVM is designed to operate properly with certain components above 55°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

Preface

Read This First

About This Manual

This user's guide describes the construction and circuitry of the DEM-DAI1802 demonstration board. It also contains instructions for connecting and setting up the DEM-DAI1802 for operation.

How to Use This Manual

This document contains the following chapters:

Chapter 1 – *Description*

Chapter 2 – *Schematics and Printed-Circuit Board*

Related Documentation From Texas Instruments

PCM1802 Single-Ended Analog-Input 24-Bit, 96-kHz Stereo A/D Converter – Literature No. SLES023

FCC Warning

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

Contents

1	Description	1-1
1.1	Block Diagram	1-2
1.2	DEM-DAI1802 Basic Connection and Operation	1-2
1.2.1	Configuration Controls	1-2
2	Schematics and Printed-Circuit Board	2-1
2.1	DEM-DAI1802 Printed-Circuit Board	2-2
2.2	DEM-DAI1802 Schematics	2-5

Figures

1-1	DEM-DAI1802 Block Diagram	1-2
1-2	Digital Signal I/F to PCM1802 (JP052)	1-4
2-1	DEM-DAI1802 Silkscreen	2-2
2-2	DEM-DAI1802 Top View	2-3
2-3	DEM-DAI1802 Bottom View	2-4
2-4	DEM-DAI1802 Analog Section Schematic Diagram	2-5
2-5	DEM-DAI1802 A/D Converter Section Schematic Diagram	2-6
2-6	DEM-DAI1802 Regulator and Connector Schematic Diagram	2-6
2-7	DEM-DAI1802 Digital Section (Digital Audio Interface) Schematic Diagram	2-7

Tables

1–1	Analog Input Selection (JP101/102)—CN101/102 for 2 V RMS, CN103/104 for 1 V RMS	1-2
1–2	PCM1802: HPF Bypass Control (SW051)	1-2
1–3	PCM1802: Oversampling Control (SW051)—64 f _S or 128 f _S	1-3
1–4	PCM1802: Master/Slave and Oversampling Rate Selection (JP002/004/052 and SW002/051)	1-3
1–5	System-Clock Dividing Ratio for MCK: 128 f _S -CS8404 (JP001)	1-3
1–6	Bit-Clock Dividing Ratio (JP002)	1-3
1–7	LR-Clock Dividing Ratio (JP004)	1-3
1–8	Data Format Selection (JP003 and SW051)	1-4
1–9	System Clock Source Selection (JP005)—Internal Clock: X001/24.576 MHz, External Clock Input: CN001	1-4
1–10	Manual Reset (SW003)	1-4
1–11	S/PDIF Transmitter Format: CS8404 Configuration (SW004)	1-5

Description

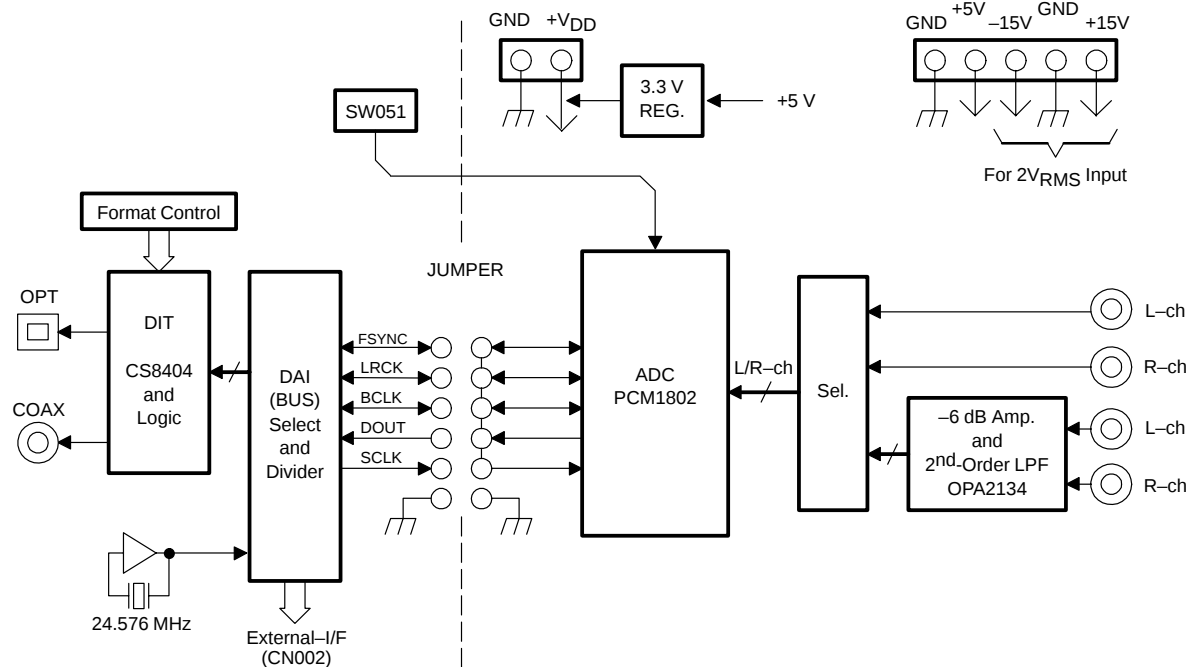
The DEM-DAI1802 is an evaluation board for the 96-kHz 24-bit PCM audio A/D converter, PCM1802, with digital audio transmitter, mode controls switch, onboard oscillator, –6 dB amplifier, and LPF.

The DEM-DAI1802 operates from 5 V and ± 15 V analog power supplies with a 1-V RMS or 2-V RMS unbalanced analog signal input.

Topic	Page
1.1 Block Diagram	1-2
1.2 DEM-DAI1802 Basic Connection and Operation	1-2

1.1 Block Diagram

Figure 1–1. DEM-DAI1802 Block Diagram



1.2 DEM-DAI1802 Basic Connection and Operation

- ❑ Connect the 5.0-V and ± 15 -V power supplies to the V_{CC} , AV_{CC} , $-AV_{CC}$, and GND on connectors CN051–CN055. The ± 15 -V supplies are required only for 2-V RMS input.
- ❑ Connect the S/PDIF output to CN003 (COAX) or U001 (OPT).
- ❑ Ensure the presence of a system clock, supplied from the onboard oscillator or external input clock connector (CN001) through switch/jumper to PCM1802.
- ❑ Set the data format using SW001, JP003, and SW051.
- ❑ Select the master or slave mode using SW002, SW051, JP002, JP004, and JP052.

1.2.1 Configuration Controls

Table 1–1. Analog Input Selection (JP101/102)—CN101/102 for 2 V RMS, CN103/104 for 1 V RMS

Input	Jumper-Pin Position
1-V RMS	Direct-IN
2-V RMS	–6dB/LPF

Table 1–2. PCM1802: HPF Bypass Control (SW051)

HPF Bypass	BYPAS (SW051)
Enable	H
Disable	L

Table 1–3. PCM1802: Oversampling Control (SW051)— $64 f_S$ or $128 f_S$

Oversampling	OSR (SW051)
$\times 128 f_S$	H
$\times 64 f_S$	L

Table 1–4. PCM1802: Master/Slave and Oversampling Rate Selection (JP002/004/052 and SW002/051)

MODE	SYSCLK	MODE1 (SW051)	MODE0 (SW051)	M/S select (SW002)	BCK sel (JP002)	LRCK sel (JP004)	FSYNC (JP052)
Master mode	$512 f_S$	L	H	Master	Remove jumper-pin	Remove jumper-pin	Remove jumper-pins
	$384 f_S$	H	L				
	$256 f_S$	H	H				
Slave mode	Auto-detect	L	L	Slave	Select /2, /4, or /8 (See Table 1–6)	Select /128, /256, or /512 (See Table 1–7)	Install SLAVE jumper-pin

Table 1–5. System-Clock Dividing Ratio for MCK: $128 f_S$ -CS8404 (JP001)

Dividing Ratio	Jumper-Pin	
	Position	MCK Value (24.576 MHz oscillator: default)
1/1	/1	—
1/2	/2	12.288 MHz ($128 f_S$ for $f_S = 96$ kHz)
1/4	/4	6.144 MHz ($128 f_S$ for $f_S = 48$ kHz)

Table 1–6. Bit-Clock Dividing Ratio (JP002)

Dividing Ratio	Jumper-Pin	
	Position	BCK Value (24.576 MHz oscillator: default)
1/2 (Slave)	/2	12.288 MHz ($64 f_S$ for $f_S = 192$ kHz)
1/4 (Slave)	/4	6.144 MHz ($64 f_S$ for $f_S = 96$ kHz)
1/8 (Slave)	/8	3.072 MHz ($64 f_S$ for $f_S = 48$ kHz)
— (Master)	Remove	—

Table 1–7. LR-Clock Dividing Ratio (JP004)

Dividing Ratio	Jumper-Pin	
	Position	MCK Value (24.576 MHz oscillator: default)
1/128 (Slave)	/128	192 kHz
1/256 (Slave)	/256	96 kHz
1/512 (Slave)	/512	48 kHz
— (Master)	Remove	—

Table 1–8. Data Format Selection (JP003 and SW051)

Data Format	JP003	FMT1	FMT0
PCM, left justified, 24 bit	L/J 24	L	L
PCM, I ² S, 24 bit	I ² S	L	H

Table 1–9. System Clock Source Selection (JP005)—Internal Clock: X001/24.576 MHz, External Clock Input: CN001

Clock Source	Jumper-Pin Position
Internal	INT
External	EXT

Table 1–10. Manual Reset (SW003)

Reset switch for CS8404

Figure 1–2. Digital Signal I/F to PCM1802 (JP052)

The digital signals generated by the internal oscillator, divider, and PCM1802 are input to this jumper. For each shorted pin the corresponding digital signal is input to the PCM1802 and CS8404.

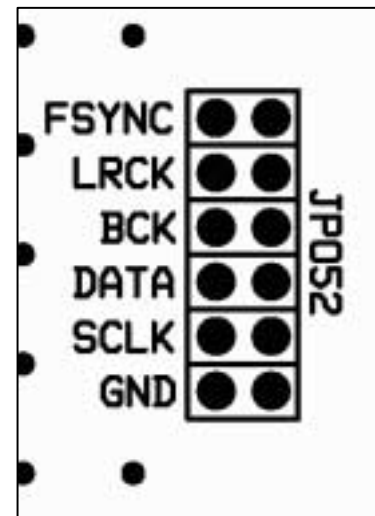


Table 1–11. S/PDIF Transmitter Format: CS8404 Configuration (SW004)

Professional Mode			Consumer Mode		
Switch	L=0, H=1		Switch	L=0, H=1	
PRO	0	Professional mode	PRO	1	Consumer mode
C9		C8,C9,C10,C11 – Channel mode (1 of 4)	C15		Generation status
	1	0000 – Not indicated (default: 2-ch)		1	0 – (see the S/PDIF standard)
	0	0100 – Stereophonic		0	1 – (see the S/PDIF standard)
EM1,EM0		C2,C3,C4 – Emphasis (2 of 3)	C8,C9		C8–C14 – Category code (2 of 7)
	1 1	Not indicated (default: none)		1 1	0000 0000 – General
	1 0	No emphasis		1 0	0100 0000 – PCM encoder/decoder
	0 1	50/15Us		0 1	1000 0000 – CD
	0 0	CCITT J.17		0 0	1100 0000 – DAT
C6,C7		C6,C7 – Sample frequency	C3		C3,C4,C5 – Emphasis (1 of 3)
	1 1	Not indicated (default: 48 kHz)		1	000 – None
	1 0	48 kHz		0	100 – 50/15Us
	0 1	44.1 kHz	C2		C2 – Copy/copyright
	0 0	32 kHz		1	0 – Copy inhibited/copyright asserted
C1		C1 – Audio	FC1, FC0		C24,C25,C26,C27 – Sample frequency
	1	0 – Normal audio		1 1	44.1 kHz
	0	1 – Nonaudio		1 0	48 kHz
TRNPT		Transparent mode		0 1	32 kHz
	0	0 – Normal operation		0 0	44.1 kHz, CD mode
	1	1 – Transparent mode			

Schematics and Printed-Circuit Board

This chapter presents the DEM-DAI1802 printed-circuit board and the DEM-DAI1802 schematics.

Topic	Page
2.1 DEM-DAI1802 Printed-Circuit Board	2-2
2.2 DEM-DAI1802 Schematics	2-5

2.1 DEM-DAI1802 Printed-Circuit Board

Figure 2–1. DEM-DAI1802 Silkscreen

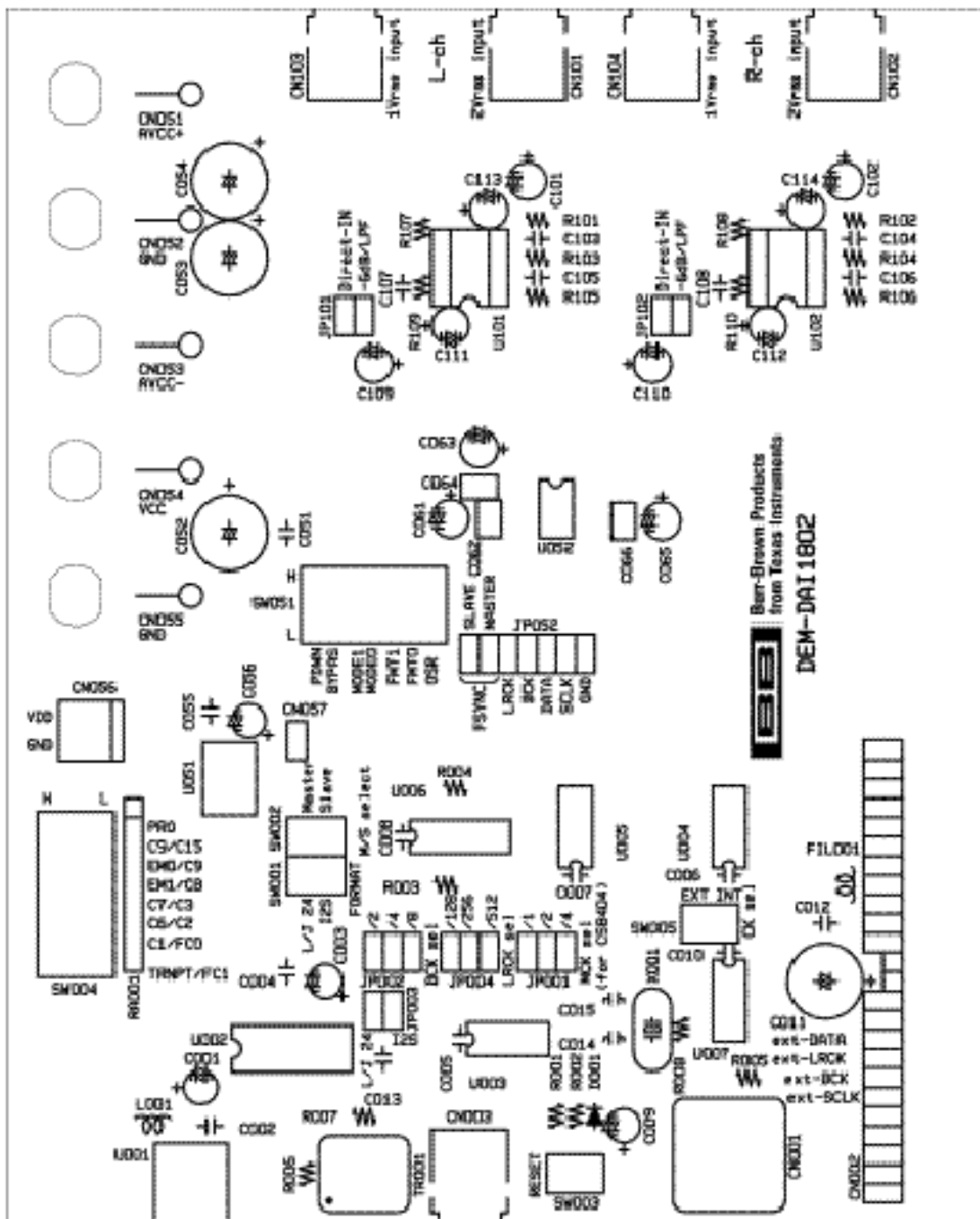


Figure 2–2. DEM-DAI1802 Top View

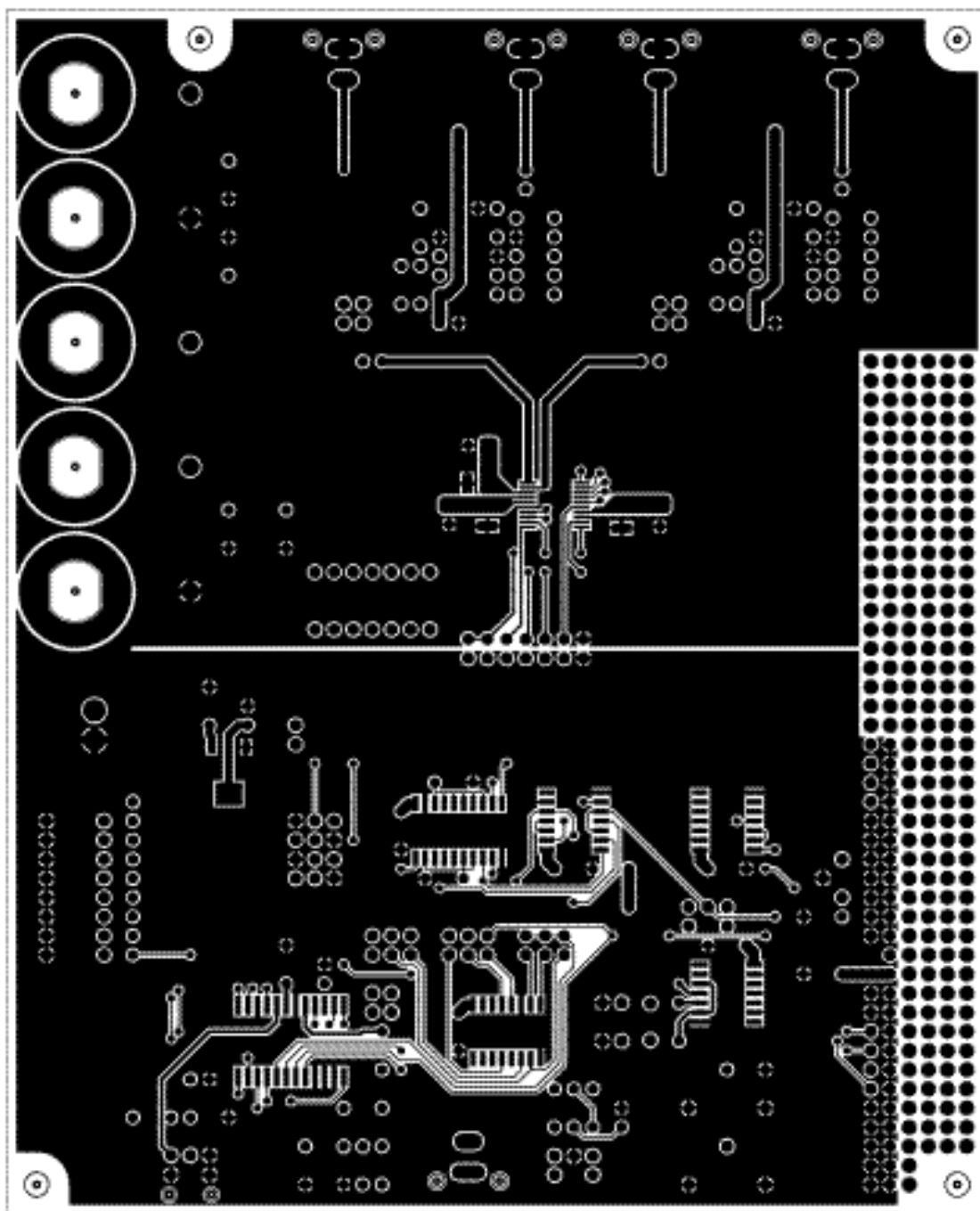
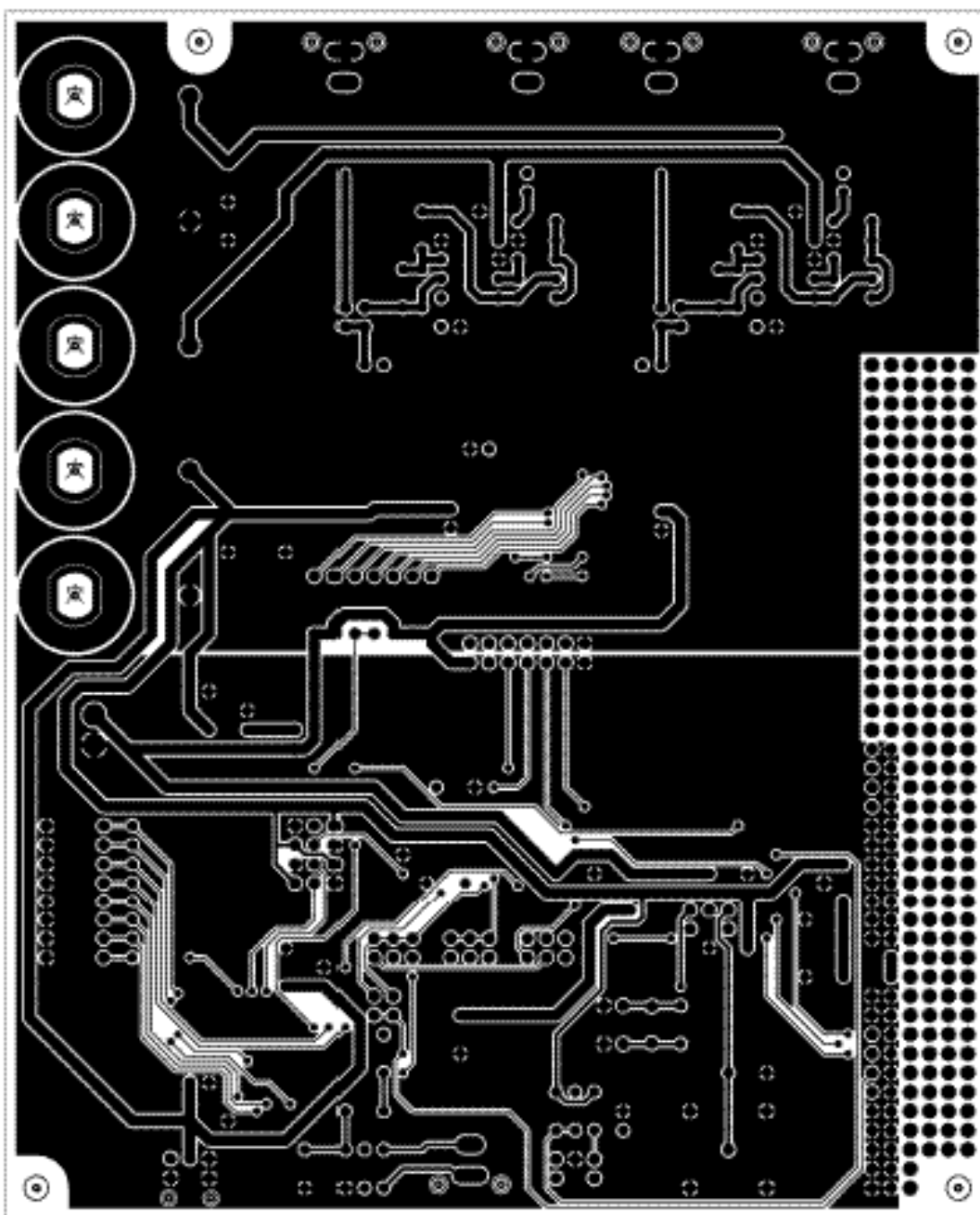


Figure 2–3. DEM-DAI1802 Bottom View



2.2 DEM-DAI1802 Schematics

Figure 2–4. DEM-DAI1802 Analog Section Schematic Diagram

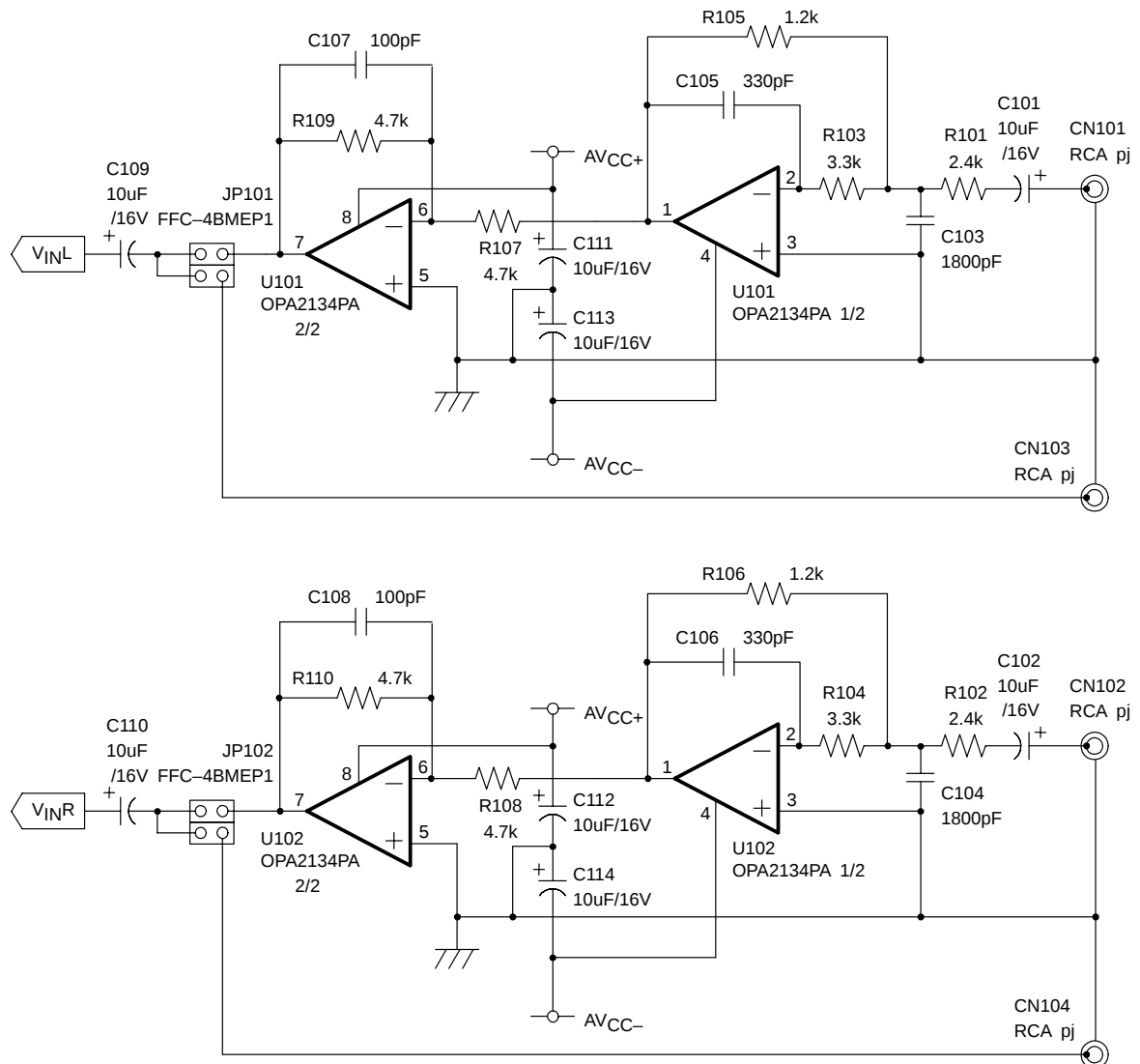


Figure 2–5. DEM-DAI1802 A/D Converter Section Schematic Diagram

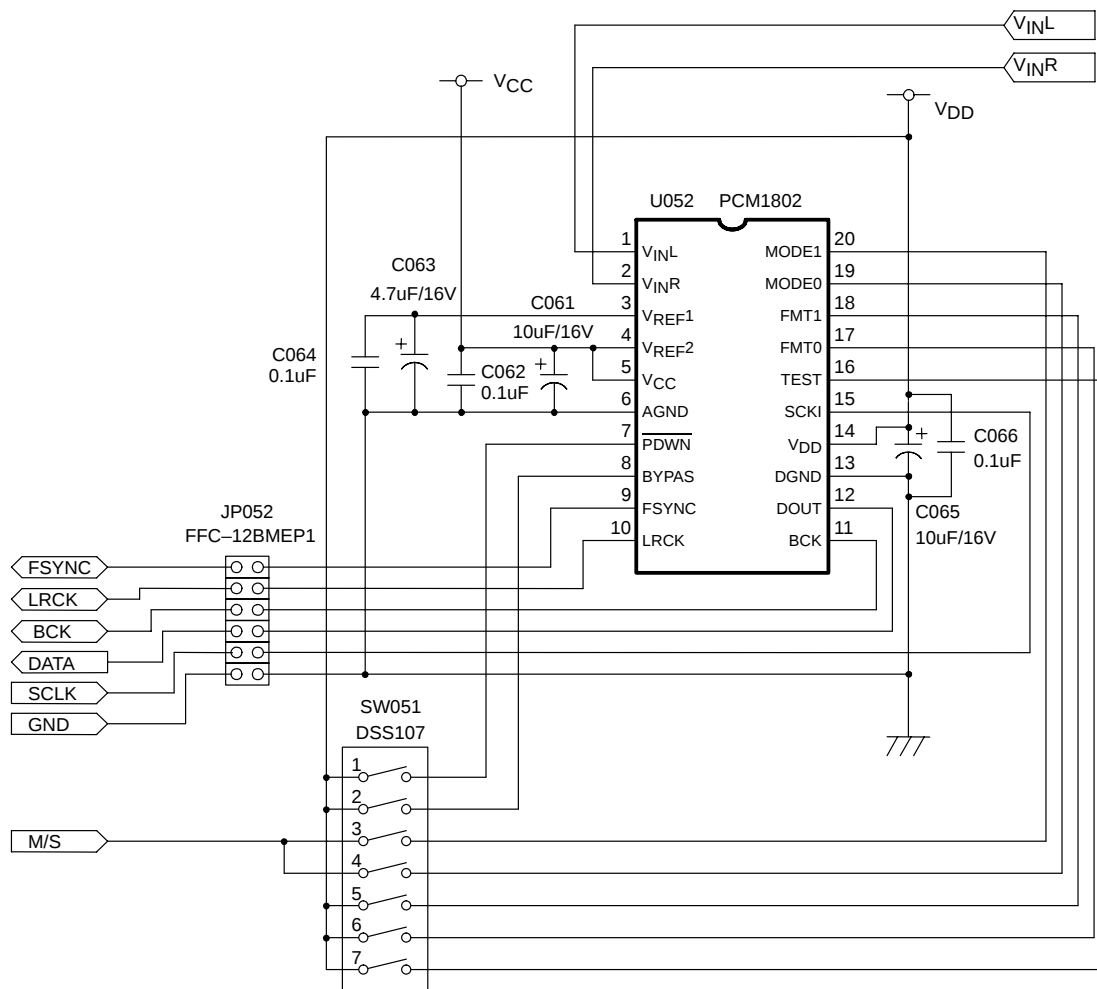


Figure 2–6. DEM-DAI1802 Regulator and Connector Schematic Diagram

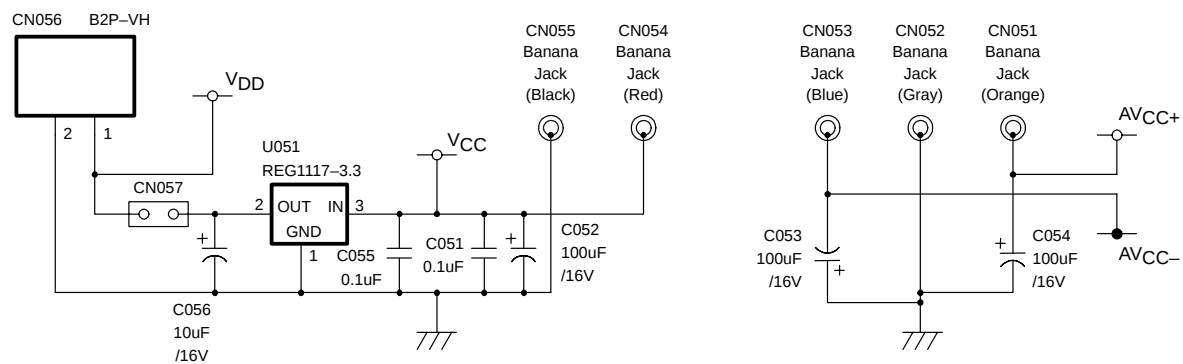


Figure 2–7. DEM-DAI1802 Digital Section (Digital Audio Interface) Schematic Diagram

