

## **MSP430G2112 Device Erratasheet**

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### **1 Revision History**

✓ The check mark indicates that the issue is present in the specified revision.

Errata Number	Rev B	Rev A
<a href="#">BCL12</a>	✓	✓
<a href="#">BCL14</a>	✓	✓
<a href="#">CPU4</a>	✓	✓
<a href="#">EEM20</a>	✓	✓
<a href="#">SYS15</a>	✓	✓
<a href="#">TA12</a>	✓	✓
<a href="#">TA16</a>	✓	✓
<a href="#">TA21</a>	✓	✓
<a href="#">TAB22</a>	✓	✓
<a href="#">USI4</a>	✓	✓
<a href="#">USI5</a>	✓	✓
<a href="#">XOSC5</a>	✓	✓

## 2 Package Markings

### N20

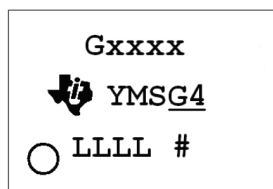
#### PDIP (N), 20 Pin



YM = Year and Month Date Code  
 LLLL = LOT Trace Code  
 S = Assembly Site Code  
 # = DIE Revision

### PW14

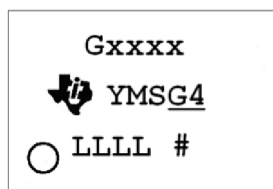
#### TSSOP (PW), 14 Pin



YM = Year and Month Date Code  
 LLLL = LOT Trace Code  
 S = Assembly Site Code  
 # = DIE Revision  
 o = PIN 1

### PW20

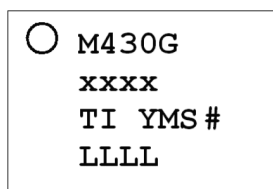
#### TSSOP (PW), 20 Pin



YM = Year and Month Date Code  
 LLLL = LOT Trace Code  
 S = Assembly Site Code  
 # = DIE Revision  
 o = PIN 1

### RSA16

#### QFN (RSA), 16 Pin



YM = Year and Month Date Code  
 LLLL = LOT Trace Code  
 S = Assembly Site Code  
 # = DIE Revision  
 o = PIN 1

### 3 Detailed Bug Description

#### BCL12 *BCS Module*

**Function** Switching RSELx or modifying DCOCTL can cause DCO dead time or a complete DCO stop

**Description** After switching RSELx bits (located in register BCSTL1) from a value of >13 to a value of <12 OR from a value of <12 to a value of >13, the resulting clock delivered by the DCO can stop before the new clock frequency is applied. This dead time is approximately 20 us. In some instances, the DCO may completely stop, requiring a power cycle.

Furthermore, if all of the RSELx bits in the BCSTL1 register are set, modifying the DCOCTL register to change the DCOx or the MODx bits could also result in DCO dead time or DCO hang up.

**Workaround** - When switching RSEL from >13 to <12, use an intermediate frequency step. The intermediate RSEL value should be 13.

Current RSEL	Target RSEL	Recommended Transition Sequence
15	14	Switch directly to target RSEL
14 or 15	13	Switch directly to target RSEL
14 or 15	0 to 12	Switch to 13 first, and then to target RSEL (two step sequence)
0 to 13	0 to 12	Switch directly to target RSEL

AND

- When switching RSEL from <12 to >13 it's recommended to set RSEL to its default value first (RSEL = 7) before switching to the desired target frequency.

AND

- In case RSEL is at 15 (highest setting) it's recommended to set RSEL to its default value first (RSEL = 7) before accessing DCOCTL to modify the DCOx and MODx bits. After the DCOCTL register modification the RSEL bits can be manipulated in an additional step.

In the majority of cases switching directly to intermediate RSEL steps as described above will prevent the occurrence of BCL12. However, a more reliable method can be implemented by changing the RSEL bits step by step in order to guarantee safe function without any dead time of the DCO.

Note that the 3-step clock startup sequence consisting of clearing DCOCTL, loading the BCSTL1 target value, and finally loading the DCOCTL target value as suggested in the in the "TLV Structure" chapter of the [MSP430x2xx Family User's Guide](#) is not affected by BCL12 if (and only if) it is executed after a device reset (PUC) prior to any other modifications being made to BCSTL1 since in this case RSEL still is at its default value of 7. However any further changes to the DCOx and MODx bits will require the consideration of the workaround outlined above.

#### BCL14 *BCS Module*

**Function** Oscillator fault forced in bypass mode when P2SEL.7 bit is not set

**Description** When the LFXT1 oscillator is used in bypass mode and P2SEL.7 is not set, the oscillator fault flag (OFIFG) will be forced to set and cannot be cleared. Due to the failsafe logic, LFXT1 cannot be used as MCLK in this case. The bug only affects the behavior of the

oscillator fault, the clocking itself works properly.

**Workaround**

Set both P2SEL.6 and P2SEL.7 if the application requires correct function of the oscillator fault flag (e.g. MCLK failsafe logic).

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**NOTE:** Setting P2SEL.7 bit disables the GPIO functionality and enables the input schmitt trigger of the pin. P2.7 should be tied to a fixed voltage level (VCC or GND) to prevent cross current.

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**CPU4**
***CPU Module***


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**Function**

PUSH #4, PUSH #8

**Description**

The single operand instruction PUSH cannot use the internal constants (CG) 4 and 8. The other internal constants (0, 1, 2, -1) can be used. The number of clock cycles is different:

PUSH #CG uses address mode 00, requiring 3 cycles, 1 word instruction

PUSH #4/#8 uses address mode 11, requiring 5 cycles, 2 word instruction

**Workaround**

Workaround implemented in assembler.

**EEM20**
***EEM Module***


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**Function**

Debugger might clear interrupt flags

**Description**

During debugging read-sensitive interrupt flags might be cleared as soon as the debugger stops. This is valid in both single-stepping and free run modes.

**Workaround**

None.

**SYS15**
***SYS Module***


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**Function**

LPM3 and LPM4 currents exceed specified limits

**Description**

LPM3 and LPM4 currents may exceed specified limits if the SMCLK source is switched from DCO to VLO or LFXT1 just before the instruction to enter LPM3 or LPM4 mode.

**Workaround**

After clock switching, a delay of at least four new clock cycles (VLO or LFXT1) must be implemented to complete the clock synchronization before going into LPM3 or LPM4.

**TA12**
***TIMER\_A Module***


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**Function**

Interrupt is lost (slow ACLK)

**Description**

Timer\_A counter is running with slow clock (external TACLK or ACLK) compared to MCLK. The compare mode is selected for the capture/compare channel and the CCRx register is incremented by one with the occurring compare interrupt (if TAR = CCRx). Due to the fast MCLK the CCRx register increment (CCRx = CCRx+1) happens before the Timer\_A counter has incremented again. Therefore the next compare interrupt should happen at once with the next Timer\_A counter increment (if TAR = CCRx + 1). This interrupt gets lost.

**Workaround** Switch capture/compare mode to capture mode before the CCRx register increment. Switch back to compare mode afterwards.

## TA16 *TIMER\_A Module*

**Function** First increment of TAR erroneous when IDx > 00

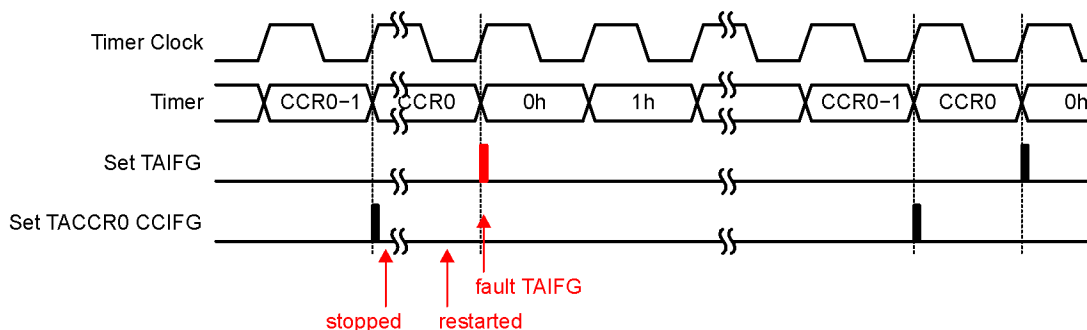
**Description** The first increment of TAR after any timer clear event (POR/TACLR) happens immediately following the first positive edge of the selected clock source (INCLK, SMCLK, ACLK or TACLK). This is independent of the clock input divider settings (ID0, ID1). All following TAR increments are performed correctly with the selected IDx settings.

**Workaround** None

## TA21 *TIMER\_A Module*

**Function** TAIFG Flag is erroneously set after Timer A restarts in Up Mode

**Description** In Up Mode, the TAIFG flag should only be set when the timer resets from TACCR0 to zero. However, if the Timer A is stopped at TAR = TACCR0, then cleared (TAR=0) by setting the TACLR bit, and finally restarted in Up Mode, the next rising edge of the TACLK will erroneously set the TAIFG flag.



**Workaround** None.

## TAB22 *TIMER\_A/TIMER\_B Module*

**Function** Timer\_A/Timer\_B register modification after Watchdog Timer PUC

**Description** Unwanted modification of the Timer\_A/Timer\_B registers TACTL/TBCTL and TAIV/TBIV can occur when a PUC is generated by the Watchdog Timer(WDT) in Watchdog mode and any Timer\_A/Timer\_B counter register TACCRx/TBCCRx is incremented/decremented (Timer\_A/Timer\_B does not need to be running).

**Workaround** Initialize TACTL/TBCTL register after the reset occurs using a MOV instruction (BIS/BIC may not fully initialize the register). TAIV/TBIV is automatically cleared following this initialization.

Example code:

```
MOV.W #VAL, &TACTL
```

or

```
MOV.W #VAL, &TBCTL
```

Where, VAL=0, if Timer is not used in application otherwise, user defined per desired function.

## **USI4**

### ***USI Module***

#### **Function**

I2C Slave mode can generate a glitch at SCL

#### **Description**

USI I2C Slave Operation at slower communication rates (less than 20kbps). During I2C bus active operation, if USICNT is written while SCL is high, I2C module will generate a glitch on SCL that can corrupt the I2C bus sequence.

#### **Workaround**

Verify that SCL is low before writing USICNT register.

## **USI5**

### ***USI Module***

#### **Function**

SPI master generates one additional clock after module reset

#### **Description**

Initializing the USI in SPI MASTER mode with the USICKPH bit set generates one additional clock pulse than defined by the value in the USICNTx bits on the SCLK pin during the first data transfer after module reset. For example, if the USICNTx bits hold the value eight, nine clock pulses are generated on the SCLK pin for the first transfer only.

#### **Workaround**

Load USICNTx with a count of N-1 bits (where N is the required number of bits) for the first transfer only.

## **XOSC5**

### ***XOSC Module***

#### **Function**

LF crystal failures may not be properly detected by the oscillator fault circuitry

#### **Description**

The oscillator fault error detection of the LFXT1 oscillator in low frequency mode (XTS = 0) may not work reliably causing a failing crystal to go undetected by the CPU, i.e. OFIFG will not be set.

#### **Workaround**

None

## **4 Document Revision History**

Changes from family erratasheet to device specific erratasheet.

1. Errata EEM20 was added
2. Errata TA22 was renamed to TAB22
3. Description for TAB22 was updated

Changes from device specific erratasheet to document Revision A.

1. USI5 Workaround was updated.

Changes from document Revision A to Revision B.

1. BCL12 Workaround was updated.

Changes from document Revision B to Revision C.

1. Errata TA21 was added to the errata documentation.

Changes from document Revision C to Revision D.

1. Silicon Revision B was added to the errata documentation.

Changes from document Revision D to Revision E.

1. BCL14 Workaround was updated.

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