

MSP430F167 Device Erratasheet

1 Revision History

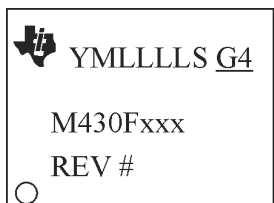
✓ The check mark indicates that the issue is present in the specified revision.

Errata Number	Rev E	Rev D	Rev C	Rev B
ADC18	✓	✓	✓	✓
ADC25	✓	✓	✓	✓
BCL5	✓	✓	✓	✓
CPU4	✓	✓	✓	✓
I2C7	✓	✓	✓	✓
I2C8	✓	✓	✓	✓
I2C9	✓	✓	✓	✓
I2C10	✓	✓	✓	✓
I2C11	✓	✓	✓	✓
I2C12	✓	✓	✓	✓
I2C13	✓	✓	✓	✓
I2C14	✓	✓	✓	✓
I2C15	✓	✓	✓	✓
I2C16	✓	✓	✓	✓
MPY2	✓	✓	✓	✓
SVS2			✓	✓
TA12	✓	✓	✓	✓
TA16	✓	✓	✓	✓
TA21	✓	✓	✓	✓
TAB22	✓	✓	✓	✓
TB2	✓	✓	✓	✓
TB16	✓	✓	✓	✓
TB24	✓	✓	✓	✓
US14			✓	✓
US15	✓	✓	✓	✓
WDG2	✓	✓	✓	✓
XOSC4				✓

2 Package Markings

PM64

LQFP (PM), 64 Pin

	YM = Year and Month Date Code LLLL = LOT Trace Code S = Assembly Site Code # = DIE Revision ○ = Pin 1
---	---

RTD64

QFN (RTD), 64 Pin

○ M430Fxxx TI YMS LLLL #	TI = TI YM = Year and Month Date Code LLLL = LOT Trace Code S = Assembly Site Code # = DIE Revision ○ = Pin 1
○ M430Fxxx TI YMS G3 LLLL #	TI = TI YM = Year and Month Date Code LLLL = LOT Trace Code S = Assembly Site Code # = DIE Revision ○ = Pin 1

3 Detailed Bug Description

ADC18	ADC12 Module
Function	Incorrect conversion result in extended sample mode
Description	<p>The ADC12 conversion result can be incorrect if the extended sample mode is selected (SHP = 0), the conversion clock is not the internal ADC12 oscillator (ADC12SSEL > 0), and one of the following two conditions is true:</p> <ul style="list-style-type: none"> - The extended sample input signal SHI is asynchronous to the clock source used for ADC12CLK and the undivided ADC12 input clock frequency exceeds 3.15 MHz. <p>or</p> <ul style="list-style-type: none"> - The extended sample input signal SHI is synchronous to the clock source used for ADC12CLK and the undivided ADC12 input clock frequency exceeds 6.3 MHz.
Workaround	<ul style="list-style-type: none"> - Use the pulse sample mode (SHP = 1). <p>or</p> <ul style="list-style-type: none"> - Use the ADC12 internal oscillator as the ADC12 clock source. <p>or</p> <ul style="list-style-type: none"> - Limit the undivided ADC12 input clock frequency to 3.15 MHz. <p>or</p> <ul style="list-style-type: none"> - Use the same clock source (such as ACLK or SMCLK) to derive both SHI and ADC12CLK, to achieve synchronous operation, and also limit the undivided ADC12 input clock frequency to 6.3 MHz.
ADC25	ADC12 Module
Function	Write to ADC12CTL0 triggers ADC12 when CONSEQ = 00
Description	<p>If ADC conversions are triggered by the Timer_B module and the ADC12 is in single-channel single-conversion mode (CONSEQ = 00), ADC sampling is enabled by write access to any bit(s) in the ADC12CTL0 register. This is contrary to the expected behavior that only the ADC12 enable conversion bit (ADC12ENC) triggers a new ADC12 sample.</p>
Workaround	<p>When operating the ADC12 in CONSEQ=00 and a Timer_B output is selected as the sample and hold source, temporarily clear the ADC12ENC bit before writing to other bits in the ADC12CTL0 register. The following capture trigger can then be re-enabled by setting ADC12ENC = 1.</p>
BCL5	BCS Module
Function	RSELx bit modifications can generate high frequency spikes on MCLK
Description	<p>When DIVMx = 00 or 01 the RSELx bits of the Basic Clock Module are incremented or decremented in steps of 2 or greater, the DCO output may momentarily generate high frequency spikes on MCLK, which may corrupt CPU operation. This is not an issue when DIVMx = 10 or 11.</p>
Workaround	<p>Set DIVMx = 10 or 11 to divide the MCLK input prior to modifying RSELx. After the RSELx bits are configured as desired, the DIVMx setting can be changed back to the original selection.</p>

CPU4
CPU Module
Function

PUSH #4, PUSH #8

Description

The single operand instruction PUSH cannot use the internal constants (CG) 4 and 8. The other internal constants (0, 1, 2, -1) can be used. The number of clock cycles is different:

PUSH #CG uses address mode 00, requiring 3 cycles, 1 word instruction

PUSH #4/#8 uses address mode 11, requiring 5 cycles, 2 word instruction

Workaround

Workaround implemented in assembler.

I2C7
USART Module
Function

ARDYIFG Interrupt flag generation can fail in I2C slave mode.

Description

When the USART is configured for I2C mode (U0CTL.I2C, SYNC, and I2CEN are set) and the module is configured as an I2C slave (U0CTL.MST=0), the ARDYIFG interrupt flag generation can fail, even when both the I2C stop condition is received and the receive buffer is empty.

This condition occurs when the I2C clock source selected by I2CSSELx is disabled by the Status Register (SR) control signals OSCOFF or SCG1.

In this configuration, the hardware clock activation is enabled by the I2C module. However, if RXRDYIFG is polled to determine data reception, the I2C hardware clock activation may be disabled before the ARDYIFG is generated.

Workaround

(1)Use interrupt service routines using the I2C interrupt vector generator feature (I2CIV) to handle all I2C interrupts.

OR

(2)After detection of I2C Own Address (OAIFG), the selected I2C clock source is enabled by clearing the OSCOFF or SCG1 Status Register (SR) bits. When the ARDYIFG is detected, the OSCOFF or SCG1 in the Status Register (SR) can be set to disable the clock source and return to the desired low power mode operation.

OR

(3)For slave only devices, it is normally not necessary to use ARDYIFG.

I2C8
USART Module
Function

Master Transmitter transmits 0FFh continuously.

Description

When the USART is configured for I2C mode (U0CTL.I2C, SYNC, and I2CEN are set) and the module is configured as an I2C master (U0CTL.MST=1) and I2CNDAT is used to control the number of bytes to transmit, the possibility exists that the master state-machine can become corrupted and start sending 0FFh as data on the I2C bus. Specifically, this error can occur when a long delay occurs between the set of the I2CTXRDY interrupt flag and the loading of I2CDRB (I2CDRW).

Workaround

After detection of the I2CTXRDY interrupt flag, verify that the I2CTXUDF bit in I2CDCTL is set before loading I2CDRB (I2CDRW).

I2C9	USART Module
Function	Master Transmitter Repeat Mode I2CSTP setting error.
Description	<p>When the USART is configured for I2C mode (U0CTL.I2C, SYNC, and I2CEN are set) and the module is configured as an I2C master (U0CTL.MST=1) and repeat mode operation is selected (I2CTCTL.I2CRM=1), the timing of the I2CSTP bit can result in lost data or extra requested transmitted bytes.</p> <p>Specifically, if interrupts are active during the following two cases:</p> <ol style="list-style-type: none"> 1) During the time between the setting of the I2CSTP bit and loading of I2CDRB (I2CDRW). 2) For transmitting slave address only, during the time between checking for I2CSTT cleared and setting I2CSTP. <p>Note: In the second case, the SCL line will be held low until the I2CDRB (I2CDRW) is loaded and then shifted out.</p>
Workaround	<p>Solution for case #1: disable all interrupts (DINT) before setting I2CSTP then re-enabling after loading of I2CDRB.</p> <p>Solution for case #2: disable all interrupts (DINT) before setting I2CSTT bit then re-enabling after setting I2CSTP bit.</p>
I2C10	USART Module
Function	Master stop bit SCL low phase does not match I2CSCLL setting.
Description	When the USART is configured for I2C mode (U0CTL.I2C, SYNC, and I2CEN are set) and the module is configured as an I2C master (U0CTL.MST=1), the hardware control of the SCL low phase before stop generation is equal to a single I2CCLK period. This is particularly noticeable with large I2CSCLL settings or large I2CPSC settings.
Workaround	None.
I2C11	USART Module
Function	Master state machine requires reset before new sequence can proceed.
Description	When the USART is configured for I2C mode (U0CTL.I2C, SYNC, and I2CEN are set) and the module is configured as an I2C master (U0CTL.MST=1), the master state-machine does not properly reset between execution cycles.
Workaround	<p>Before starting the new master sequence, clear and then re-set the I2CEN bit in the U0CTL register.</p> <pre>bic.b #I2CEN,&U0CTL bis.b #I2CEN,&U0CTL</pre>
I2C12	USART Module
Function	Master/Slave loses data on reception (lost RXRDYIFG).
Description	If the I2C data register I2CDRB (I2CDRW) is read at the same time that data is loaded

from the internal I2C shift register into I2CDRB (I2CDRW), then the received data is lost and no corresponding receive ready interrupt (RXRDYIFG) is generated. Following RXRDYIFG interrupts are processed but the missing byte cannot be recovered.

Workaround

Do not read the I2CDRB(I2CDRW) register while data is being loaded into it. This can be ensured by reading this register in a timely manner using any one of the following methods:

- 1) Handle RXRDYIFG events with all other interrupt sources disabled.
- 2) Use the DMA for receiving incoming I2C data. The DMA interrupt or ARDYIFG interrupt can be used to initiate further processing of received data.
- 3) Enable nested interrupts to allow immediate processing of RXRDYIFG interrupts. (Care must be taken to avoid stack overflows).

I2C13
USART Module
Function

Glitch on SCL between I2C communication cycles can corrupt the state machine in I2C master mode.

Description

When the USART is configured for I2C communication (U0CTL.I2C, SYNC, and I2CEN are set) and the module is configured as an I2C master (U0CTL.MST=1), the I2C module is automatically switched to slave mode following the I2C master's generation of a stop condition. If SCL is then pulled low and released again, the following device behavior can be observed:

- 1) When SCL is pulled low after the stop condition is generated and while ARDYIFG is not yet set, then ARDYIFG is not set as expected and ALIFG is set. SCL is released. See workaround 1 for details on how to handle this condition.
- 2) When SCL is pulled low at the same time as ARDYIFG is being set, ALIFG is set and SCL is released. Subsequent communication can result in an immediate ALIFG generation. See workaround 2 for details on how to handle this condition.
- 3) When SCL is pulled low after ARDYIFG is set but before ARDYIFG is cleared, ALIFG is not set, but SCL is held low by the master. An SCL hang-up condition occurs. See workaround 3 for details on how to handle this condition.
- 4) When SCL is pulled low after ARDYIFG is cleared, the module operates as intended. The ALIFG flag is not set and SCL is released.

Workaround

1. ALIFG must be processed. Data bytes are not affected.
2. ALIFG must be processed. Data bytes are not affected. To avoid a second ALIFG, clear I2CEN and re-set I2CEN before new communication begins.
3. Clear I2CEN and re-set I2CEN before new communication begins to clear the SCL hang-up.

I2C14
USART Module
Function

Master SCL phases do not match I2CSCLx settings.

Description

When the USART is configured for I2C mode (U0CTL.I2C, SYNC, and I2CEN are set) and the module is used as an I2C master (U0CTL.MST=1), the generated I2C shift clock (SCL) high and low phases may be one or more I2CIN clock periods longer than defined by I2CSCLH and I2CSCLL. High I2CIN frequencies, large external pull-up resistors, and a large capacitive bus loading on SCL increase the likelihood for this to occur.

Workaround If possible, use an I2CIN input frequency of 1MHz or less. Additionally, use low-impedance I2C pull-up resistors, preferably in the lower single-digit k-Ohm range, and minimize capacitive load on SCL.

I2C15 *USART Module*

Function I2CBUSY flag may clear before stop condition

Description The I2CBUSY flag may already be cleared before the Stop condition on the bus is seen.

Workaround Use the I2CBB flag instead of the I2CBUSY flag.

I2C16 *USART Module*

Function I2C Slave may not detect own address correctly

Description When an interrupt occurs between ACK and stop conditions of a slave transmission, the slave may not acknowledge the slave address byte if all below conditions are fulfilled:

- STT interrupt is enabled
- Device is in LPMx during start condition.

If the failure occurs, the I2C state machine switches into IDLE state.

Workaround (1)Do not use the STT interrupt for slave transmission.
Or
(2)Disable all interrupts between ACK and stop condition on I2C

MPY2 *MPY Module*

Function Multiplier Result register corruption

Description Depending on the address of the write instruction, writing to the multiplier result registers (RESHI, RESLO, or SUMEXT) may corrupt the result registers. The address dependency varies between a 2-word and a 3-word instructions.

Workaround Ensure that a write instruction to an MPY result register (for example, mov.w #200, &RESHI) is not located at an address with the four least significant bits shown in Table 1:

Table 1. Sensitive Addresses for Write Access to MPY Result Registers MAB[3:0]

RESLOW 013Ah		RESHI 013Ch		SUMEXT 013Eh	
3 Word	2 Word	3 Word	2 Word	3 Word	2 Word
2	4	2	4	2	4
6	8	4	6	6	8
A	C	A	C	A	C
E	0	C	E	–	–

SVS2 *SVS Module*

Function	DAC1 overwrites an input of the SVS comparator
Description	DAC1 overrides the input of the SVS comparator. This is caused by a conflict between SVS and DAC1 at Port 6.7. DAC1 is enabled when DAC12AMPx is > 0.
Workaround	Do not enable DAC1 when SVS is used.

TA12 *TIMER_A Module*

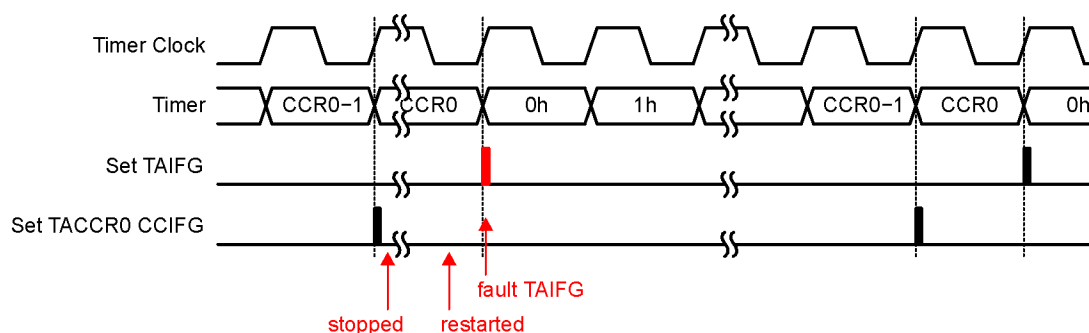
Function	Interrupt is lost (slow ACLK)
Description	Timer_A counter is running with slow clock (external TACLK or ACLK) compared to MCLK. The compare mode is selected for the capture/compare channel and the CCRx register is incremented by one with the occurring compare interrupt (if TAR = CCRx). Due to the fast MCLK the CCRx register increment (CCRx = CCRx+1) happens before the Timer_A counter has incremented again. Therefore the next compare interrupt should happen at once with the next Timer_A counter increment (if TAR = CCRx + 1). This interrupt gets lost.
Workaround	Switch capture/compare mode to capture mode before the CCRx register increment. Switch back to compare mode afterwards.

TA16 *TIMER_A Module*

Function	First increment of TAR erroneous when IDx > 00
Description	The first increment of TAR after any timer clear event (POR/TACLR) happens immediately following the first positive edge of the selected clock source (INCLK, SMCLK, ACLK or TACLK). This is independent of the clock input divider settings (ID0, ID1). All following TAR increments are performed correctly with the selected IDx settings.
Workaround	None

TA21 *TIMER_A Module*

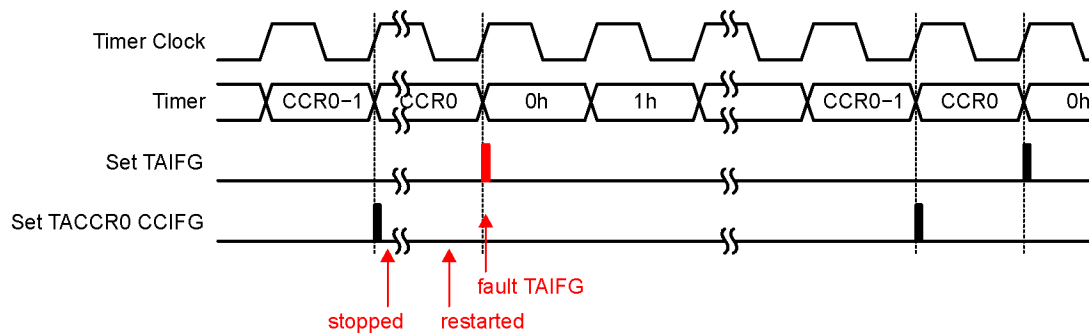
Function	TAIFG Flag is erroneously set after Timer A restarts in Up Mode
Description	In Up Mode, the TAIFG flag should only be set when the timer resets from TACCR0 to zero. However, if the Timer A is stopped at TAR = TACCR0, then cleared (TAR=0) by setting the TACLR bit, and finally restarted in Up Mode, the next rising edge of the TACLK will erroneously set the TAIFG flag.



Workaround	None.
-------------------	-------

TAB22	<i>TIMER_A/TIMER_B Module</i>
Function	Timer_A/Timer_B register modification after Watchdog Timer PUC
Description	Unwanted modification of the Timer_A/Timer_B registers TACTL/TBCTL and TAIV/TBIV can occur when a PUC is generated by the Watchdog Timer(WDT) in Watchdog mode and any Timer_A/Timer_B counter register TACCRx/TBCCRx is incremented/decremented (Timer_A/Timer_B does not need to be running).
Workaround	<p>Initialize TACTL/TBCTL register after the reset occurs using a MOV instruction (BIS/BIC may not fully initialize the register). TAIV/TBIV is automatically cleared following this initialization.</p> <p>Example code:</p> <pre>MOV.W #VAL, &TACTL</pre> <p>or</p> <pre>MOV.W #VAL, &TBCTL</pre> <p>Where, VAL=0, if Timer is not used in application otherwise, user defined per desired function.</p>
TB2	<i>TIMER_B Module</i>
Function	Interrupt is lost (slow ACLK)
Description	<p>Timer_B counter is running with slow clock (external TBCLK or ACLK) compared to MCLK. The compare mode is selected for the capture/compare channel and the CCRx register is incremented by 1 with the occurring compare interrupt (if TBR = CCRx).</p> <p>Due to the fast MCLK, the CCRx register increment ($CCRx = CCRx + 1$) happens before the Timer_B counter has incremented again. Therefore, the next compare interrupt should happen at once with the next Timer_B counter increment (if $TBR = CCRx + 1$). This interrupt is lost.</p>
Workaround	Switch capture/compare mode to capture mode before the CCRx register increment. Switch back to compare mode afterward.
TB16	<i>TIMER_B Module</i>
Function	First increment of TBR erroneous when IDx > 00
Description	The first increment of TBR after any timer clear event (POR/TBCLR) happens immediately following the first positive edge of the selected clock source (INCLK, SMCLK, ACLK, or TBCLK). This is independent of the clock input divider settings (ID0, ID1). All following TBR increments are performed correctly with the selected IDx settings.
Workaround	None
TB24	<i>TIMER_B Module</i>
Function	TBIFG Flag is erroneously set after Timer B restarts in Up Mode
Description	In Up Mode, the TBIFG flag should only be set when the timer resets from TBCCR0 to zero. However, if the Timer A is stopped at $TBR = TBCCR0$, then cleared ($TBR=0$) by

setting the TBCLR bit, and finally restarted in Up Mode, the next rising edge of the TBCLK will erroneously set the TBIFG flag.



Workaround None.

US14 *USART Module*

Function Start edge of received characters may be ignored

Description When using the USART in UART mode with UxBR0 = 0x03 and UxBR1 = 0x00, the start edge of received characters may be ignored due to internal timing conflicts within the UART state machine. This condition does not apply when UxBR0 is > 0x03.

Workaround None

US15 *USART Module*

Function UART receive with two stop bits

Description USART hardware does not detect a missing second stop bit when SPB = 1. The Framing Error Flag (FE) will not be set under this condition and erroneous data reception may occur.

Workaround None (Configure USART for a single stop bit, SPB = 0)

WDG2 *WDT Module*

Function Incorrectly accessing a flash control register

Description If a key violation is caused by incorrectly accessing a flash control register, the watchdog interrupt flag is set in addition to the expected PUC.

Workaround None

XOSC4 *XOSC Module*

Function XT1 high frequency oscillator low power wake-up error

Description The XT1 high frequency oscillator wake-up from low power mode operation is not functional.

Workaround

If using the XT1 high frequency oscillator circuitry (BCSCTL1.XTS = 1), the OSCOFF bit in the Status Register (SR) must always be 0.

4 Document Revision History

Changes from family erratasheet to device specific erratasheet.

1. Errata MPY2 was added
2. Errata I2C16 was added
3. Description for TAB22 was updated

Changes from device specific erratasheet to document Revision A.

1. Errata TA21 was added to the errata documentation.

Changes from document Revision A to Revision B.

1. Errata TB24 was added to the errata documentation.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com