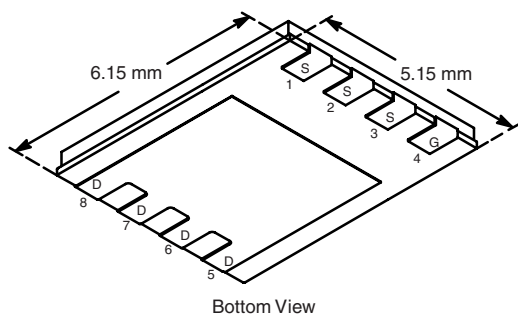


N-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^a	Q_g (Typ.)
20	0.0019 at $V_{GS} = 10$ V	60 ^g	35.3 nC
	0.00255 at $V_{GS} = 4.5$ V	60 ^g	

PowerPAK SO-8



Bottom View

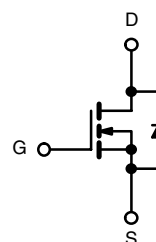
Ordering Information: SiR866DP-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

- Halogen-free
- TrenchFET[®] Gen III Power MOSFET
- Low $R_{DS(on)}$
- PWM (Q_{gd} and R_g) Optimized
- 100 % R_g Tested
- 100 % UIS Tested

APPLICATIONS

- Fixed Telecom
- Low-Side dc-to-dc
- OR-ing



N-Channel MOSFET



RoHS
COMPLIANT

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted				
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ($T_J = 150$ °C)	$T_C = 25$ °C	I_D	60 ^g	A
	$T_C = 70$ °C		60 ^g	
	$T_A = 25$ °C		39 ^{b, c}	
	$T_A = 70$ °C		31 ^{b, c}	
Pulsed Drain Current		I_{DM}	80	A
Continuous Source-Drain Diode Current	$T_C = 25$ °C	I_S	60 ^g	
	$T_A = 25$ °C		4.9 ^{b, c}	
Single Pulse Avalanche Current		I_{AS}	40	mJ
Avalanche Energy		E_{AS}	80	
Maximum Power Dissipation	$T_C = 25$ °C	P_D	83	W
	$T_C = 70$ °C		53	
	$T_A = 25$ °C		5.4 ^{b, c}	
	$T_A = 70$ °C		3.4 ^{b, c}	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{d, e}			260	

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, f}	$t \leq 10$ s	R_{thJA}	18	23	°C/W
	Steady State	R_{thJC}	1.0	1.5	

Notes:

a. Based on $T_C = 25$ °C.

b. Surface Mounted on 1" x 1" FR4 board.

c. $t = 10$ s.

d. See Solder Profile (<http://www.vishay.com/ppg?73257>). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

f. Maximum under Steady State conditions is 65 °C/W.

g. Package Limited.

SPECIFICATIONS T _J = 25 °C, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	20			V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 5 mA		20		mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			- 6.4		
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.2		2.3	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V			1	μA
		V _{DS} = 20 V, V _{GS} = 0 V, T _J = 55 °C			10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	30			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 20 A		0.0015	0.0019	Ω
		V _{GS} = 4.5 V, I _D = 15 A		0.00205	0.00255	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 20 A		78		S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz		4730		pF
Output Capacitance	C _{oss}			1310		
Reverse Transfer Capacitance	C _{rss}			540		
Total Gate Charge	Q _g	V _{DS} = 10 V, V _{GS} = 10 V, I _D = 15 A		71	107	nC
		V _{DS} = 10 V, V _{GS} = 4.5 V, I _D = 15 A		35.3	53	
Gate-Source Charge	Q _{gs}			11.7		
Gate-Drain Charge	Q _{gd}			9.5		
Gate Resistance	R _g	f = 1 MHz	0.2	0.95	1.9	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 10 V, R _L = 1 Ω I _D ≅ 10 A, V _{GEN} = 4.5 V, R _g = 1 Ω		42	80	ns
Rise Time	t _r			23	45	
Turn-Off Delay Time	t _{d(off)}			66	120	
Fall Time	t _f			49	90	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 10 V, R _L = 1 Ω I _D ≅ 10 A, V _{GEN} = 10 V, R _g = 1 Ω		20	40	
Rise Time	t _r			8	16	
Turn-Off Delay Time	t _{d(off)}			46	90	
Fall Time	t _f			9	15	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			60	A
Pulse Diode Forward Current ^a	I _{SM}				80	
Body Diode Voltage	V _{SD}	I _S = 4 A		0.72	1.1	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = 10 A, dI/dt = 100 A/μs, T _J = 25 °C		40	70	ns
Body Diode Reverse Recovery Charge	Q _{rr}			34	60	nC
Reverse Recovery Fall Time	t _a			19		ns
Reverse Recovery Rise Time	t _b			21		

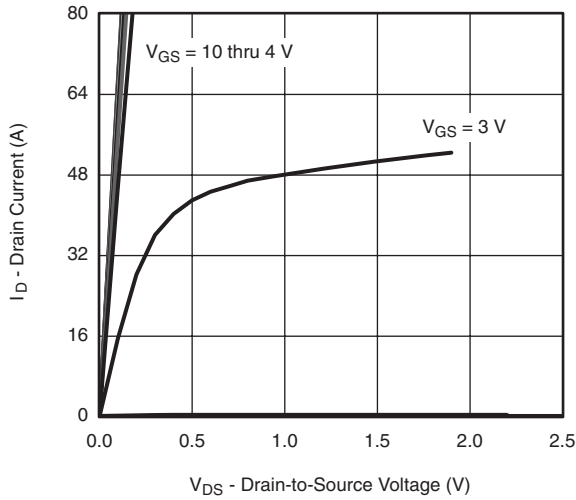
Notes:

a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

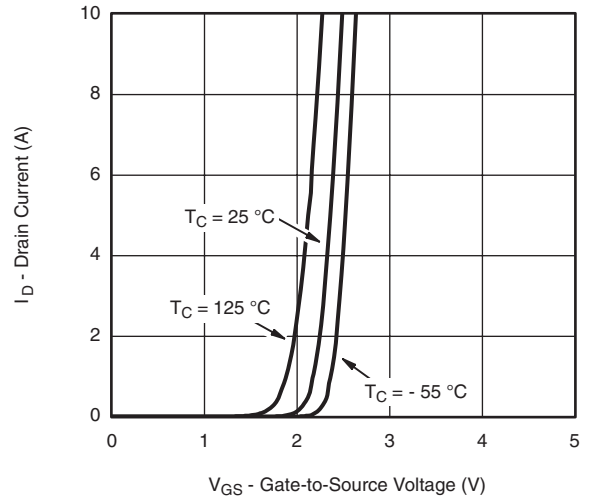
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

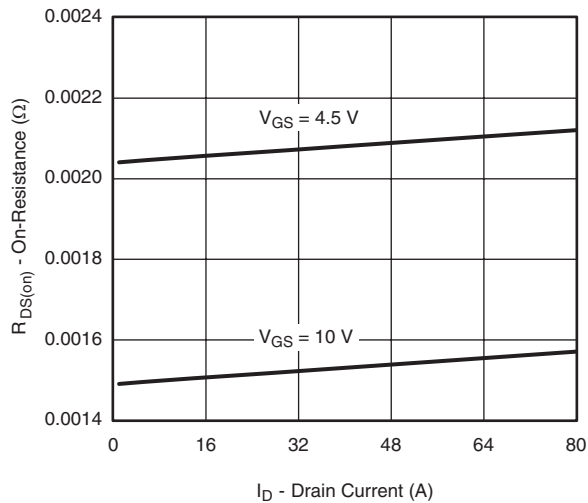
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



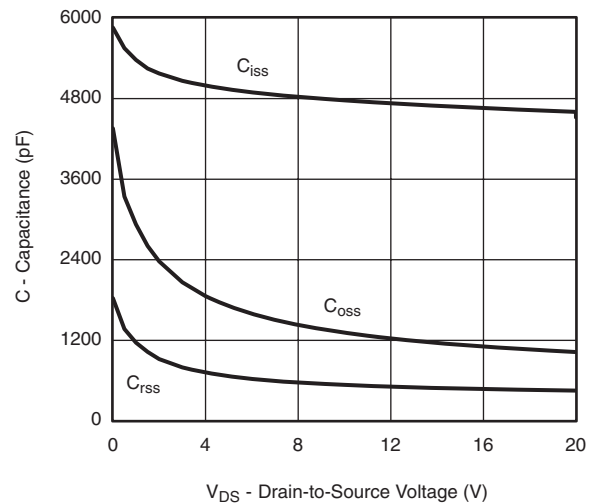
Output Characteristics



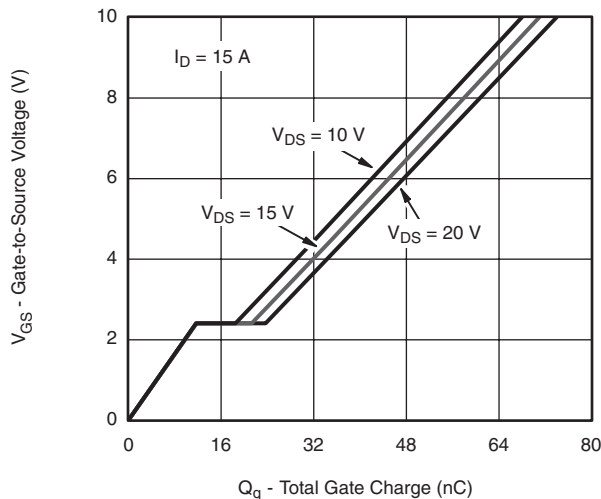
Transfer Characteristics



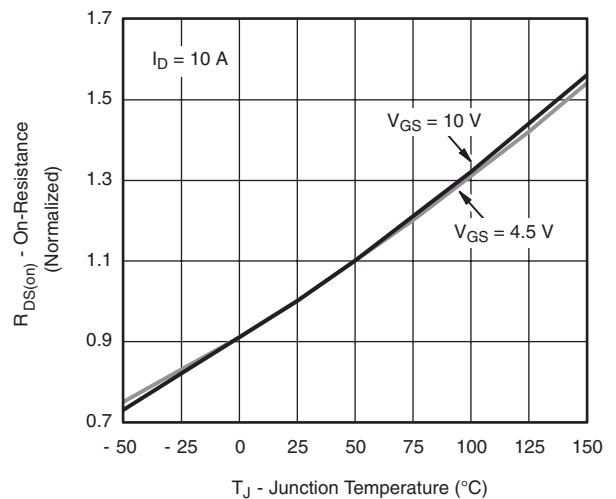
On-Resistance vs. Drain Current and Gate Voltage



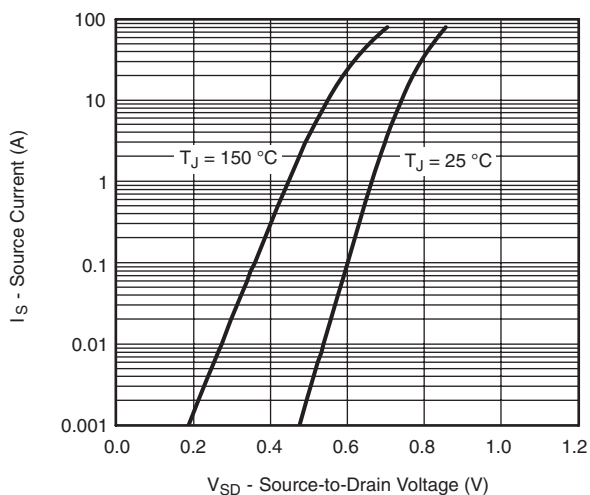
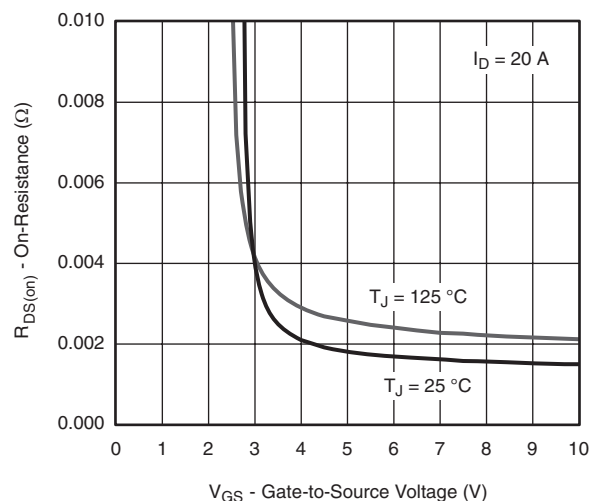
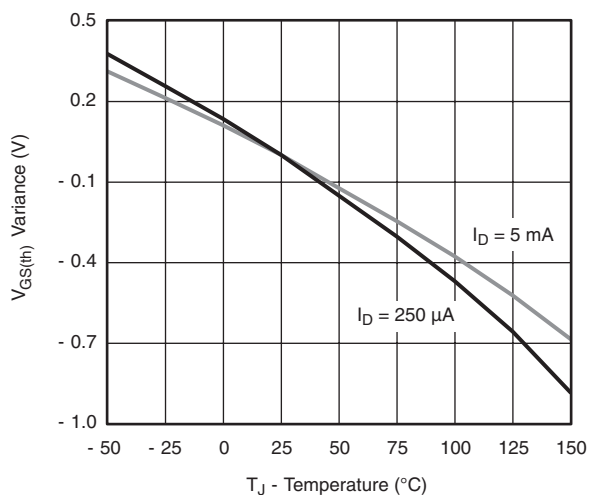
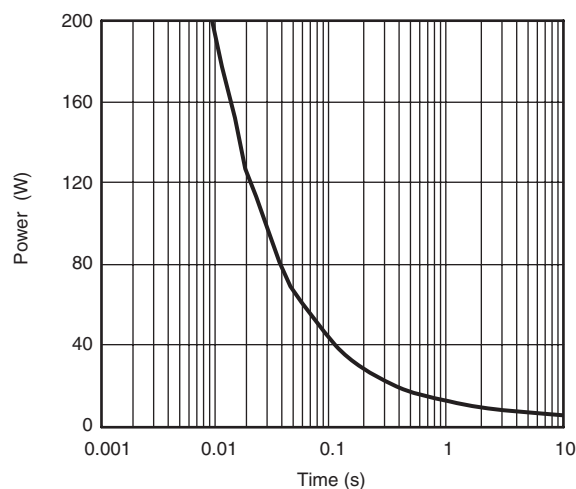
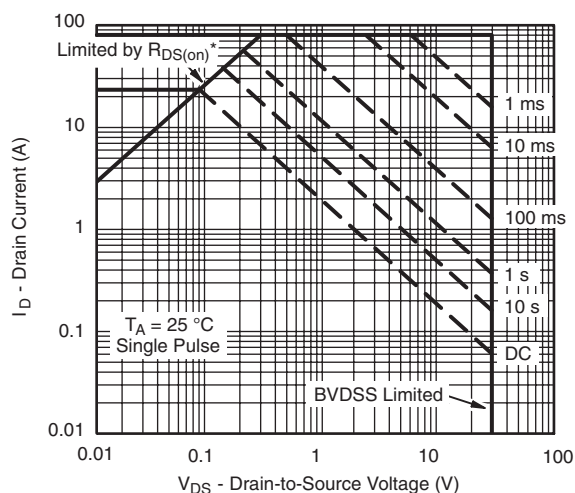
Capacitance



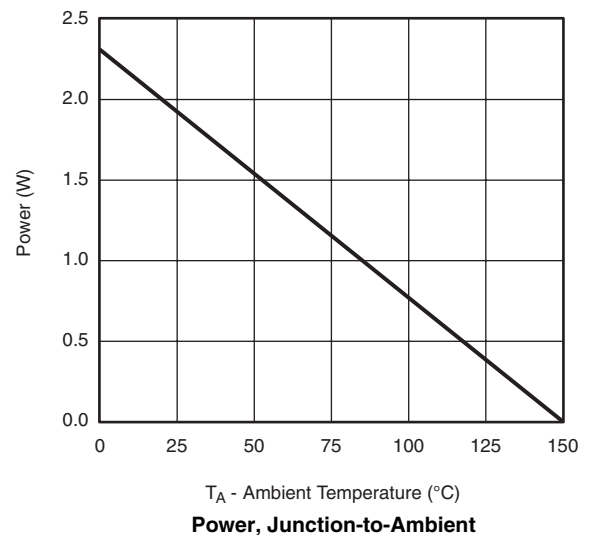
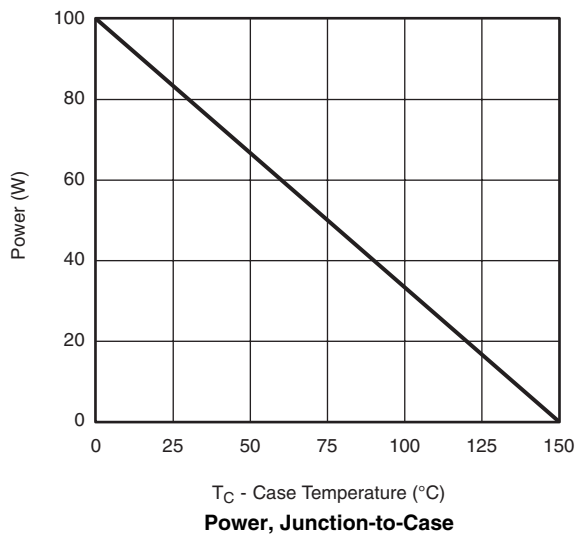
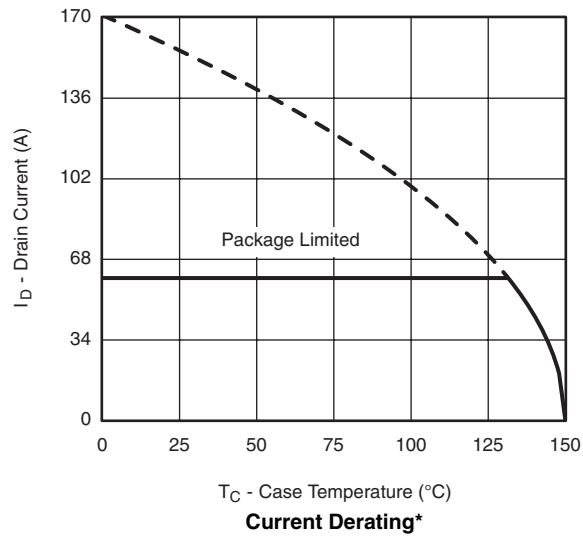
Gate Charge



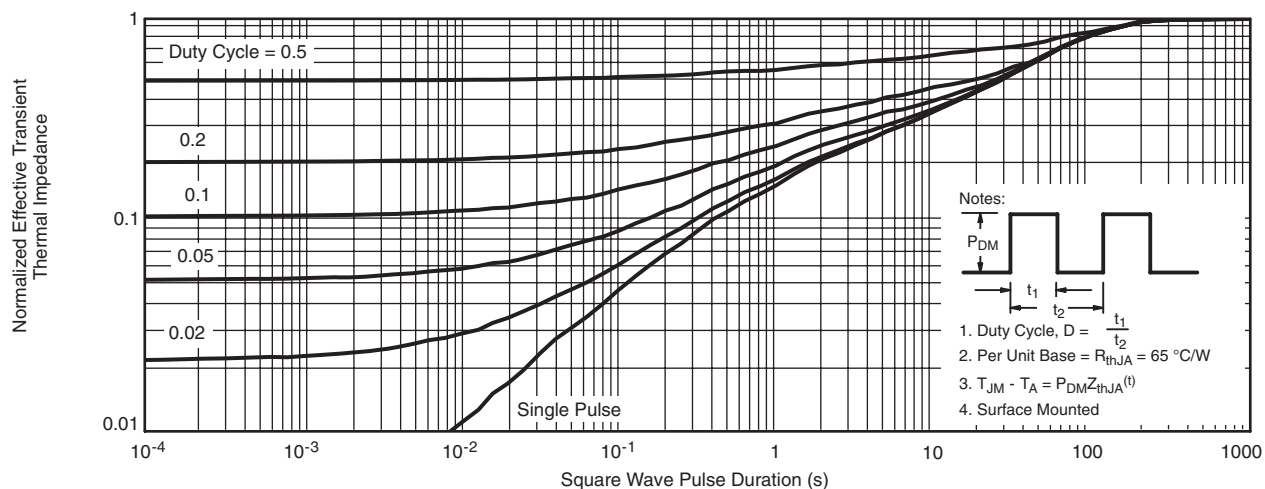
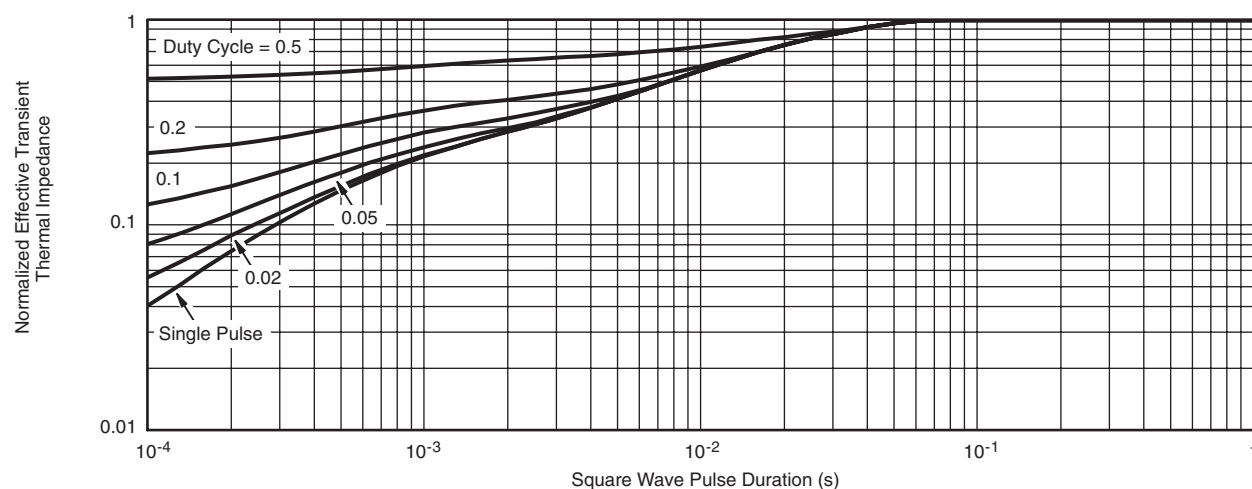
On-Resistance vs. Junction Temperature

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted**Source-Drain Diode Forward Voltage****On-Resistance vs. Gate-to-Source Voltage****Threshold Voltage****Single Pulse Power, Junction-to-Ambient*** $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified**Safe Operating Area, Junction-to-Ambient**

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



* The power dissipation P_D is based on $T_{J(max)} = 175$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted**Normalized Thermal Transient Impedance, Junction-to-Ambient****Normalized Thermal Transient Impedance, Junction-to-Case**

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PowerPAK® SO-8, (Single/Dual)



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.97	1.04	1.12	0.038	0.041	0.044
A1		-	0.05	0	-	0.002
b	0.33	0.41	0.51	0.013	0.016	0.020
c	0.23	0.28	0.33	0.009	0.011	0.013
D	5.05	5.15	5.26	0.199	0.203	0.207
D1	4.80	4.90	5.00	0.189	0.193	0.197
D2	3.56	3.76	3.91	0.140	0.148	0.154
D3	1.32	1.50	1.68	0.052	0.059	0.066
D4	0.57 typ.			0.0225 typ.		
D5	3.98 typ.			0.157 typ.		
E	6.05	6.15	6.25	0.238	0.242	0.246
E1	5.79	5.89	5.99	0.228	0.232	0.236
E2 (for AL product)	3.30	3.48	3.66	0.130	0.137	0.144
E2 (for other product)	3.48	3.66	3.84	0.137	0.144	0.151
E3	3.68	3.78	3.91	0.145	0.149	0.154
E4 (for AL product)	0.58 typ.			0.023 typ.		
E4 (for other product)	0.75 typ.			0.030 typ.		
e	1.27 BSC			0.050 BSC		
K (for AL product)	1.45 typ.			0.057 typ.		
K (for other product)	1.27 typ.			0.050 typ.		
K1	0.56	-	-	0.022	-	-
H	0.51	0.61	0.71	0.020	0.024	0.028
L	0.51	0.61	0.71	0.020	0.024	0.028
L1	0.06	0.13	0.20	0.002	0.005	0.008
θ	0°	-	12°	0°	-	12°
W	0.15	0.25	0.36	0.006	0.010	0.014
M	0.125 typ.			0.005 typ.		
ECN: C13-0702-Rev. K, 20-May-13						
DWG: 5881						

RECOMMENDED MINIMUM PADS FOR PowerPAK® SO-8 Single



Recommended Minimum Pads
Dimensions in Inches/(mm)

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