New Product



SiR494DP

RoHS

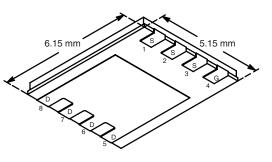
COMPLIANT

HALOGEN

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N-Channel 12-V (D-S) MOSFET

PRODUCT SUMMARY					
V _{DS} (V)	R_{DS(on)} (Ω)	I _D (A) ^a	Q _g (Typ.)		
12	0.0012 at V _{GS} = 10 V	60	50 nC		
12	0.0017 at V_{GS} = 4.5 V	60	50 110		



PowerPAK[®] SO-8

Bottom View

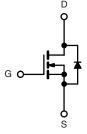
Ordering Information: SiR494DP-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

- Halogen-free According to IEC 61249-2-21
 Definition
- TrenchFET[®] Gen III Power MOSFET
- 100 % R_g Tested
- 100 % UIS Tested
- Compliant to RoHS Directive 2002/95/EC

APPLICATIONS

- DC/DC
- OR-ing



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS	T _A = 25 °C, unles	ss otherwise not	ted	
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V _{DS}	12	v
Gate-Source Voltage		V _{GS}	± 20	v
	T _C = 25 °C		60 ^a	
Continuous Drain Current ($T_1 = 150 \text{ °C}$)	T _C = 70 °C		60 ^a	
Continuous Diain Guneni (1j = 130 °C)	T _A = 25 °C		53.7 ^{b, c}	
	T _A = 70 °C		43 ^{b, c}	A
Pulsed Drain Current		I _{DM}	100	
Continuous Source-Drain Diode Current	T _C = 25 °C	I _S	60 ^a	
Continuous Source-Drain Diode Current	T _A = 25 °C	'S	5.6 ^{b, c}	
Single Pulse Avalanche Current		I _{AS}	15	
Single Pulse Avalanche Energy	L = 0.1 mm	E _{AS}	11	mJ
	T _C = 25 °C		104	
Maximum Power Dissipation	T _C = 70 °C	P _D	66.6	w
	T _A = 25 °C	· D	6.25 ^{b, c}	••
	T _A = 70 °C		4.0 ^{b, c}	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{d, e}			260	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, f}	t ≤ 10 s	R _{thJA}	15	20	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R _{thJC}	0.9	1.2	0/11

Notes:

a. Package limited.

b. Surface Mounted on 1" x 1" FR4 board.

c. t = 10 s.

d. See Solder Profile (<u>www.vishay.com/ppg?73257</u>). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

f. Maximum under Steady State conditions is 54 °C/W.

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Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Static					•	
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 \text{ V}, \text{ I}_{D} = 250 \mu\text{A}$	12			V
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	I _D = 250 μA		9.5		mV/°C
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	η – 200 μη		- 6.1		mv/ v
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \ \mu A$	1.0		2.5	V
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			± 100	nA
Zaus Oata Valtaga Dusia Ouwant		$V_{DS} = 12 \text{ V}, V_{GS} = 0 \text{ V}$			1	μA
Zero Gate Voltage Drain Current	IDSS	V_{DS} = 12 V, V_{GS} = 0 V, T_{J} = 55 °C			10	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	30			Α
	Р	V _{GS} = 10 V, I _D = 20 A		0.001	0.0012	0
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 4.5 \text{ V}, \text{ I}_{D} = 20 \text{ A}$		0.0014	0.0017	Ω
Forward Transconductance ^a	9 _{fs}	V _{DS} = 10 V, I _D = 20 A		95		S
Dynamic ^b					1	
Input Capacitance	C _{iss}			6900		
Output Capacitance	C _{oss}	$V_{DS} = 6 V, V_{GS} = 0 V, f = 1 MHz$		4130		pF
Reverse Transfer Capacitance	C _{rss}			1785		
Takal Oaka Okaana	Qg	$V_{DS} = 6 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 20 \text{ A}$		98	150	
Total Gate Charge				50	75	
Gate-Source Charge	Q _{gs}	$V_{\rm DS}$ = 6 V, $V_{\rm GS}$ = 4.5 V, $I_{\rm D}$ = 20 A		16.5		nC
Gate-Drain Charge	Q _{gd}			15		
Gate Resistance	R _g	f = 1 MHz	0.2	1.05	2	Ω
Turn-On Delay Time	t _{d(on)}			19	35	
Rise Time	t _r	V_{DD} = 10 V, R_L = 1.0 Ω		10	20	
Turn-Off Delay Time	t _{d(off)}	$\rm I_D \cong 10$ A, $\rm V_{GEN}$ = 10 V, $\rm R_g$ = 1 Ω		48	90	
Fall Time	t _f			11	22	1
Turn-On Delay Time	t _{d(on)}			42	80	ns
Rise Time	t _r	V_{DD} = 10 V, R_L = 1.0 Ω		60	110	
Turn-Off Delay Time	t _{d(off)}	$I_D \cong$ 10 A, V_{GEN} = 4.5 V, R_g = 1 Ω		54	100	
Fall Time	t _f			54	100	1
Drain-Source Body Diode Characteristic	cs				•	
Continuous Source-Drain Diode Current	۱ _S	T _C = 25 °C			60	٨
Pulse Diode Forward Current ^a	I _{SM}				100	A
Body Diode Voltage	V _{SD}	I _S = 5 A		0.73	1.1	V
Body Diode Reverse Recovery Time	t _{rr}			46	80	ns
Body Diode Reverse Recovery Charge	Q _{rr}	L = 10.0 d/dt = 100.04 trans = 25.90		44	80	nC
Reverse Recovery Fall Time	t _a	$I_F = 10 \text{ A}, \text{ dl/dt} = 100 \text{ A/}\mu\text{s}, \text{ T}_J = 25 ^\circ\text{C}$		22		
Reverse Recovery Rise Time	t _b			24		ns

Notes:

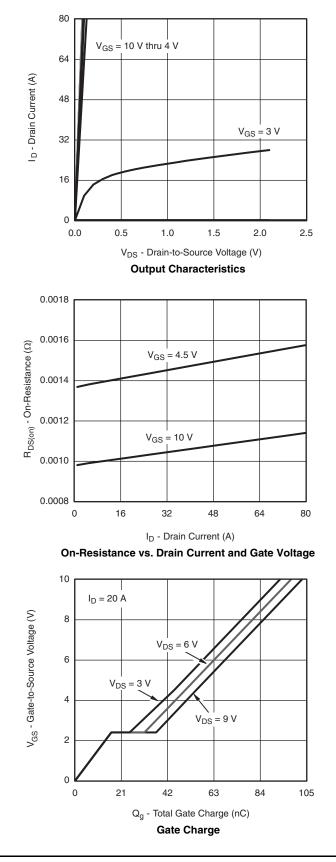
a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %. b. Guaranteed by design, not subject to production testing.

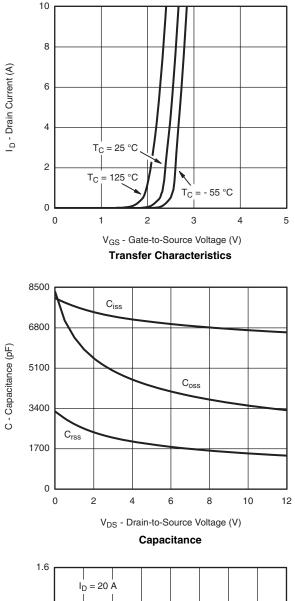
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

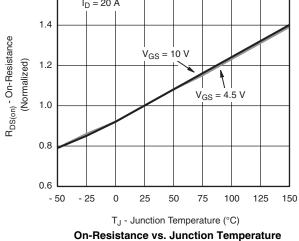


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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted





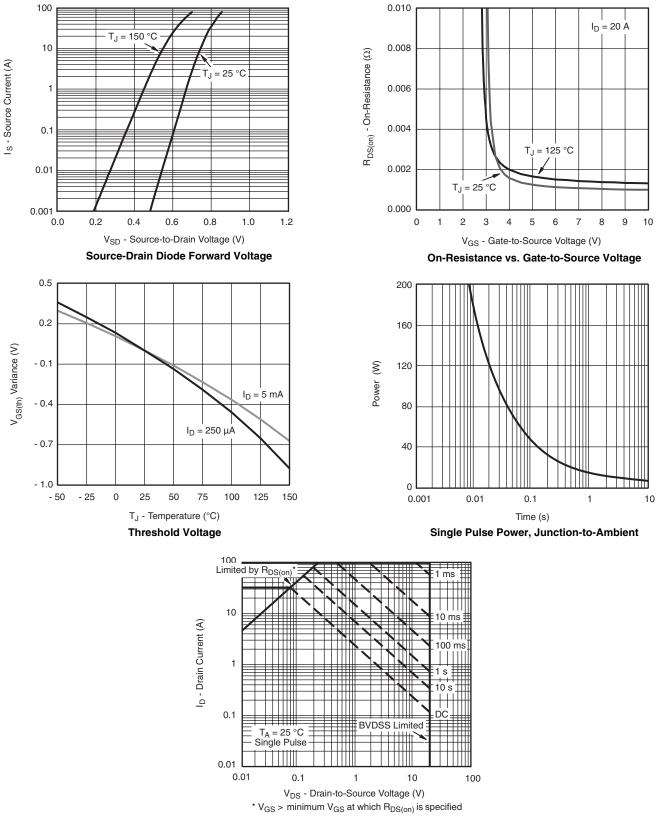


Document Number: 64824 S09-0874-Rev. A, 18-May-09

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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

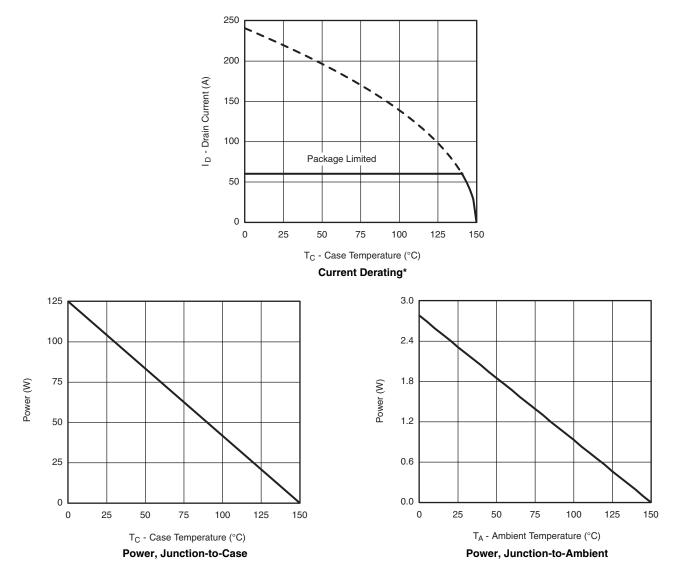


Safe Operating Area, Junction-to-Ambient



SiR494DP Vishay Siliconix

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

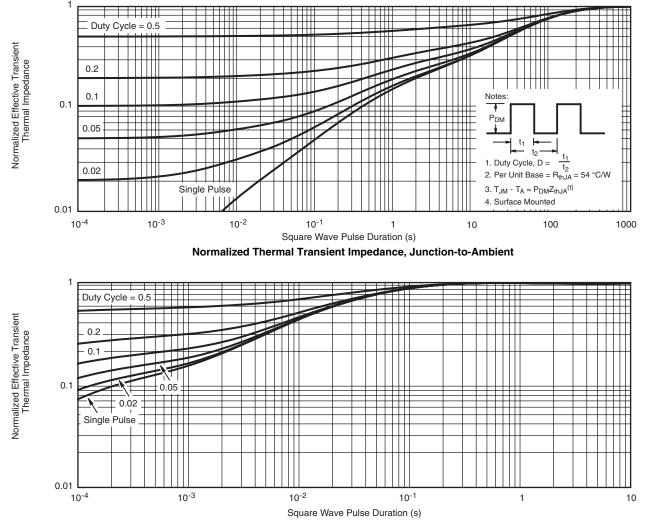


* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg264824.



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PowerPAK[®] SO-8, (Single/Dual)









Backside View of Dual Pad

Notes

1. Inch will govern.

2 Dimensions exclusive of mold gate burrs.

3. Dimensions exclusive of mold flash and cutting burrs.

DIM.	MILLIMETERS			INCHES			
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A	0.97	1.04	1.12	0.038	0.041	0.044	
A1		-	0.05	0	-	0.002	
b	0.33	0.41	0.51	0.013	0.016	0.020	
С	0.23	0.28	0.33	0.009	0.011	0.013	
D	5.05	5.15	5.26	0.199	0.203	0.207	
D1	4.80	4.90	5.00	0.189	0.193	0.197	
D2	3.56	3.76	3.91	0.140	0.148	0.154	
D3	1.32	1.50	1.68	0.052	0.059	0.066	
D4	0.57 typ.				0.0225 typ.		
D5	3.98 typ.				0.157 typ.		
E	6.05	6.15	6.25	0.238	0.242	0.246	
E1	5.79	5.89	5.99	0.228	0.232	0.236	
E2 (for AL product)	3.30	3.48	3.66	0.130	0.137	0.144	
E2 (for other product)	3.48	3.66	3.84	0.137	0.144	0.151	
E3	3.68	3.78	3.91	0.145	0.149	0.154	
E4 (for AL product)		0.58 typ.		0.023 typ.			
E4 (for other product)		0.75 typ.		0.030 typ.			
е	1.27 BSC			0.050 BSC			
K (for AL product)	1.45 typ.			0.057 typ.			
K (for other product)	1.27 typ.			0.050 typ.			
K1	0.56	-	-	0.022	-	-	
Н	0.51	0.61	0.71	0.020	0.024	0.028	
L	0.51	0.61	0.71	0.020	0.024	0.028	
L1	0.06	0.13	0.20	0.002	0.005	0.008	
θ	0°	-	12°	0°	-	12°	
W	0.15	0.25	0.36	0.006	0.010	0.014	
М	0.125 typ.			0.005 typ.			

Revison: 20-May-13

Document Number: 71655



Application Note 826

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RECOMMENDED MINIMUM PADS FOR PowerPAK® SO-8 Single



Recommended Minimum Pads Dimensions in Inches/(mm)

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