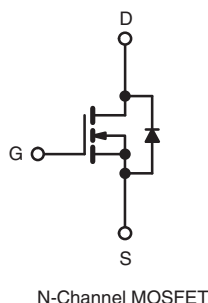
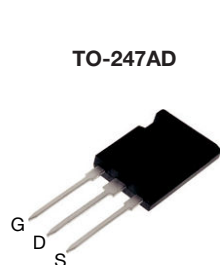


## E Series Power MOSFET

### PRODUCT SUMMARY

$V_{DS}$ (V) at $T_J$ max.	650	
$R_{DS(on)}$ max. at 25 °C ( $\Omega$ )	$V_{GS} = 10$ V	0.099
$Q_g$ (Max.) (nC)	150	
$Q_{gs}$ (nC)	24	
$Q_{gd}$ (nC)	42	
Configuration	Single	



### FEATURES

- Low Figure-of-Merit (FOM):  $R_{on} \times Q_g$
- Low Input Capacitance ( $C_{iss}$ )
- Reduced Switching and Conduction Losses
- Ultra Low Gate Charge ( $Q_g$ )
- Avalanche Energy Rated (UIS)
- Material categorization: For definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

### APPLICATIONS

- Server and Telecom Power Supplies
- Switch Mode Power Supplies (SMPS)
- Power Factor Correction Power Supplies (PFC)
- Lighting
  - High-Intensity Discharge (HID)
  - Fluorescent Ballast Lighting
- Industrial
  - Welding
  - Induction Heating
  - Motor Drives
  - Battery Chargers
  - Renewable Energy
  - Solar (PV Inverters)

### ORDERING INFORMATION

Package	TO-247AD
Lead (Pb)-free and Halogen-free	SiHW33N60E-GE3

### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$	600	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Gate-Source Voltage AC ( $f > 1$ Hz)		30	
Continuous Drain Current ( $T_J = 150$ °C)	$V_{GS}$ at 10 V	$T_C = 25$ °C	A
		$T_C = 100$ °C	
Pulsed Drain Current <sup>a</sup>	$I_{DM}$	88	
Linear Derating Factor		2.2	W/°C
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$	793	mJ
Maximum Power Dissipation	$P_D$	278	W
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to + 150	°C
Drain-Source Voltage Slope	$dV/dt$	$T_J = 125$ °C	V/ns
Reverse Diode $dV/dt$ <sup>d</sup>			
Soldering Recommendations (Peak Temperature) <sup>c</sup>		for 10 s	°C


#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DD} = 50$  V, starting  $T_J = 25$  °C,  $L = 28.2$  mH,  $R_g = 25$   $\Omega$ ,  $I_{AS} = 7.5$  A.
- 1.6 mm from case.
- $I_{SD} \leq I_D$ ,  $dI/dt = 100$  A/ $\mu$ s, starting  $T_J = 25$  °C.

**THERMAL RESISTANCE RATINGS**

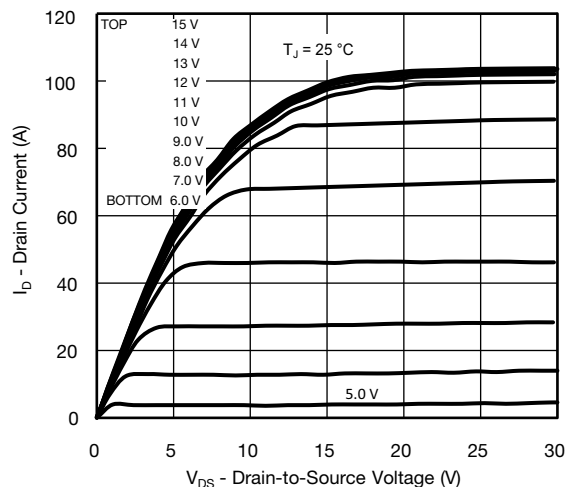
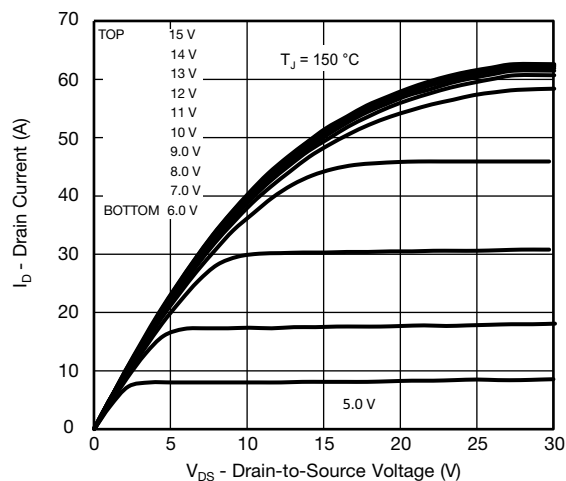
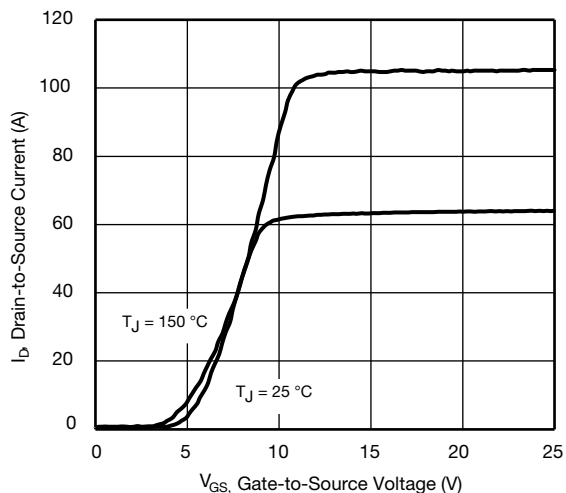
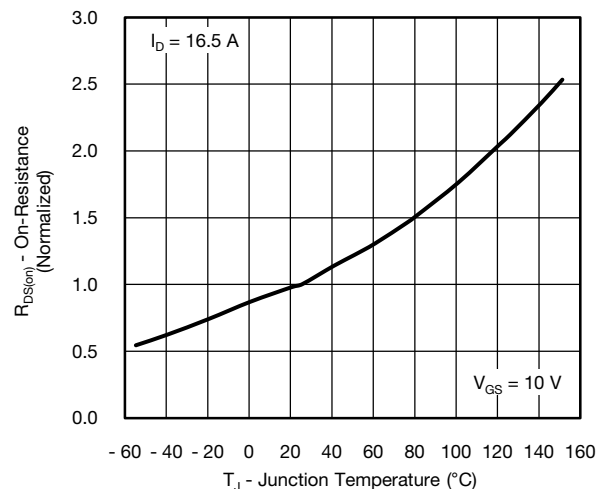
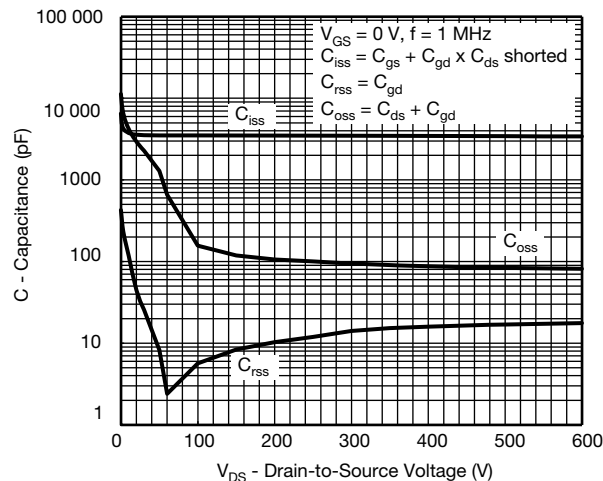
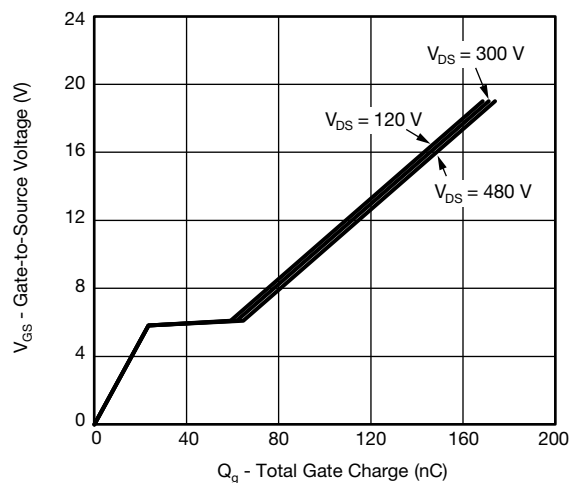
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	40	°C/W
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	0.45	

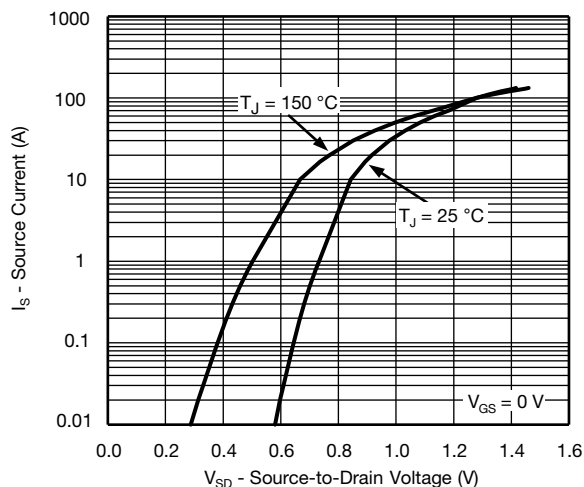
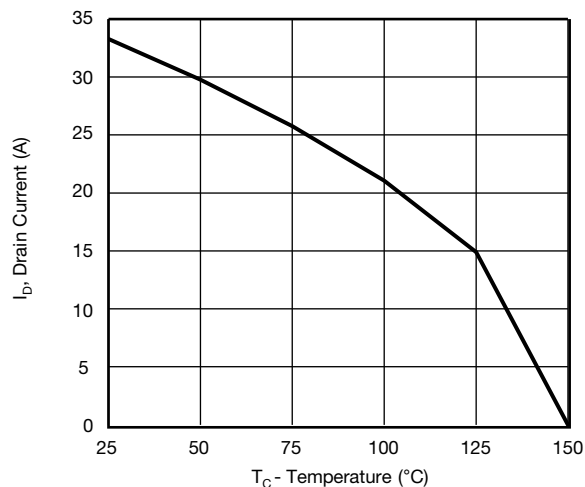
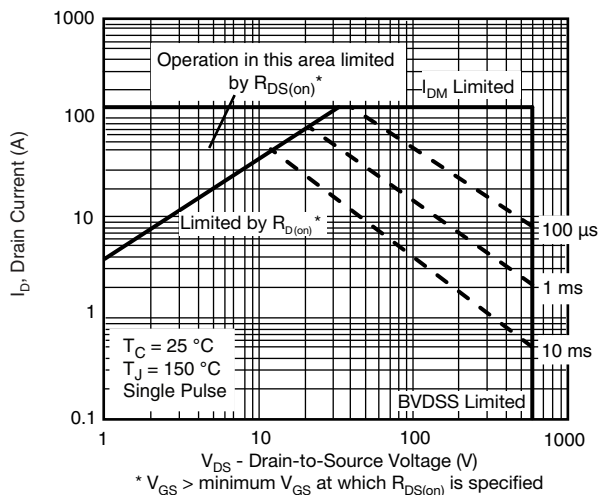
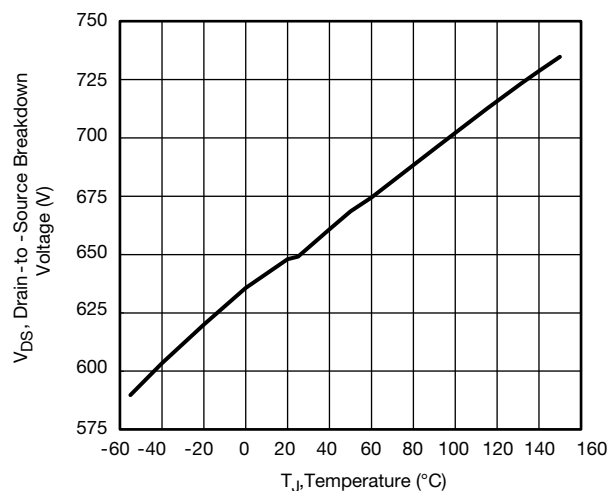
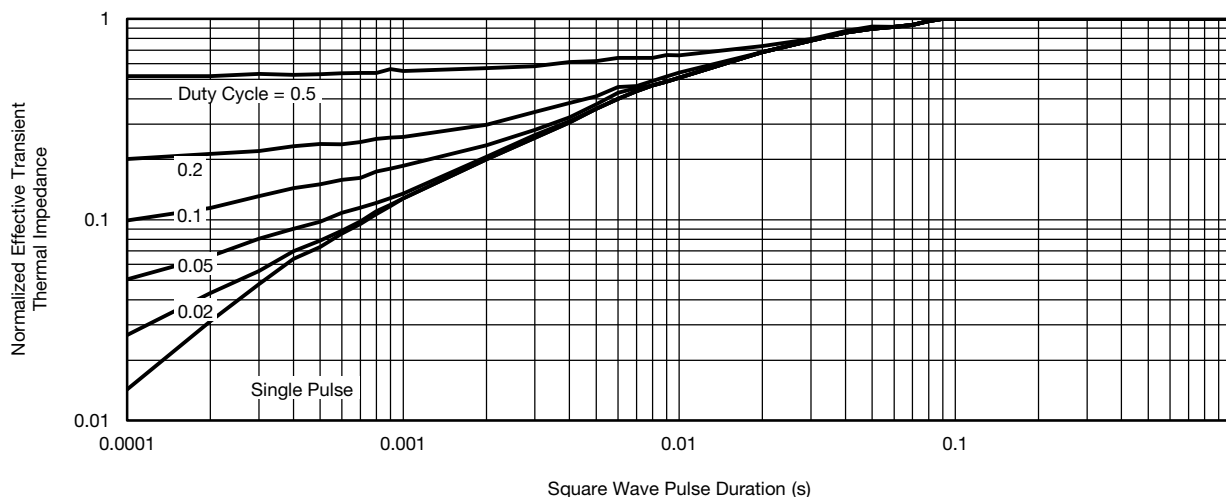
**SPECIFICATIONS** ( $T_J = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

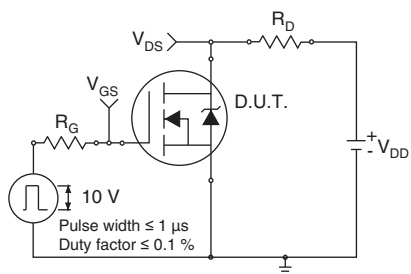
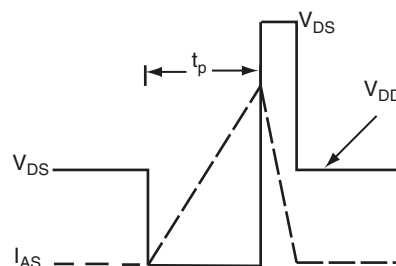
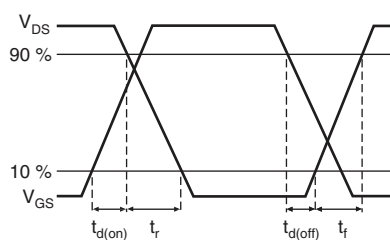
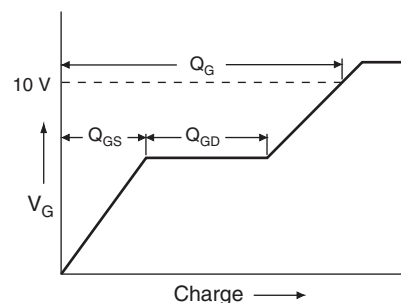
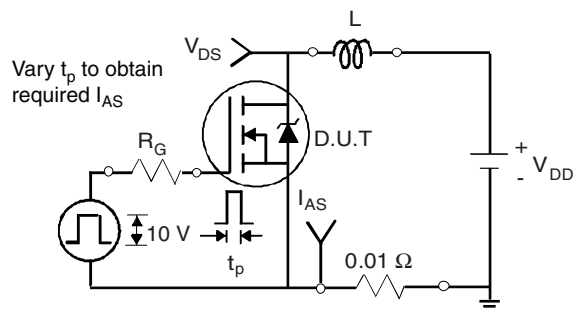
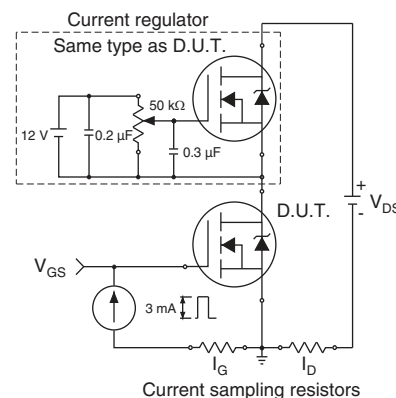
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}$ , $I_D = 250\text{ }\mu\text{A}$		600	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^{\circ}\text{C}$ , $I_D = 1\text{ mA}$		-	0.71	-	V/ $^{\circ}\text{C}$
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$		2.0	-	4.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$		-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 600\text{ V}$ , $V_{GS} = 0\text{ V}$		-	-	1	$\mu\text{A}$
		$V_{DS} = 480\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_J = 125\text{ }^{\circ}\text{C}$		-	-	10	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 16.5\text{ A}$	-	0.083	0.099	$\Omega$
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 30\text{ V}$ , $I_D = 16.5\text{ A}$		-	11	-	S
Dynamic							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}$ , $V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$		-	3508	-	pF
Output Capacitance	$C_{oss}$			-	156	-	
Reverse Transfer Capacitance	$C_{rss}$			-	6	-	
Effective output capacitance, energy related <sup>b</sup>	$C_{o(er)}$	$V_{GS} = 0\text{ V}$ , $V_{DS} = 0\text{ V to } 480\text{ V}$		-	136	-	
Effective output capacitance, time related <sup>c</sup>	$C_{o(tr)}$			-	468	-	
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}$	$I_D = 16.5\text{ A}$ , $V_{DS} = 480\text{ V}$	-	100	150	nC
Gate-Source Charge	$Q_{gs}$			-	24	-	
Gate-Drain Charge	$Q_{gd}$			-	42	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 480\text{ V}$ , $I_D = 16.5\text{ A}$ $R_g = 9.1\text{ }\Omega$ , $V_{GS} = 10\text{ V}$		-	28	56	ns
Rise Time	$t_r$			-	60	90	
Turn-Off Delay Time	$t_{d(off)}$			-	99	150	
Fall Time	$t_f$			-	54	80	
Gate Input Resistance	$R_g$	$f = 1\text{ MHz}$ , open drain		-	0.7	-	$\Omega$
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	33	A
Pulsed Diode Forward Current	$I_{SM}$			-	-	88	
Diode ForwardVoltage	$V_{SD}$	$T_J = 25\text{ }^{\circ}\text{C}$ , $I_S = 16.5\text{ A}$ , $V_{GS} = 0\text{ V}$		-	0.9	1.2	V
Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^{\circ}\text{C}$ , $I_F = I_S$ , $dI/dt = 100\text{ A}/\mu\text{s}$ , $V_R = 20\text{ V}$		-	503	1006	ns
Reverse Recovery Charge	$Q_{rr}$			-	8.5	17	$\mu\text{C}$
Reverse Recovery Current	$I_{RRM}$			-	26	-	A

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature.  
b.  $C_{oss(er)}$  is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$ .  
c.  $C_{oss(tr)}$  is a fixed capacitance that gives the charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$ .

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Fig. 1 - Typical Output Characteristics,  $T_C = 150^\circ\text{C}$** 

**Fig. 2 - Typical Output Characteristics,  $T_C = 150^\circ\text{C}$** 

**Fig. 3 - Typical Transfer Characteristics**

**Fig. 4 - Normalized On-Resistance vs. Temperature**

**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**

**Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage**


**Fig. 7 - Typical Source-Drain Diode Forward Voltage**

**Fig. 9 - Maximum Drain Current vs. Case Temperature**

**Fig. 8 - Maximum Safe Operating Area**

**Fig. 10 - Typical Drain-to-Source Voltage vs. Temperature**

**Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case**


**Fig. 12 - Switching Time Test Circuit**

**Fig. 15 - Unclamped Inductive Waveforms**

**Fig. 13 - Switching Time Waveforms**

**Fig. 16 - Basic Gate Charge Waveform**

**Fig. 14 - Unclamped Inductive Test Circuit**

**Fig. 17 - Gate Charge Test Circuit**

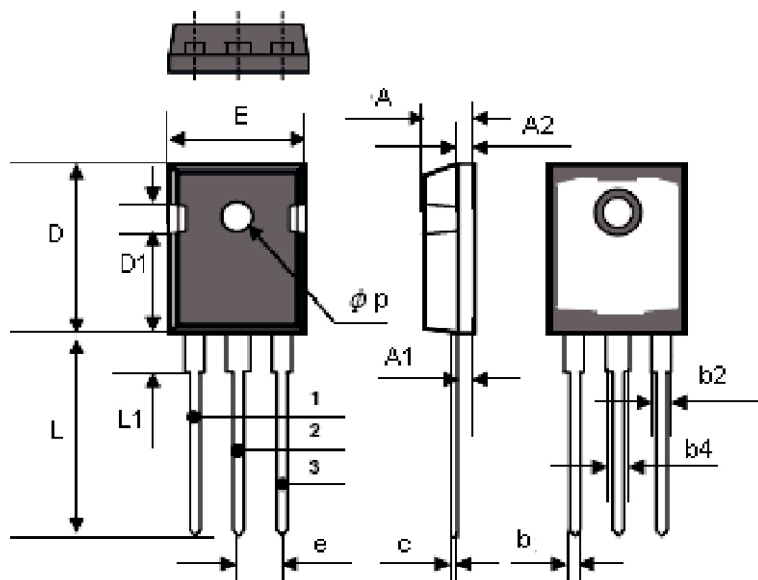


**Fig. 18 - For N-Channel**

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## TO-247AD (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.90	5.10	0.193	0.200
A1	2.30	2.40	0.090	0.094
A2	1.92	2.08	0.076	0.082
b	1.15	1.25	0.045	0.049
b2	1.95	2.05	0.077	0.081
b4	2.85	3.11	0.112	0.122
c	0.6 BSC		0.024 BSC	
D	20.80	21.46	0.819	0.845
D1	4.37	4.63	0.172	0.182
e	5.32	5.58	0.209	0.220
E	15.77	16.03	0.621	0.631
L	19.85	20.11	0.781	0.792
L1	4.07	4.33	0.160	0.170
Ø p	3.56	3.66	0.140	0.144

ECN: X12-0191-Rev. A, 22-Oct-12  
DWG: 6010



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