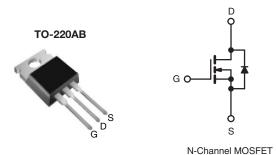


Power MOSFET

PRODUCT SUMM	IARY	
V_{DS} (V) at T_J max.	560)
$R_{DS(on)}(\Omega)$	V _{GS} = 10 V	0.225
Q _g (Max.) (nC)	76	
Q _{gs} (nC)	21	
Q _{gd} (nC)	29	
Configuration	Sing	le



FEATURES

- Low Figure-of-Merit Ron x Qq
- 100 % Avalanche Tested
- High Peak Current Capability
- dV/dt Ruggedness
- Improved t_{rr}/Q_{rr}
- Improved Gate Charge
- High Power Dissipations Capability
- Compliant to RoHS Directive 2002/95/EC



ORDERING INFORMATION	
Package	TO-220AB
Lead (Pb)-free	SiHP18N50C-E3

ABSOLUTE MAXIMUM RATINGS	$T_{\mathbf{C}} = 25 ^{\circ}\mathrm{C},$	unless otherwis	se noted)		
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V _{DS}	500	V
Gate-Source Voltage			V_{GS}	± 30	7 v
Continuous Drain Current (T, = 150 °C) ^a	V _{GS} at 10	T _C = 25 °C		18	
Continuous Drain Current (1) = 150 C)	V _{GS} at 10	T _C = 100 °C	I _D	11	Α
Pulsed Drain Current ^b	•		I _{DM}	72	
Linear Derating Factor		TO-220AB		1.8	W/°C
Single Pulse Avalanche Energy ^c			E _{AS}	361	mJ
Maximum Power Dissipation		TO-220AB	P_{D}	223	W
Peak Diode Recovery dV/dt ^d			dV/dt	5	V/ns
Operating Junction and Storage Temperature F	ange		T _J , T _{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperatur	e) ^d	for 10 s		300	7

Notes

- a. Drain current limited by maximum junction temperature.
- b. Repetitive rating; pulse width limited by maximum junction temperature.
- c. V_{DD} = 50 V, starting T_J = 25 °C, L = 2.5 mH, R_g = 25 Ω , I_{AS} = 17 A.
- d. $I_{SD} \le 18$ A, $dI/dt \le 380$ A/µs, $V_{DD} \le V_{DS}$, $T_J \le 150$ °C.
- e. 1.6 mm from case.

^{*} Pb containing terminations are not RoHS compliant, exemptions may apply



THERMAL RESISTANCE RAT	INGS				
PARAMETER		SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	TO-220	R _{thJA}	-	62	°C/W
Maximum Junction-to-Case (Drain)	TO-220	R _{thJC}	-	0.56	G/VV

PARAMETER	SYMBOL	TES	T CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	V _{GS}	= 0 V, I _D = 250 μA	500	-	-	V
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Referenc	e to 25 °C, I _D = 1 mA	-	0.6	-	V/°C
Gate-Source Threshold Voltage (N)	V _{GS(th)}	V _{DS} :	= V _{GS} , I _D = 250 μA	3.0	-	5.0	V
Gate-Source Leakage	I _{GSS}		V _{GS} = ± 30 V	=	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}		= 500 V, V _{GS} = 0 V	-	-	25	μA
2010 date Voltage Brain Garrent	1033	$V_{DS} = 400 \ V_{DS}$	$V_{\rm H} = 0 V_{\rm H} = 125 ^{\circ}{\rm C}$	-	-	250	μ, ,
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	$I_D = 10 \text{ A}$	-	0.225	0.270	Ω
Forward Transconductance ^a	g_{fs}	V _{DS}	= 50 V, I _D = 10 A	-	6.4	-	S
Dynamic							
Input Capacitance	C _{iss}	$V_{GS} = 0 V$,		ı	2451	2942	pF
Output Capacitance	C_{oss}		V _{DS} = 25 V,		300	360	
Reverse Transfer Capacitance	C _{rss}	f = 1.0 MHz		=	26	32	
Internal Gate Resistance	R _g	f = 1.0 MHz, open drain		-	1.1	-	Ω
Total Gate Charge	Q_g			-	65	76	
Gate-Source Charge	Q _{gs}	V _{GS} = 10 V		=	21	-	nC
Gate-Drain Charge	Q _{gd}	1			29	-	
Turn-On Delay Time	t _{d(on)}			=	80	-	
Rise Time	t _r	V _{DD} =	= 250 V, I _D = 18 A	-	27	-]
Turn-Off Delay Time	t _{d(off)}	$R_g = 7.5 \Omega, V_{GS} = 10 V$		=	32	-	ns
Fall Time	t _f			-	44	-	
Drain-Source Body Diode Characteristic	s						
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	18	_
Pulsed Diode Forward Current	I _{SM}			-	-	72	A
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = 18 A, V _{GS} = 0 V		-	-	1.5	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = I _S , dI/dt = 100 A/µs, V _R = 35 V		-	503	-	ns
Body Diode Reverse Recovery Charge	Q _{rr}			-	6.7	-	μC
Reverse Recovery Current	I _{RRM}			-	30	-	Α

Note

The information shown here is a preliminary product proposal, not a commercial product datasheet. Vishay Siliconix is not committed to produce this or any similar product. This information should not be used for design purposes, nor construed as an offer to furnish or sell such products.

a. Repetitive rating; pulse width limited by maximum junction temperature.



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

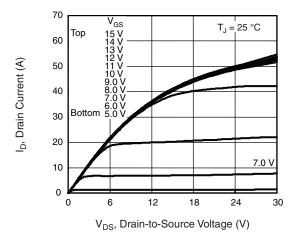


Fig. 1 - Typical Output Characteristics, T_C = 150 $^{\circ}C$

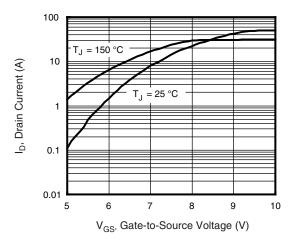


Fig. 3 - Typical Transfer Characteristics

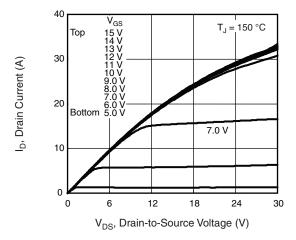


Fig. 2 - Typical Output Characteristics, T_C = 150 °C

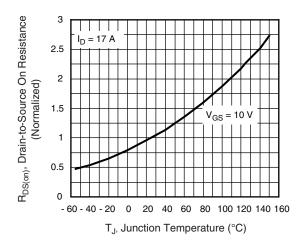


Fig. 4 - Normalized On-Resistance vs. Temperature



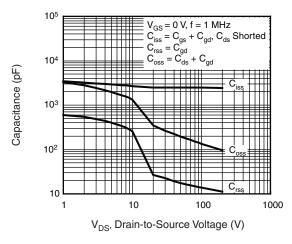


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

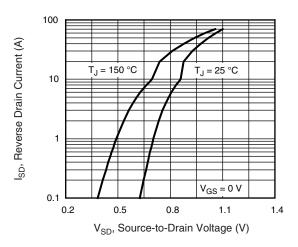


Fig. 7 - Typical Source-Drain Diode Forward Voltage

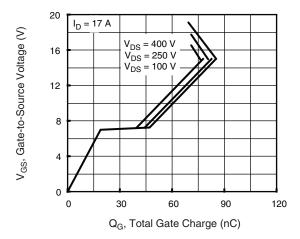


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

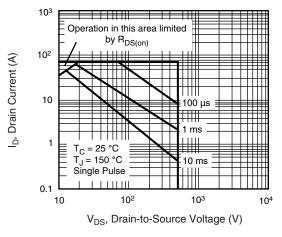


Fig. 8 - Maximum Safe Operating Area

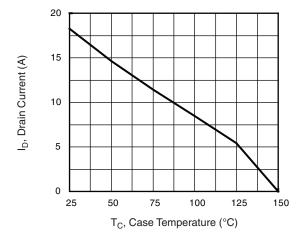


Fig. 9 - Maximum Drain Current vs. Case Temperature



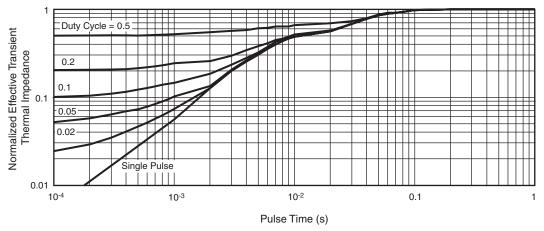


Fig. 10 - Normalized Thermal Transient Impedance, Junction-to-Case

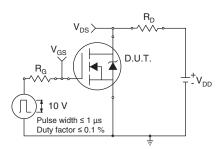


Fig. 11a - Switching Time Test Circuit

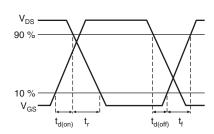


Fig. 11b - Switching Time Waveforms

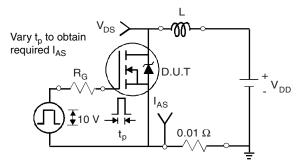


Fig. 12a - Unclamped Inductive Test Circuit

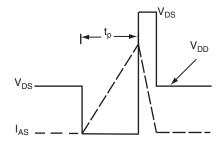


Fig. 12b - Unclamped Inductive Waveforms

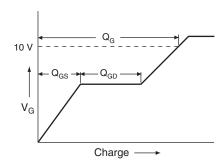


Fig. 13a - Basic Gate Charge Waveform

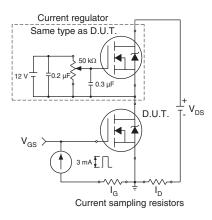
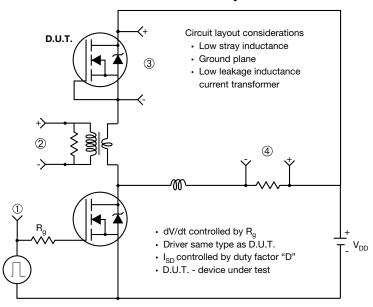


Fig. 13b - Gate Charge Test Circuit



Peak Diode Recovery dV/dt Test Circuit



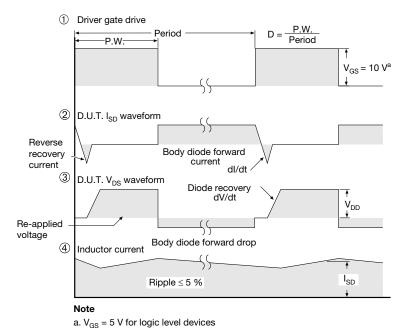
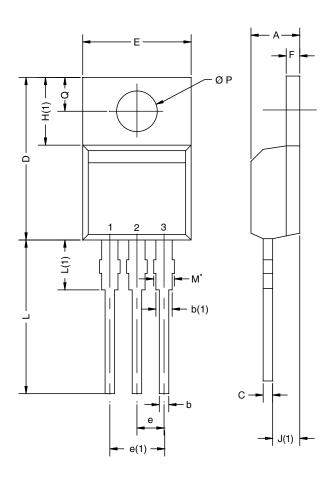


Fig. 14 - For N-Channel

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?91374.



TO-220AB



	MILLIMETERS		INC	HES
DIM.	MIN.	MAX.	MIN.	MAX.
А	4.25	4.65	0.167	0.183
b	0.69	1.01	0.027	0.040
b(1)	1.20	1.73	0.047	0.068
С	0.36	0.61	0.014	0.024
D	14.85	15.49	0.585	0.610
Е	10.04	10.51	0.395	0.414
е	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.09	6.48	0.240	0.255
J(1)	2.41	2.92	0.095	0.115
L	13.35	14.02	0.526	0.552
L(1)	3.32	3.82	0.131	0.150
ØΡ	3.54	3.94	0.139	0.155
Q	2.60	3.00	0.102	0.118
ECN: T13-0	724-Rev. O,	14-Oct-13		·

DWG: 5471

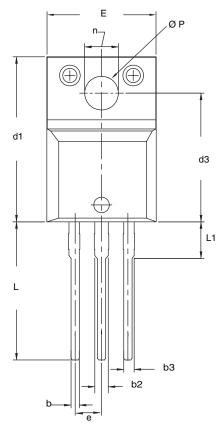
Note

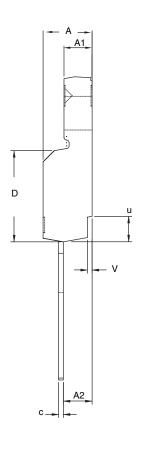
 $^{^{\}star}$ M = 1.32 mm to 1.62 mm (dimension including protrusion) Heatsink hole for HVM





TO-220 FULLPAK (HIGH VOLTAGE)





	MILLII	METERS	INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
Α	4.570	4.830	0.180	0.190
A1	2.570	2.830	0.101	0.111
A2	2.510	2.850	0.099	0.112
b	0.622	0.890	0.024	0.035
b2	1.229	1.400	0.048	0.055
b3	1.229	1.400	0.048	0.055
С	0.440	0.629	0.017	0.025
D	8.650	9.800	0.341	0.386
d1	15.88	16.120	0.622	0.635
d3	12.300	12.920	0.484	0.509
E	10.360	10.630	0.408	0.419
е	2.54	BSC	0.100	BSC
L	13.200	13.730	0.520	0.541
L1	3.100	3.500	0.122	0.138
n	6.050	6.150	0.238	0.242
ØΡ	3.050	3.450	0.120	0.136
u	2.400	2.500	0.094	0.098
V	0.400	0.500	0.016	0.020

EUN: X09-0126-Rev. B, 26-Oct-09 DWG: 5972

- To be used only for process drawing.
 These dimensions apply to all TO-220, FULLPAK leadframe versions 3 leads.
 All critical dimensions should C meet C_{pk} > 1.33.
- 4. All dimensions include burrs and plating thickness.
- 5. No chipping or package damage.

Document Number: 91359 Revision: 26-Oct-09



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Vishay

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Revision: 02-Oct-12 Document Number: 91000