



Dual N-Channel 30 V (D-S) MOSFET

PRODUCT SUMMARY				
V _{DS} (V)	$R_{DS(on)}\left(\Omega\right)$	I _D (A) ^a	Q _g (Typ.)	
30	0.0195 at V _{GS} = 10 V	8.5	7.1	
	0.023 at V _{GS} = 4.5 V	8.6	7.1	

FEATURES

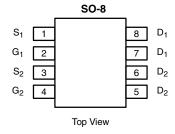
- TrenchFET® Power MOSFET
- 100 % R_g Tested
- 100 % UIS Tested
- Compliant to RoHS Directive 2002/95/EC



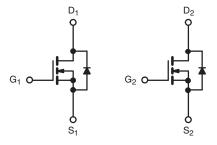
COMPLIANT

APPLICATIONS

- Notebook System Power
- Low Current DC/DC



Ordering Information: Si4214DDY-T1-E3 (Lead (Pb)-free)



N-Channel MOSFET

N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $(T_A =$	25 °C, unless other	rwise noted)			
Parameter	Symbol	Limit	Unit		
Drain-Source Voltage	V_{DS}	30	V		
Gate-Source Voltage	V_{GS}	± 20]		
	T _C = 25 °C		8.5		
Continuous Drain Current (T _{.1} = 150 °C)	T _C = 70 °C	I _D	7.5		
Continuous Brain Current (1) = 100 °C)	T _A = 25 °C		7.5 ^{b, c}		
	T _A = 70 °C		5.9 ^{b, c}		
Pulsed Drain Current		I _{DM}	30	A	
Source-Drain Current Diode Current	T _C = 25 °C	- I _S	2.8		
Source-Drain Current blode Current	T _A = 25 °C	'S	1.8 ^{b, c}		
Pulsed Source-Drain Current		I _{SM}	30		
Single Pulse Avalanche Current	L = 0.1 mH	I _{AS}	10		
Single Pulse Avalanche Energy	L = 0.111111	E _{AS}	5		
	T _C = 25 °C		3.1		
Maximum Power Dissipation	$T_C = 70 ^{\circ}C$	P_{D}	2.0	W	
Maximum Fower Dissipation	T _A = 25 °C		2.0 ^{b, c}		
	T _A = 70 °C		1.25 ^{b, c}		
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C		

THERMAL RESISTANCE RATINGS						
Parameter	Symbol	Тур.	Max.	Unit		
Maximum Junction-to-Ambient ^{b, d}	t ≤ 10 s	R _{thJA}	52	62.5	°C/W	
Maximum Junction-to-Foot (Drain)	Steady-State	R_{thJF}	30	40	7 0/11	

- a. Based on $T_C = 25$ °C.
- b. Surface mounted on 1" x 1" FR4 board.
- c. t = 10 s.
- d. Maximum under steady state conditions is 110 °C/W.

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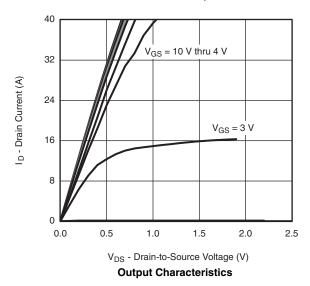
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Static	7			<u> </u>		
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	30			V
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$ $I_D = 250 \mu A$			3.0		
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I _D = 250 μA		- 5.2		mV/°C
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	1.2		2.5	V
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			100	nA
·	,	V _{DS} = 30 V, V _{GS} = 0 V			1	μΑ
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V, TJ = 55 °C			10	
On -State Drain Current ^b	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 10 V	20			Α
Drain-Source On-State Resistance ^b		V _{GS} = 10 V, I _D = 8 A		0.016	0.0195	Ω
	R _{DS(on)}	$V_{GS} = 4.5 \text{ V}, I_D = 5 \text{ A}$		0.019	0.023	
Forward Transconductance ^b	9 _{fs}	V _{DS} = 15 V, I _D = 8 A		27		S
Dynamic ^a						
Input Capacitance	C _{iss}			660		pF
Output Capacitance	C _{oss}	V _{DS} = 15 V, V _{GS} = 0 V, I _D = 1 MHz		140		
Reverse Transfer Capacitance	C _{rss}	[86		
Tabal Oada Obaana		$V_{DS} = 15 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 8 \text{ A}$		14.5	22	nC
Total Gate Charge	Q _g			7.1	11	
Gate-Source Charge	Q _{gs}	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 8 \text{ A}$		1.9		
Gate-Drain Charge	Q_{gd}			2.7		
Gate Resistance	R_g	f = 1 MHz	0.5	2.6	5.2	Ω
Turn-On Delay Time	t _{d(on)}			14	28	
Rise Time	t _r	$V_{DD} = 15 \text{ V}, R_L = 3 \Omega$		45	80	
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 5 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$		18	35	
Fall Time	t _f			12	24	no
Turn-On Delay Time	t _{d(on)}			7	14	ns
Rise Time	t _r	V_{DD} = 15 V, R_L = 3 Ω		10	20	
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 5 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$		15	30	
Fall Time	t _f			7	14	
Drain-Source Body Diode Characteristi	cs					
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			2.8	^
Pulse Diode Forward Current ^a	I _{SM}				30	Α
Body Diode Voltage	V_{SD}	I _S = 2 A		0.77	1.1	V
Body Diode Reverse Recovery Time	t _{rr}			17	34	ns
Body Diode Reverse Recovery Charge	Q_{rr} $I_F = 5 \text{ A, dl/dt} = 100 \text{ A/µs, T}_J = 25 °C$			9	18	nC
Reverse Recovery Fall Time	t _a	- 1F = 5 A, αι/αι = 100 A/μs, 1j = 25 °C		10		nC
Reverse Recovery Rise Time	t _b	7		7		- nS

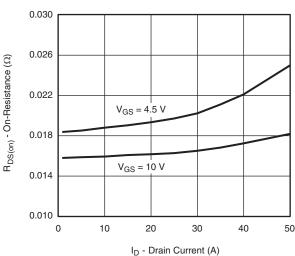
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



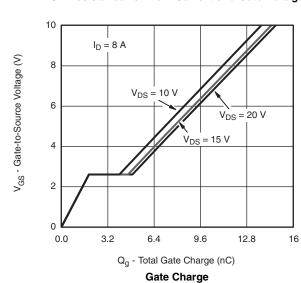


TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



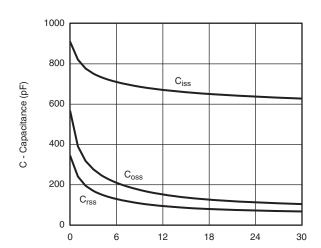


On-Resistance vs. Drain Current and Gate Voltage

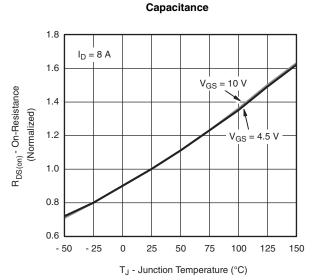


10 8 I_D - Drain Current (A) 6 T_C = 25 °C 2 125 °C T_{C} 55 °C $T_C =$ 0 0

V_{GS} - Gate-to-Source Voltage (V) **Transfer Characteristics**



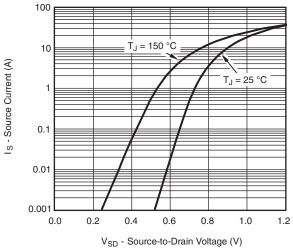
V_{DS} - Drain-to-Source Voltage (V)



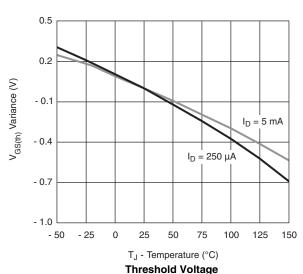
On-Resistance vs. Junction Temperature

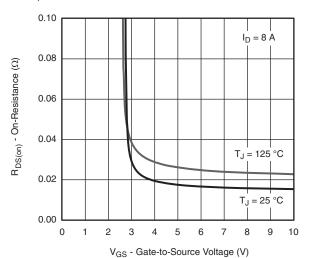
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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

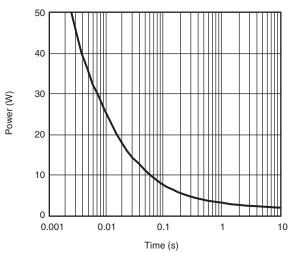


Source-Drain Diode Forward Voltage

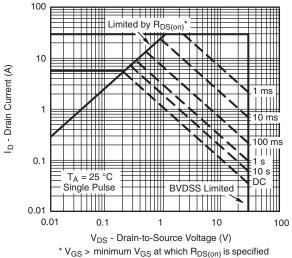




On-Resistance vs. Gate-to-Source Voltage



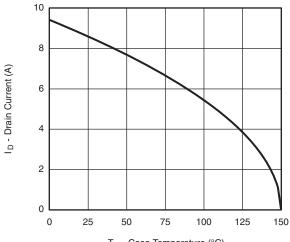
Single Pulse Power, Junction-to-Ambient



Safe Operating Area, Junction-to-Ambient

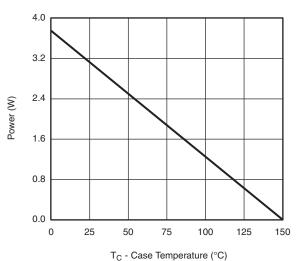


TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

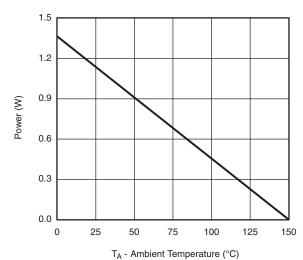


T_C - Case Temperature (°C)

Current Derating*





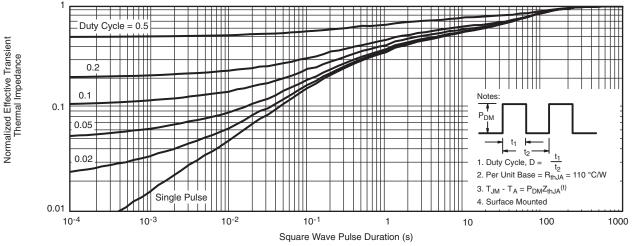


Power Derating, Junction-to-Ambient

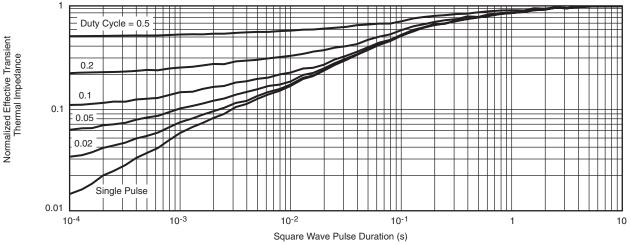
^{*} The power dissipation PD is based on TJ(max) = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations.



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