

# 4V Drive Nch + Nch MOSFET

## SH8K15

### ● Structure

Silicon N-channel MOSFET

### ● Features

- 1) Low on-resistance.
- 2) Built-in G-S Protection Diode.
- 3) Small Surface Mount Package (SOP8).

### ● Application

Switching

### ● Packaging specifications

Type	Package	Taping
	Code	TB
	Basic ordering unit (pieces)	2500
SH8K15		○

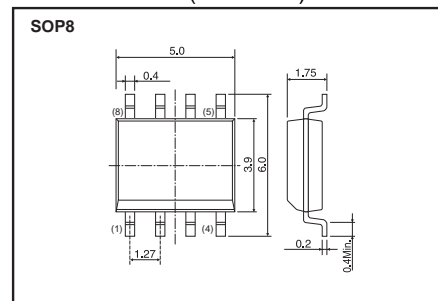
### ● Absolute maximum ratings (Ta = 25°C)

Parameter		Symbol	Limits	Unit
Drain-source voltage		$V_{DSS}$	30	V
Gate-source voltage		$V_{GSS}$	±20	V
Drain current	Continuous	$I_D$	±9.0	A
	Pulsed	$I_{DP}$ *1	±36	A
Source current (Body Diode)	Continuous	$I_s$	1.6	A
	Pulsed	$I_{sp}$ *1	36	A
Power dissipation		$P_D$ *2	2.0	W / TOTAL
			1.4	W / ELEMENT
Channel temperature		$T_{ch}$	150	°C
Range of storage temperature		$T_{stg}$	-55 to +150	°C

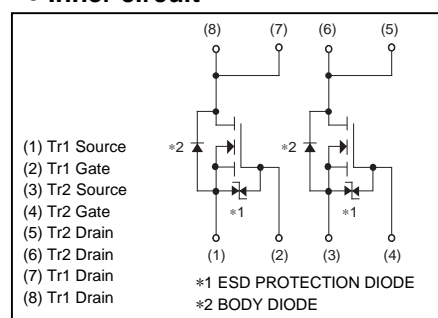
 \*1  $P_w \leq 10\mu s$ , Duty cycle  $\leq 1\%$ 

\*2 Mounted on a ceramic board.

### ● Dimensions (Unit : mm)



### ● Inner circuit



● **Electrical characteristics** (Ta = 25°C)

<It is the same ratings for Tr1 and Tr2.>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	$I_{GSS}$	-	-	$\pm 10$	$\mu A$	$V_{GS} = \pm 20V, V_{DS} = 0V$
Drain-source breakdown voltage	$V_{(BR)DSS}$	30	-	-	V	$I_D = 1mA, V_{GS} = 0V$
Zero gate voltage drain current	$I_{DSS}$	-	-	1	$\mu A$	$V_{DS} = 30V, V_{GS} = 0V$
Gate threshold voltage	$V_{GS(th)}$	1.0	-	2.5	V	$V_{DS} = 10V, I_D = 1mA$
Static drain-source on-state resistance	$R_{DS(on)}^*$	-	15	21	$m\Omega$	$I_D = 9.0A, V_{GS} = 10V$
		-	18	25		$I_D = 9.0A, V_{GS} = 4.5V$
		-	20	28		$I_D = 9.0A, V_{GS} = 4.0V$
Forward transfer admittance	$ Y_{fs} ^*$	5.0	-	-	S	$I_D = 9.0A, V_{DS} = 10V$
Input capacitance	$C_{iss}$	-	630	-	pF	$V_{DS} = 10V$
Output capacitance	$C_{oss}$	-	230	-	pF	$V_{GS} = 0V$
Reverse transfer capacitance	$C_{rss}$	-	110	-	pF	$f = 1MHz$
Turn-on delay time	$t_{d(on)}^*$	-	10	-	ns	$I_D = 4.5A, V_{DD} \approx 15V$
Rise time	$t_r^*$	-	33	-	ns	$V_{GS} = 10V$
Turn-off delay time	$t_{d(off)}^*$	-	42	-	ns	$R_L = 3.3\Omega$
Fall time	$t_f^*$	-	10	-	ns	$R_G = 10\Omega$
Total gate charge	$Q_g^*$	-	8.5	-	nC	$I_D = 9A$
Gate-source charge	$Q_{gs}^*$	-	2.3	-	nC	$V_{DD} \approx 15V$
Gate-drain charge	$Q_{gd}^*$	-	4.0	-	nC	$V_{GS} = 5V$

\*Pulsed

● **Body diode characteristics** (Source-Drain) (Ta = 25°C)

<It is the same ratings for Tr1 and Tr2.>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward Voltage	$V_{SD}^*$	-	-	1.2	V	$I_S = 9.0A, V_{GS} = 0V$

\*Pulsed

●Electrical characteristic curves (Ta=25°C)

Fig.1 Typical Output Characteristics ( I )

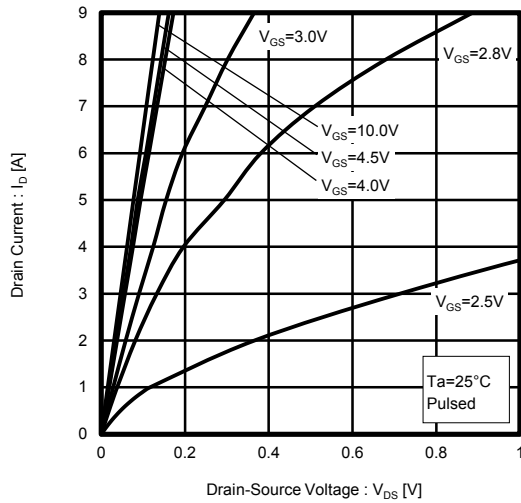


Fig.2 Typical Output Characteristics ( II )

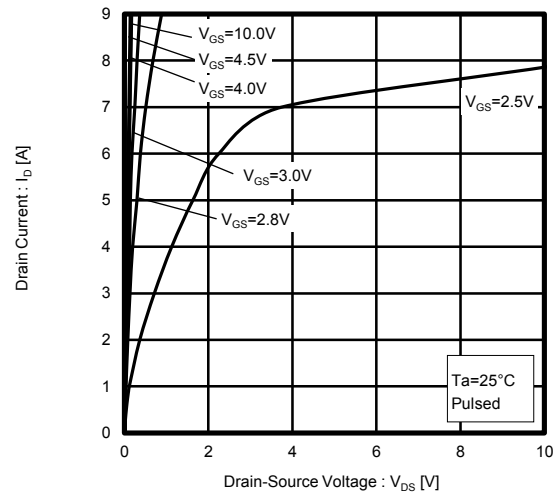


Fig.3 Static Drain-Source On-State Resistance vs. Drain Current

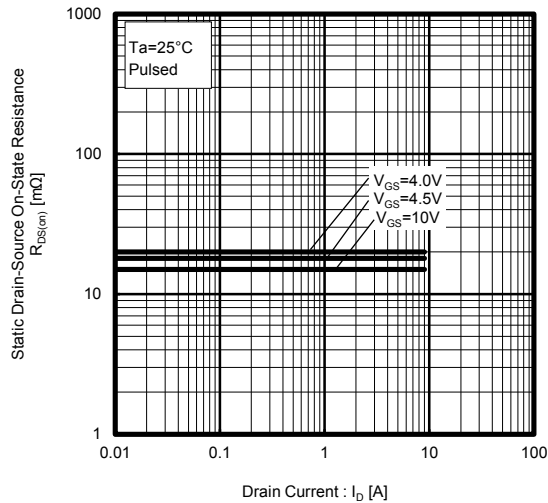


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current

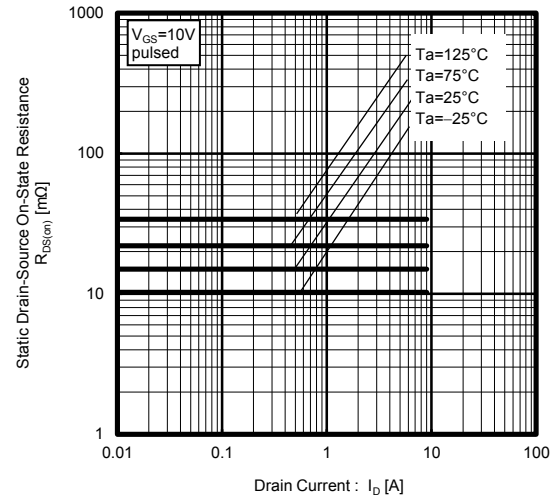


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current

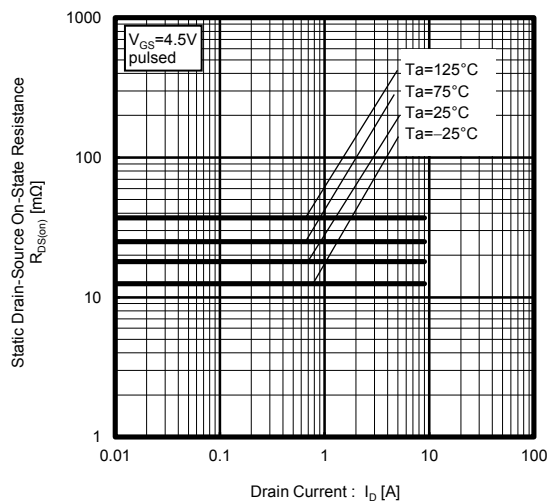


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current

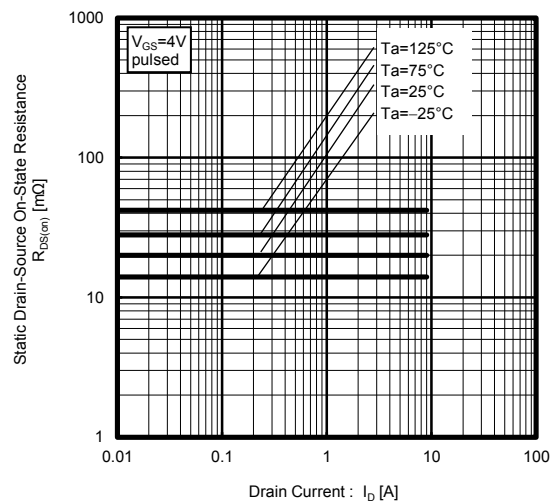


Fig.7 Forward Transfer Admittance vs. Drain Current

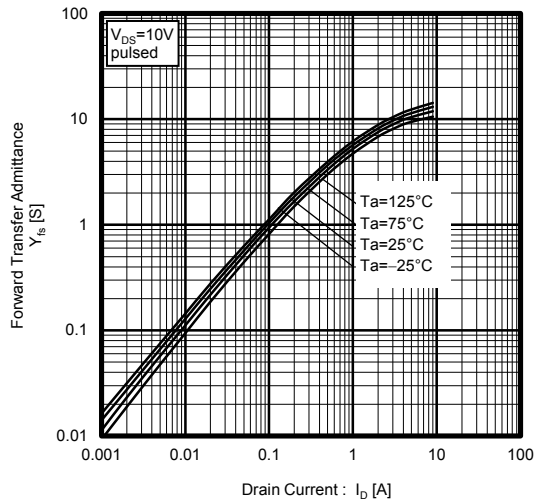


Fig.8 Typical Transfer Characteristics

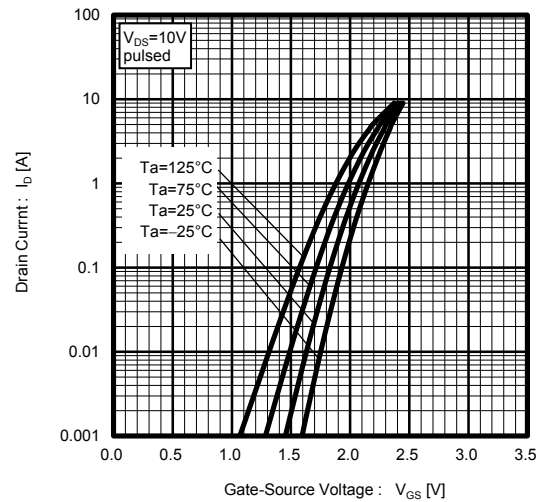


Fig.9 Source Current vs. Source-Drain Voltage

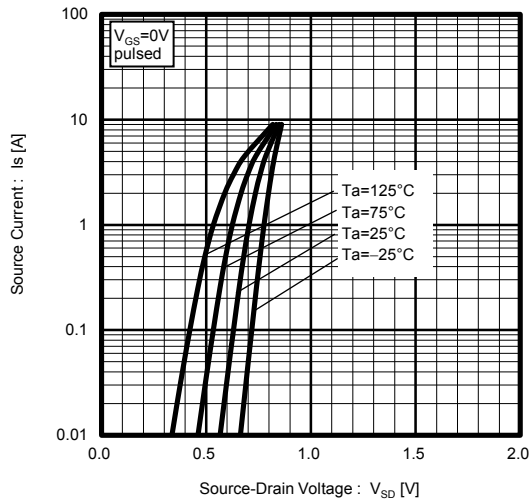


Fig.10 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

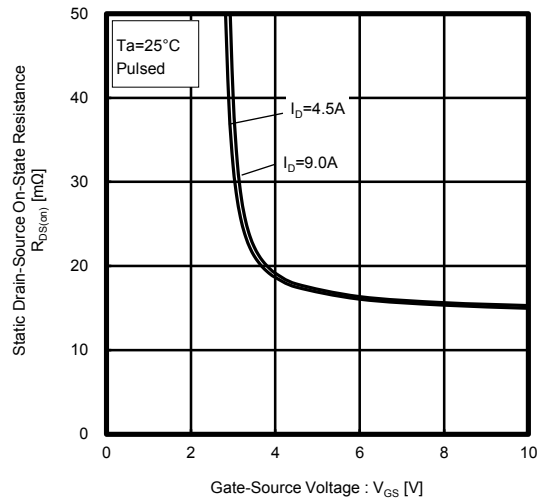


Fig.11 Switching Characteristics

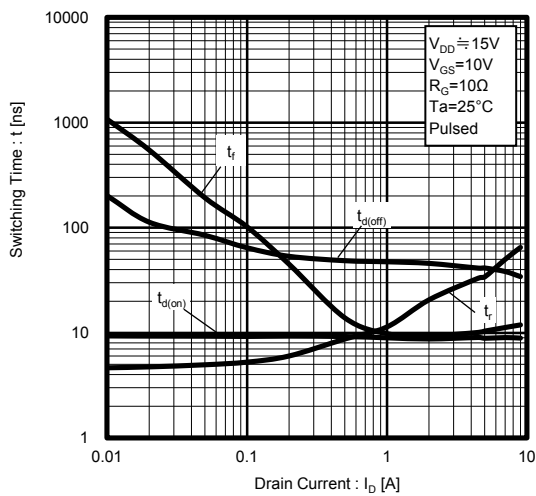


Fig.12 Dynamic Input Characteristics

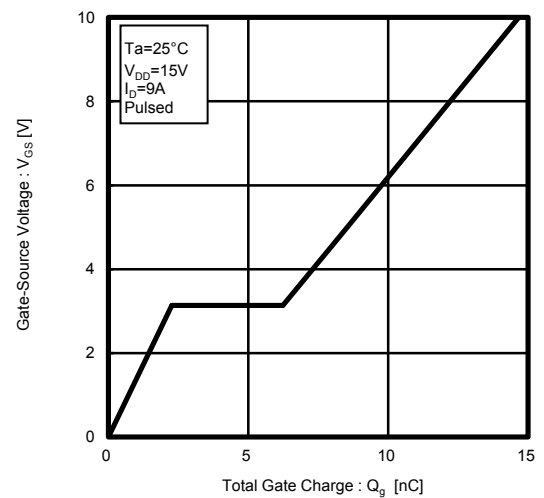


Fig.13 Typical Capacitance vs. Drain-Source Voltage

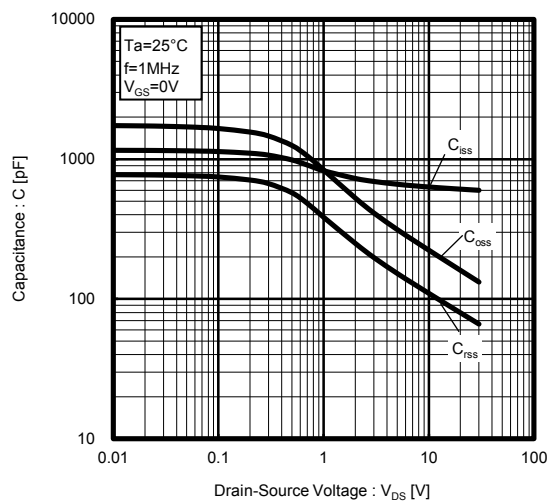


Fig.14 Maximum Safe Operating Area

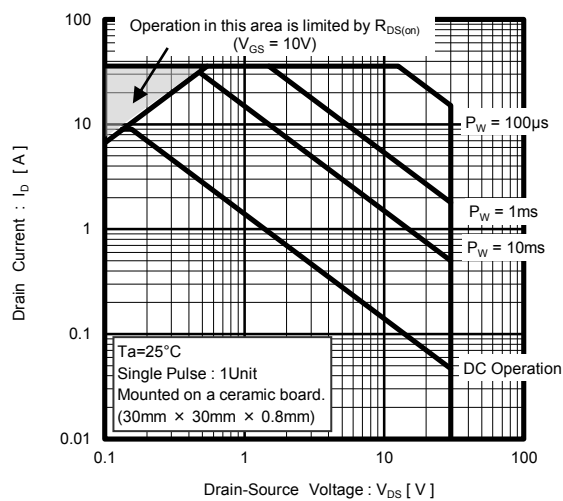
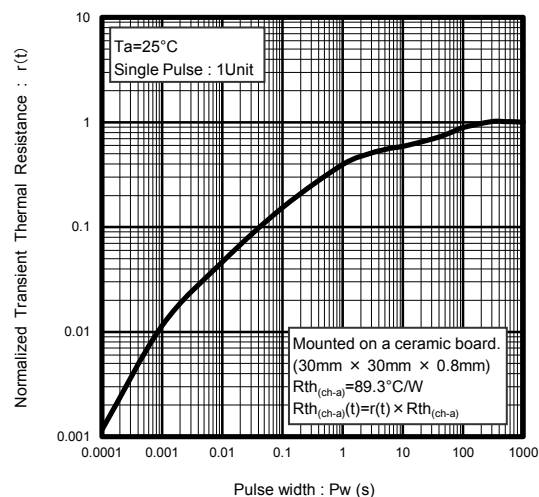


Fig.15 Normalized Transient Thermal Resistance v.s. Pulse Width



## ● Measurement circuits

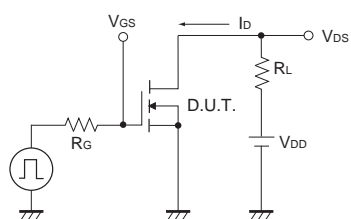


Fig.1-1 Switching Time Measurement Circuit

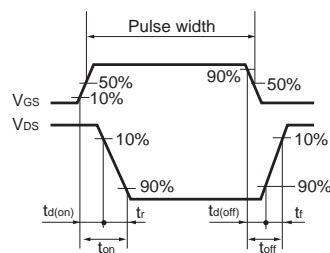


Fig.1-2 Switching Waveforms

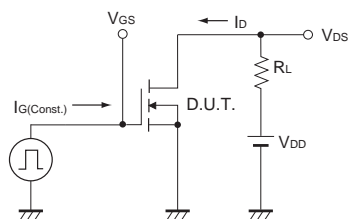


Fig.2-1 Gate Charge Measurement Circuit

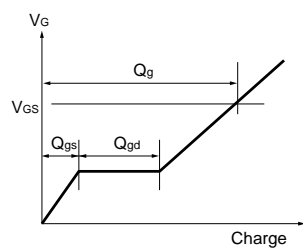


Fig.2-2 Gate Charge Waveform

## ● Notice

This product might cause chip aging and breakdown under the large electrified environment. Please consider to design ESD protection circuit.

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