

DAC31x2EVM

This document is a user's guide for the DAC31x2EVM, an evaluation fixture for the <u>DAC3152</u> and <u>DAC3162</u> (DAC31x2) series of dual-channel, 10-/12-bit, 500-MSPS digital-to-analog converters (DACs). The DAC31x2EVM includes the <u>TRF3703-33</u> quadrature modulator to facilitate measuring the output signals at a desired RF frequency. The EVM also includes the <u>CDCP1803</u> clock buffer that distributes the clocks to the DAC, as well as a pattern generator. This EVM is ideally suited for mating with the <u>TSW3100</u> pattern generation card for evaluating QAM, WCDMA, LTE, or other high-performance modulation schemes. For more information about the DAC31x2 family, see the <u>product data sheet</u> (available for download at <u>www.ti.com</u>).

Throughout this document, the acronym *EVM* and the phrases *evaluation module* and *evaluation fixture* are synonymous with the DAC31x2EVM.

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TEXAS INSTRUMENTS

Introduction

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1 Introduction

1.1 Block Diagram

Figure 1 shows the DAC31x2EVM block diagram.

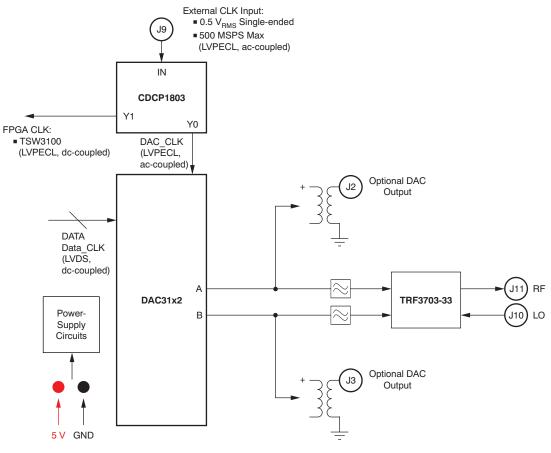


Figure 1. DAC31x2EVM Block Diagram

1.2 Software Control

No software is required to use the DAC31x2EVM.



2 Testing and Configuration

This section outlines the basic procedure for testing the DAC31x2EVM.

2.1 Test Set-Up

Figure 2 illustrates the test configuration for general testing of the DAC31x2 with the TSW3100 pattern generation card.

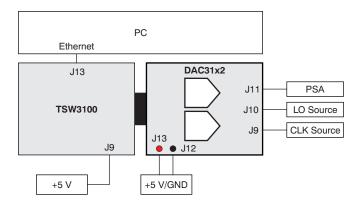


Figure 2. DAC31x2EVM Test Setup

2.2 Test Set-Up Connections

Follow these procedures to properly connect the DAC31x2EVM and the TSW3100 pattern generator.

TSW3100 Pattern Generator:

- Connect a 5-V power supply to J9, the 5V_IN jack of the TSW3100EVM.
- Connect the PC Ethernet port to J13, the Ethernet port of the TSW3100. The cable should be a standard crossover Cat5e Ethernet cable.

DAC31x2EVM:

- Connect the J5 connector of DAC31x2EVM to connector J74 of the TSW3100EVM.
- Connect 5 V and Ground to connectors J12 and J13 respectively.
- Provide a 0.5-V_{RMS}, 500-MHz (max) clock at J9, the CLOCK IN SMA port of the DAC31x2EVM.
- Provide a 7-dBm, 350-MHz to 4-GHz local oscillator (LO) source at port J10 of the DAC31x2EVM. This
 input provides the LO source to the TRF3703-33 modulators.
- Connect the RF output port of (J11) to the spectrum analyzer.

DAC31x2EVM Jumpers:

Power distribution to the DAC31x2 and CDCP1803 devices on the EVM can be achieved through low-dropout regulators (LDOs) or dc-dc converters. Jumpers JP24, JP25, JP26, and JP27 allow the user to choose one of the power schemes from these two available options. The default setting of these jumpers is shown; these settings use power management for the ICs through dc-dc switchers.

- JP24 on pin {1,2}
- JP25 on pin {1,2}
- JP26 on pin {1,2}
- JP27 on pin {1,2}

Jumper JP4 supplies power to the TRF3703-33 modulator. This jumper must be installed in order to use the modulator.



Testing and Configuration

2.3 TSW3100 Quick-Start Operation

Refer to the <u>TSW3100 User's Guide</u> for a more detailed discussion of how to set up and operate the TSW3100. This user guide presumes that the TSW3100 software is installed and functioning properly.

CommsSignalPattern Setup from Default Configuration (WCDMA):

- Step 1. Change the interpolation value to DAC Clock Rate / 3.84 (that is, 491.52/3.84 = 128).
- Step 2. Enter the desired offset frequency (for example, 30 MHz) for each desired carrier.
- Step 3. Select the LVDS Output button.
- Step 4. Select the Offset Binary option.
- Step 5. Check the LOAD and Run box.
- Step 6. Press the green **Create** button.

Figure 3 shows a screenshot of the properly configured TSW3100 software interface.

TSW3100_CommSignalPattern_v2p7		
Test Models Signal Type TM1 - 64ch Complex TM3 - 32ch Complex IF TM5 - 30ch Swap I/Q OAM QAM	Res DVV –30000 Hz	 max size ✓ time offset Random Seed Invert Time (ms) =1.1
Center Frequency fs:/4 ExactFreq 30.72 IF (MHz) Display Options CCDF plot Ext FFT Plot Q vs T 30 ResBW (kHz)	160 140 (Ep) 120 120 100 100 80	
Carriers Enable Off Freq (MHz) Gain (dB) SCR Code Carrier 1 30 0 0 Carrier 2 -2.5 0 1 Carrier 2 -2.5 0 1	60 40	100 150 200 250
Carrier 3 2.5 0 2	master slave CMOS GC5325 GC5325 Bit Reverse I	LOAD and Run Interleaved Stop 16b MSB Justify 192.168.1.12 Ping Ping
Create v2.7 (c) 2005-2010 Texas Instruments		

Figure 3. TSW3100 CommsSignalPattern (WCDMA) Programming GUI

2.4 DAC31x2EVM Configuration for Modulator Output

Follow these steps to set up the DAC31x2EVM and perform a spectrum analysis.

- Step 1. Set the clock input to 491.52 MHz at 0.5 V_{RMS} at the J9 SMA connector of the DAC31x2EVM.
- Step 2. Supply the LO source of 900 MHz (7 dBm) at the J10 SMA connector of the DAC31x2EVM.
- Step 3. Turn on power to the board at J12/J13.
- Step 4. Verify the spectrum using the Spectrum Analyzer at the RF output of the DAC31x2EVM (J11).

A typical WCDMA output from a wave analyzer is shown in Figure 4.

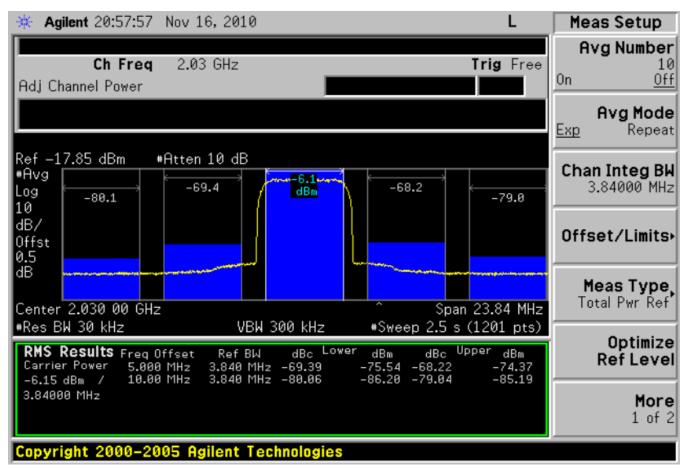


Figure 4. DAC3162EVM and TRF3703-33 WCDMA Output



Testing and Configuration

2.5 DAC31x2EVM Configuration for DAC Output

Follow this procedure to configure the DAC31x2EVM in order to test the EVM signal output.

- Step 1. Four $0-\Omega$ resistors must be moved in order to configure the output of the DAC31x2 as 1:1 transformer-coupled.
 - Remove the resistors R109, R110, R111, and R112
 - Install the resistors R211, R207, R191, and R195
- Step 2. Provide the clock input: 491.52 MHz at 1.5 V_{RMS} at the J9 SMA connector of the DAC31x2EVM.
- Step 3. Turn on power to the board at J12/J13.
- Step 4. Verify the spectrum using the Spectrum Analyzer at the two DAC outputs of the DAC31x2EVM (J3 and J2).

Figure 5 illustrates a typical transformer-coupled output using a wave analyzer.

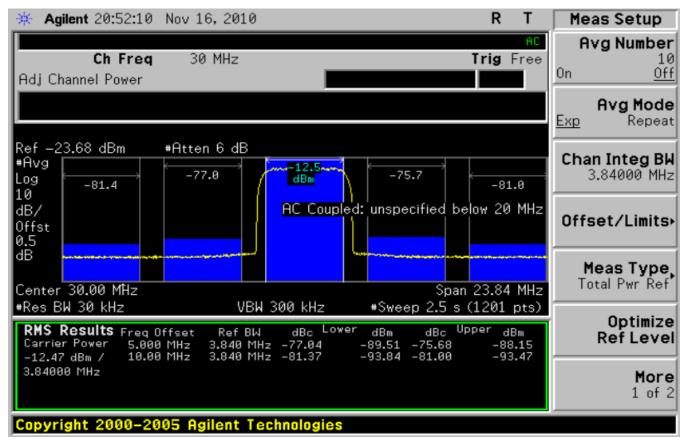


Figure 5. DAC3162EVM Transformer-Coupled Output at 30 MHz IF

DAC31x2EVM



Revision History

Changes from Original (November, 2010) to A Revision Pa			
•	Updated abstract to reflect device availability; removed DAC3172 from associated devices	1	
•	Updated title of Figure 4	5	
•	Changed title of Figure 5	. 6	

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 5 V to 7 V and the output voltage range of 2.8 V to 3.8 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than +55° C. The EVM is designed to operate properly with certain components above +55° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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