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April 1<sup>st</sup>, 2010 Renesas Electronics Corporation

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# HA1630S01/02/03 Series

# Ultra-Small Low Voltage Operation CMOS Single Operational Amplifier

REJ03D0798-0100 Rev.1.00 Mar 10, 2006

#### **Description**

The HA1630S01/02/03 are single CMOS Operational Amplifiers realizing low voltage operation, low input offset voltage and low supply current. In addition to a low operating voltage from 1.8V, these device output can achieve full swing output voltage capability extending to either supply. Available in an ultra-small CMPAK-5 package that occupies only 1/8 the area of the SOP-8 package.

#### **Features**

Low power and single supply operation
 Low input offset voltage
  $V_{DD} = 1.8$  to 5.5 V
  $V_{IO} = 4.0$  mV Max

• Low supply current  $I_{DD} = 15 \mu A \text{ Typ (HA1630S01)}$ 

 $I_{DD} = 50 \mu A \text{ Typ (HA1630S02)}$  $I_{DD} = 100 \mu A \text{ Typ (HA1630S03)}$ 

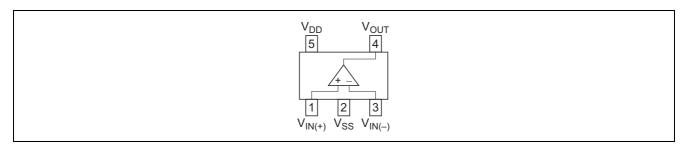
• Maximum output voltage  $V_{OH} = 2.9 \text{ V Min (at } V_{DD} = 3.0 \text{ V})$ 

• Low input bias current  $I_{IB} = 1 pA Typ$ 

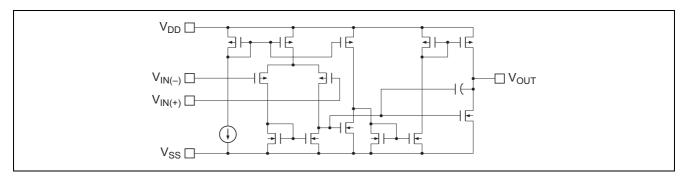
## **Ordering Information**

Type No.	Package Name	Package Code	
HA1630S01CM	CMPAK-5	PTSP0005ZC-A	
HA1630S01LP	MPAK-5	PLSP0005ZB-A	
HA1630S02CM	CMPAK-5	PTSP0005ZC-A	
HA1630S02LP	MPAK-5	PLSP0005ZB-A	
HA1630S03CM	CMPAK-5	PTSP0005ZC-A	
HA1630S03LP	MPAK-5	PLSP0005ZB-A	

# **Pin Arrangement**



# **Equivalent Circuit**



## **Absolute Maximum Ratings**

 $(Ta = 25^{\circ}C)$ 

Items	Symbol	Ratings	Unit	Note
Supply voltage	$V_{DD}$	7	V	
Differential input voltage	V <sub>IN(diff)</sub>	$-V_{DD}$ to $+V_{DD}$	V	
Input voltage	V <sub>IN</sub>	-0.3 to +V <sub>DD</sub>	V	1
Power dissipation	P <sub>T</sub>	200	mW	
Operating temp. Range	Topr	-40 to +85	°C	
Storage temp. Range	Tstg	-55 to +125	°C	

Note: 1. Do not apply Input Voltage exceeding  $V_{DD}$  or 7 V.

### **Electrical Characteristics**

 $(V_{DD} = 3.0 \text{ V}, \text{Ta} = 25^{\circ}\text{C})$ 

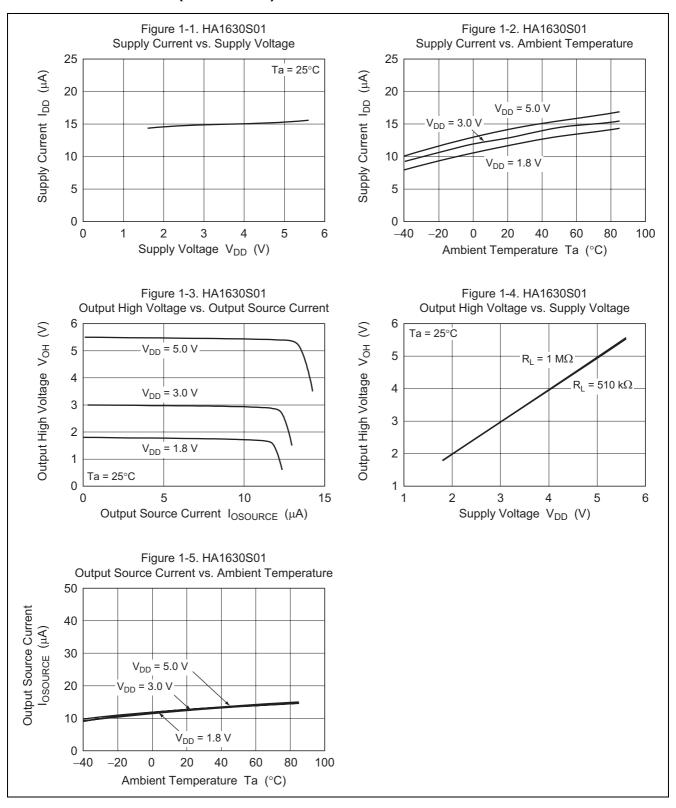
Items	Symbol	Min	Тур	Max	Unit	Test Condition
Input offset voltage	V <sub>IO</sub>	_		4.0	mV	Vin = 1.5 V
Input offset current	I <sub>IO</sub>	_	(1.0)	_	pА	Vin = 1.5 V
Input bias current	I <sub>IB</sub>	_	(1.0)	_	pА	Vin = 1.5 V
Output high voltage	VoH	2.9	_	_	V	$R_L = 1 M\Omega$
Output source current	I <sub>O SOURCE</sub>	6	12	_	μΑ	V <sub>OH</sub> = 2.5 V (HA1630S01)
		25	50	_		V <sub>OH</sub> = 2.5 V (HA1630S02)
		50	100	_		V <sub>OH</sub> = 2.5 V (HA1630S03)
Output low voltage	V <sub>OL</sub>	_	_	0.1	V	$R_L = 1 M\Omega$
Output sink current	I <sub>O SINK</sub>	_	(0.8)	_	mA	V <sub>OL</sub> = 0.5 V (HA1630S01)
		_	(1.0)	_		V <sub>OL</sub> = 0.5 V (HA1630S02)
		_	(1.2)	_		V <sub>OL</sub> = 0.5 V (HA1630S03)
Common mode input voltage	V <sub>CM</sub>	-0.1 to 2.1	_	_	V	
range						
Slew rate	SR	_	(0.125)	_	V/μs	$C_L = 20 \text{ pF (HA1630S01)}$
		_	(0.50)	_		$C_L = 20 \text{ pF (HA1630S02)}$
		_	(1.00)	_		$C_L = 20 \text{ pF (HA1630S03)}$
Voltage gain	$A_V$	60	100	_	dB	
Gain bandwidth product	BW	_	(200)	_	kHz	$C_L = 20 \text{ pF (HA1630S01)}$
		_	(680)	_		$C_L = 20 \text{ pF (HA1630S02)}$
			(1200)	_		$C_L = 20 \text{ pF (HA1630S03)}$
Power supply rejection ratio	PSRR	60	80	_	dB	
Common mode rejection ratio	CMRR	60	80	_	dB	
Supply current	I <sub>DD</sub>	_	15	30	μΑ	R <sub>L</sub> = ∞ (HA1630S01)
			50	100		R <sub>L</sub> = ∞ (HA1630S02)
			100	200		R <sub>L</sub> = ∞ (HA1630S03)

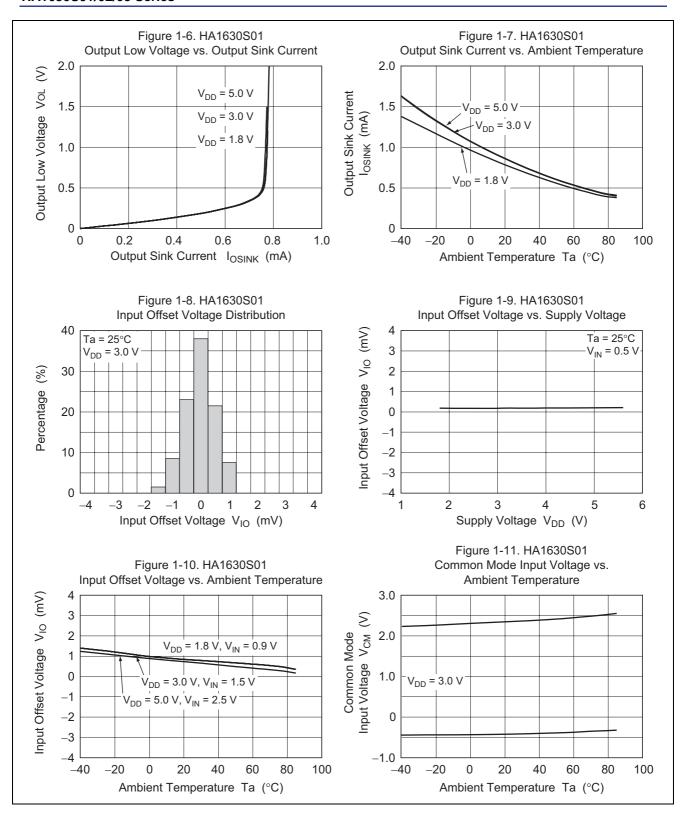
Note: 1. ( ): Design specification

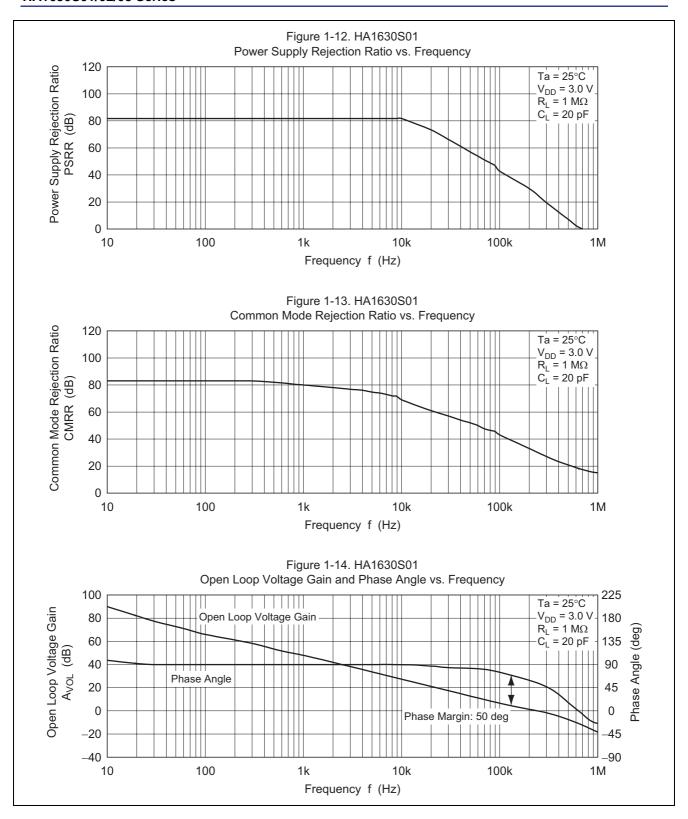
## **Table of Graphs**

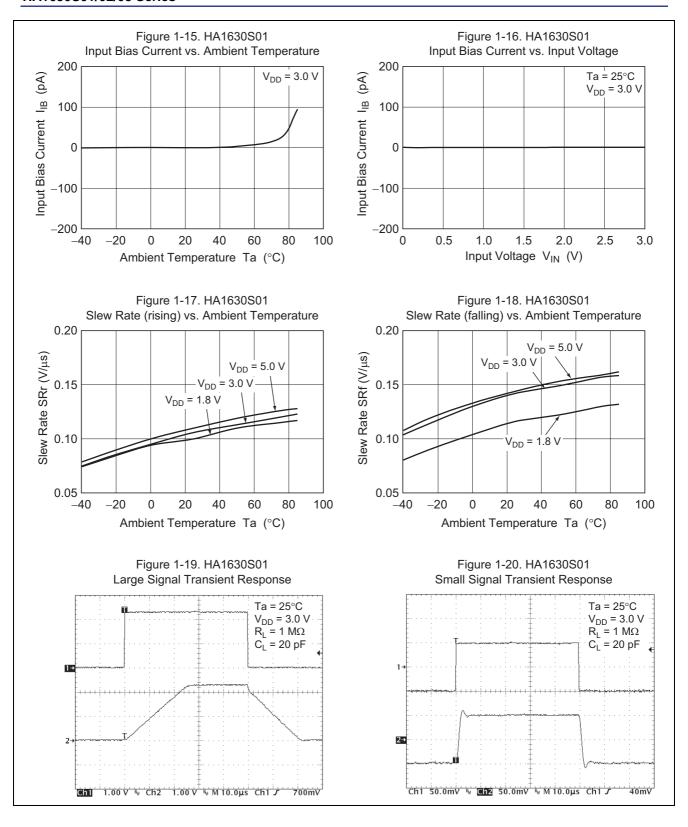
Et.,			HA1630S01	HA1630S02	HA1630S03	Test
	cal Characte	1	Figure	Figure	Figure	Circuit
Supply current	$I_{DD}$	vs Supply voltage	1-1	2-1	3-1	2
		vs Ambient temperature	1-2	2-2	3-2	
Output high voltage	$V_{OH}$	vs Output source current	1-3	2-3	3-3	4
		vs Supply voltage	1-4	2-4	3-4	
Output source current	I <sub>O SOURCE</sub>	vs Ambient temperature	1-5	2-5	3-5	6
Output low voltage	$V_{OL}$	vs Output sink current	1-6	2-6	3-6	5
Output sink current	I <sub>O SINK</sub>	vs Ambient temperature	1-7	2-7	3-7	6
Input offset voltage	V <sub>IO</sub>	Distribution	1-8	2-8	3-8	1
		vs Supply voltage	1-9	2-9	3-9	
		vs Ambient temperature	1-10	2-10	3-10	
Common mode input voltage range	V <sub>CM</sub>	vs Ambient temperature	1-11	2-11	3-11	7
Power supply rejection ratio	PSRR	vs Frequency	1-12	2-12	3-12	1
Common mode rejection ratio	CMRR	vs Frequency	1-13	2-13	3-13	7
Voltage gain & phase angle	A <sub>V</sub>	vs Frequency	1-14	2-14	3-14	10
Input bias current	I <sub>IB</sub>	vs Ambient temperature	1-15	2-15	3-15	3
		vs Input voltage	1-16	2-16	3-16	
Slew Rate (rising)	SRr	vs Ambient temperature	1-17	2-17	3-17	9
Slew Rate (falling)	SRf	vs Ambient temperature	1-18	2-18	3-18	]
Slew rate		Large signal transient response	1-19	2-19	3-19	
		Small signal transient response	1-20	2-20	3-20	
Total harmonic distortion +	(0 dB)	vs. Output voltage p-p	_	2-21	3-21	8
noise	(40 dB)	vs. Output voltage p-p	_	2-22	3-22	]
Maximum p-p output voltage		vs Frequency	1-21	2-23	3-23	
Voltage noise density		vs Frequency	1-22	2-24	3-24	

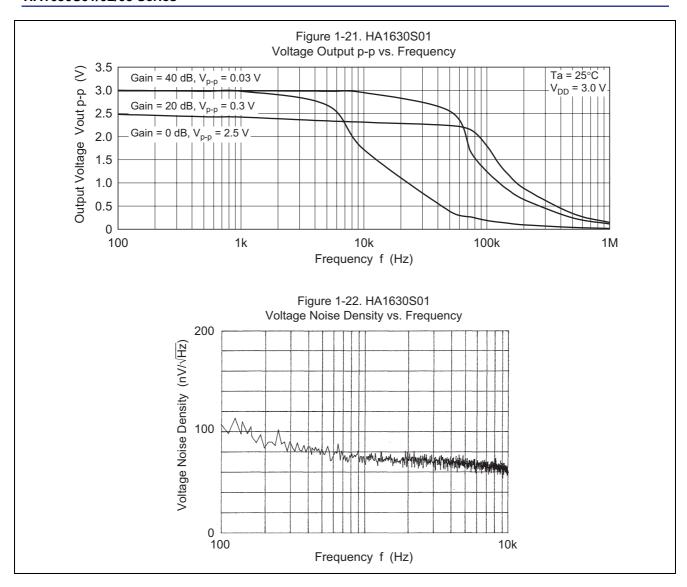
### **Main Characteristics (HA1630S01)**



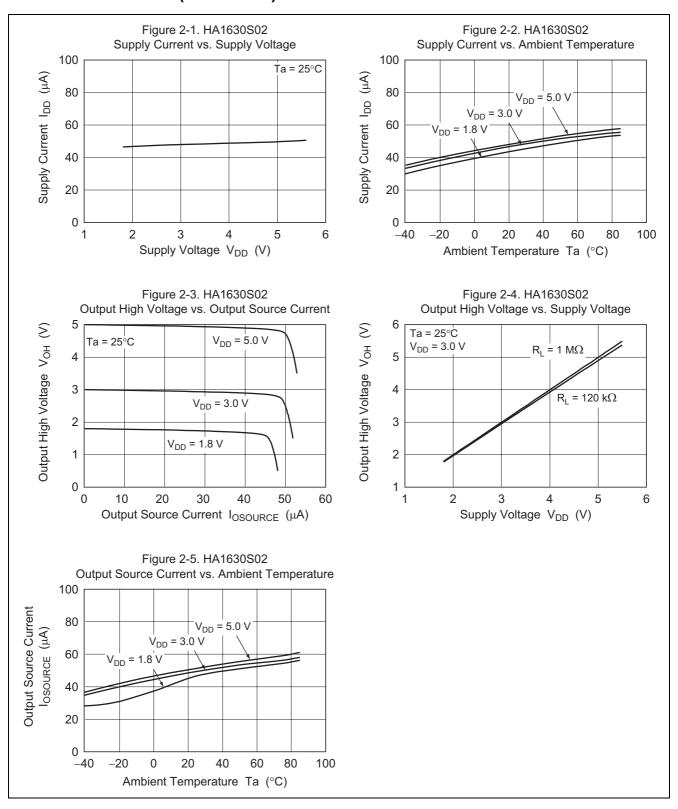


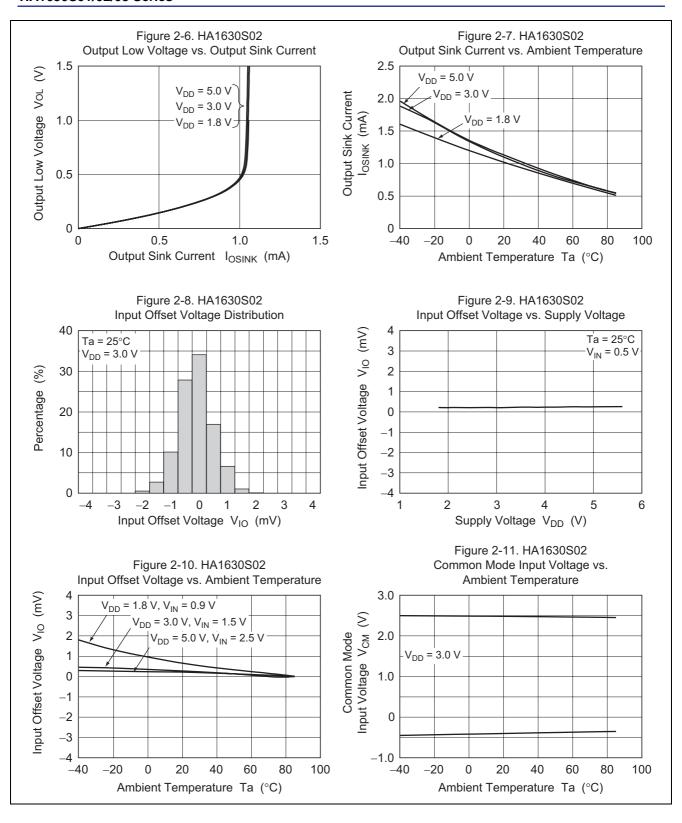


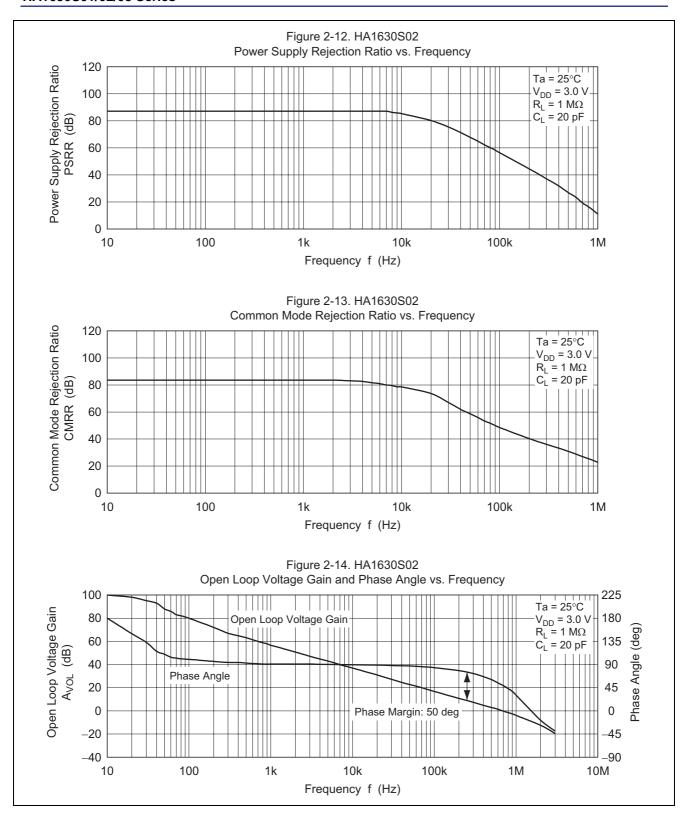


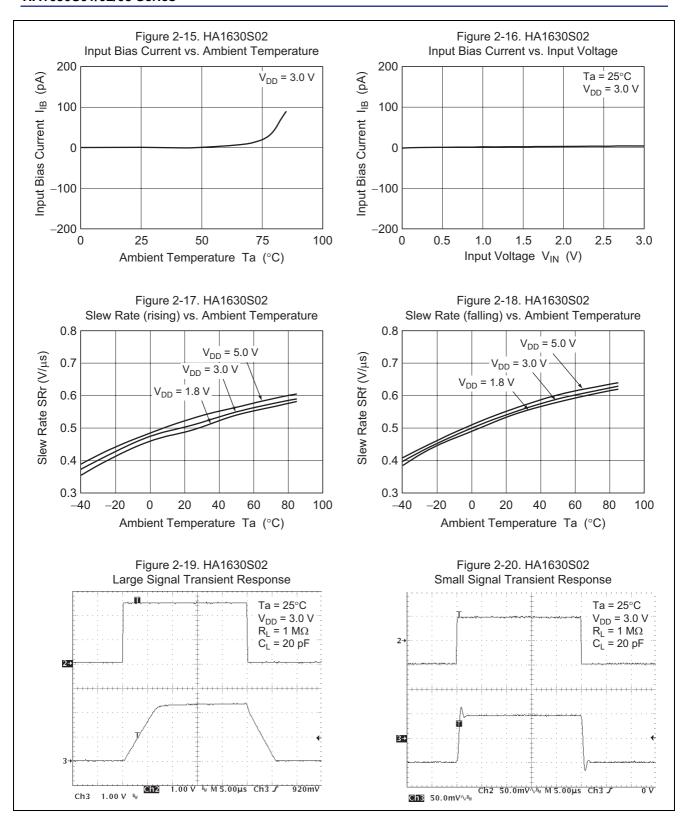


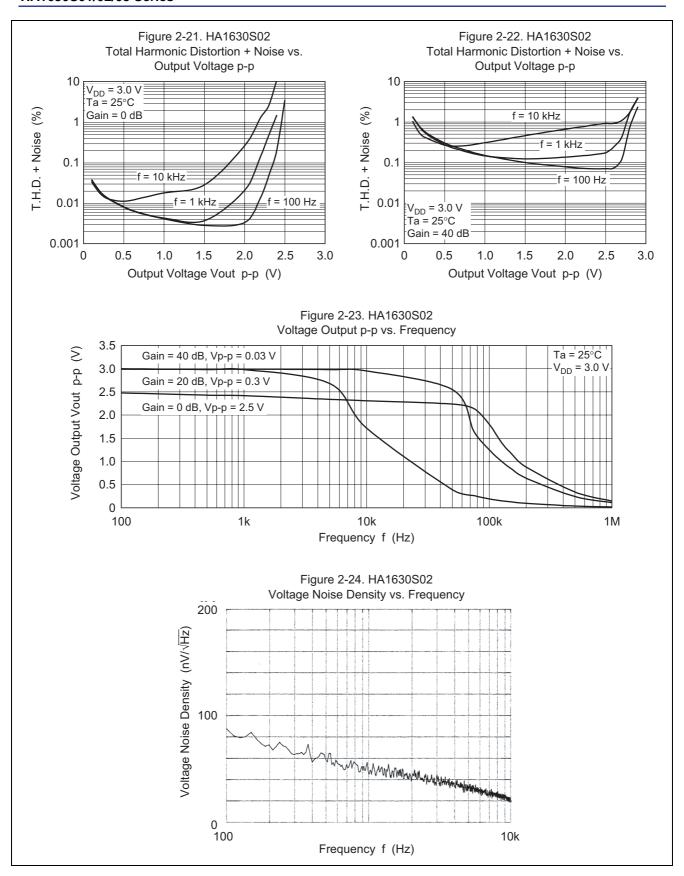
#### Main Characteristics (HA1630S02)



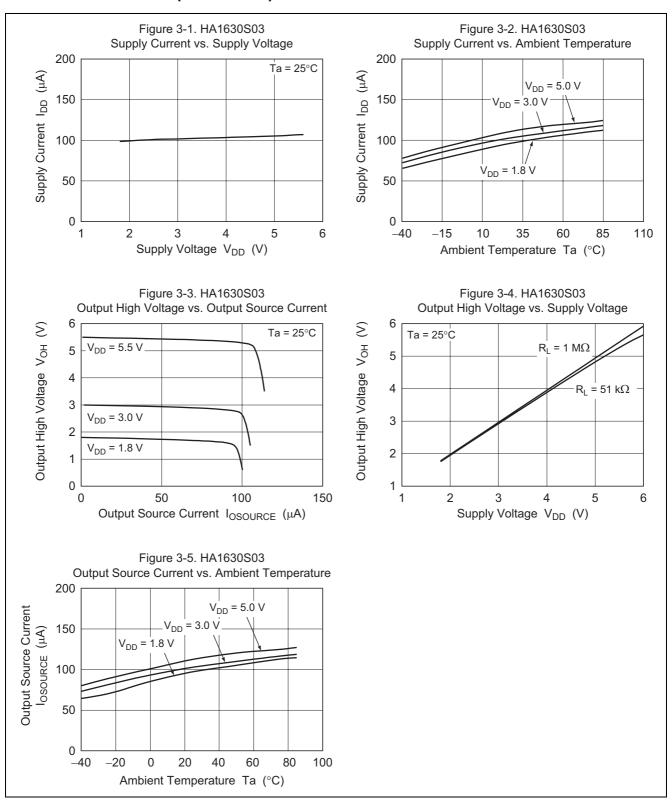


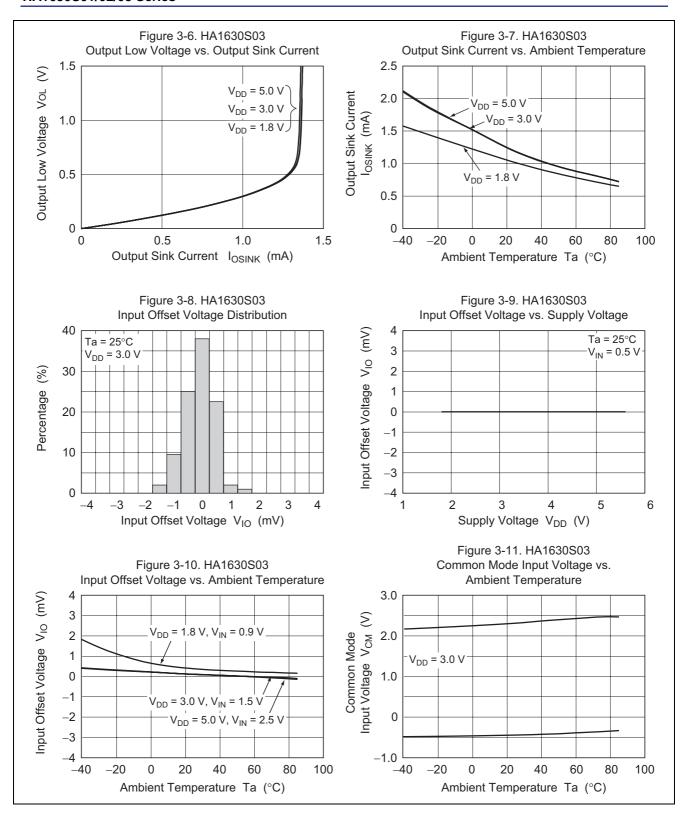


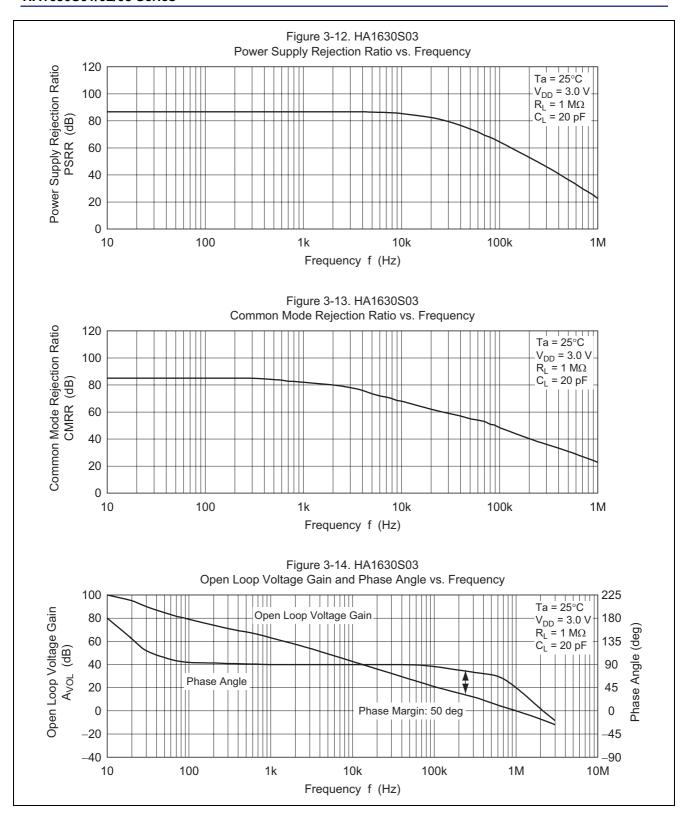


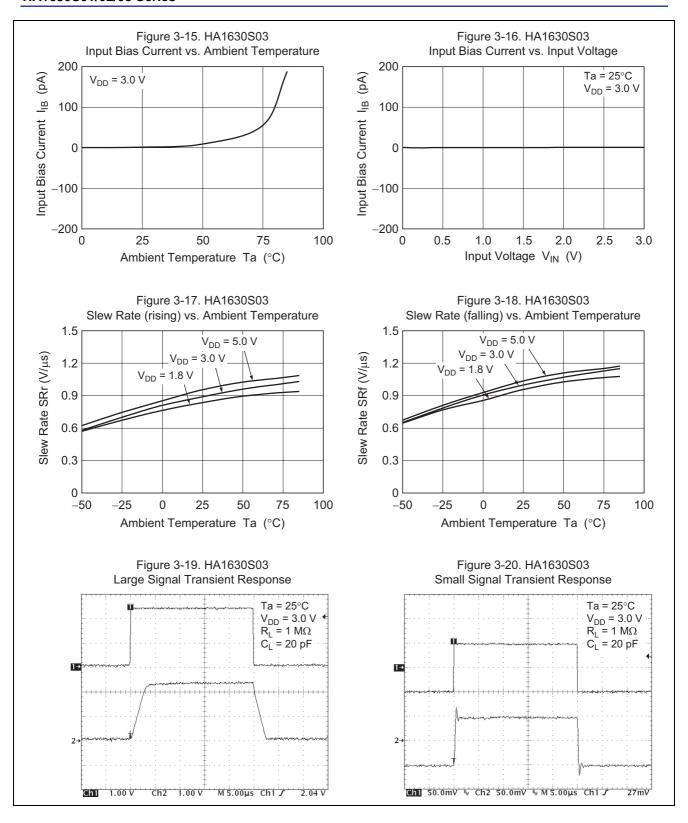


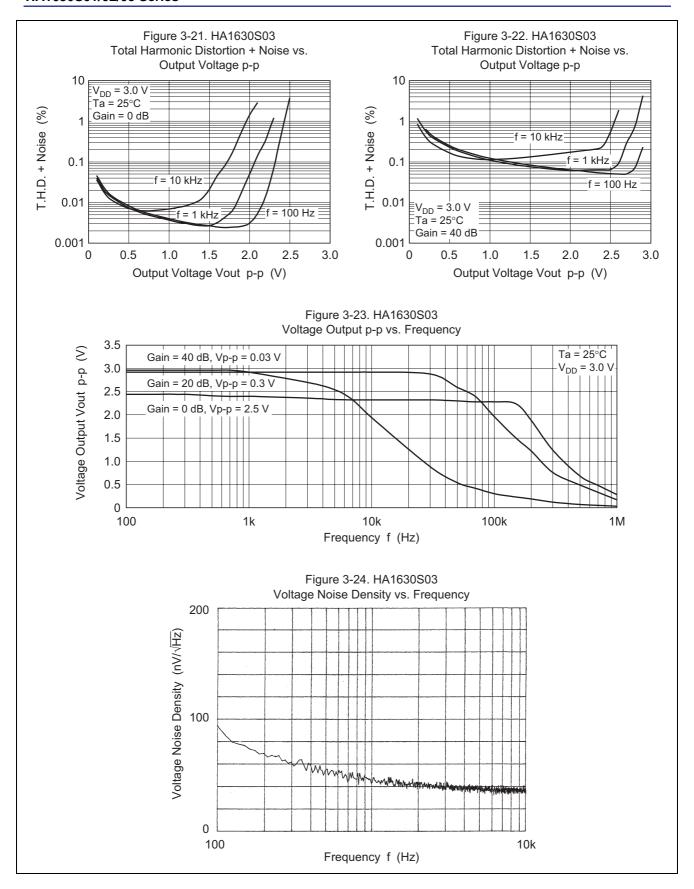
#### Main Characteristics (HA1630S03)





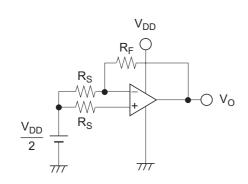






#### **Test Circuits**

1. Power Supply Rejection Ratio, PSRP & Voltage Offset,  $V_{IO}$ 



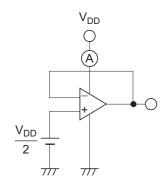
$$\frac{V_{IO}}{V_{IO}} = \left(V_O - \frac{V_{DD}}{2}\right) \times \frac{R_S}{R_S + R_F}$$

**PSRR** 

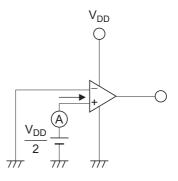
$$PSRR = -20log \left( \left| \frac{V_{O1} - V_{O2}}{V_{DD1} - V_{DD2}} \right| \times \frac{R_S}{R_S + R_F} \right)$$

Measure  $V_O$  corresponding to  $V_{DD1}$  = 1.8 V and  $V_{DD2}$  = 5.5 V

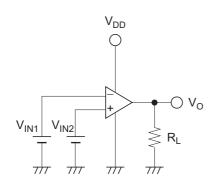
2. Supply Current, I<sub>DD</sub>



3. Input Bias Current, I<sub>IB</sub>



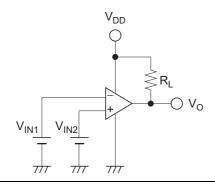
4. Output High Voltage,  $V_{OH}$ 



$$V_{\mathsf{OH}}$$

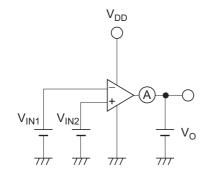
$$R_L = 1 \text{ M}\Omega$$
  
 $V_{IN1} = V_{DD} / 2 - 0.05 \text{ V}$   
 $V_{IN2} = V_{DD} / 2 + 0.05 \text{ V}$ 

5. Output Low Voltage, V<sub>OL</sub>



$$\begin{split} & \frac{V_{OL}}{R_L = 1 \text{ M}\Omega} \\ & V_{IN1} = V_{DD} \, / \, 2 + 0.05 \text{ V} \\ & V_{IN2} = V_{DD} \, / \, 2 - 0.05 \text{ V} \end{split}$$

6. Output Source Current, IOSOURCE & Output Sink Current, IOSINK

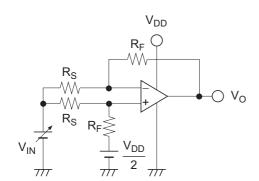


$$V_O = V_{DD} - 0.5 \text{ V}$$
  
 $V_{IN1} = V_{DD} / 2 - 0.05 \text{ V}$   
 $V_{IN2} = V_{DD} / 2 + 0.05 \text{ V}$ 

#### I<sub>OSINK</sub>

$$V_O = + 0.5 \text{ V}$$
  
 $V_{IN1} = V_{DD} / 2 + 0.05 \text{ V}$   
 $V_{IN2} = V_{DD} / 2 - 0.05 \text{ V}$ 

7. Common Mode Input Voltage,  $V_{CM}$  & Common Mode Rejection Ratio, CMRR

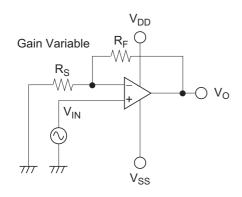


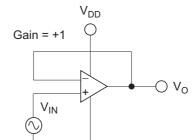
#### CMRR

CMRR = 
$$-20\log\left(\left|\frac{V_{O1} - V_{O2}}{V_{IN1} - V_{IN2}}\right| \times \frac{R_S}{R_S + R_F}\right)$$

Measure  $V_0$  corresponding to  $V_{IN1}$  = 0 V and  $V_{IN2}$  = 2.1 V

8. Total Harmonic Distortion, THD

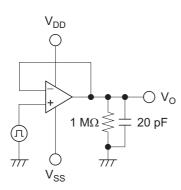




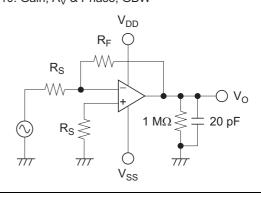
 $V_{SS}$ 

 $\frac{\text{THD}}{\text{Gain Variable}}$   $1 + R_F / R_S = 100$  freq = 100 Hz, 1 kHz, 10 kHz

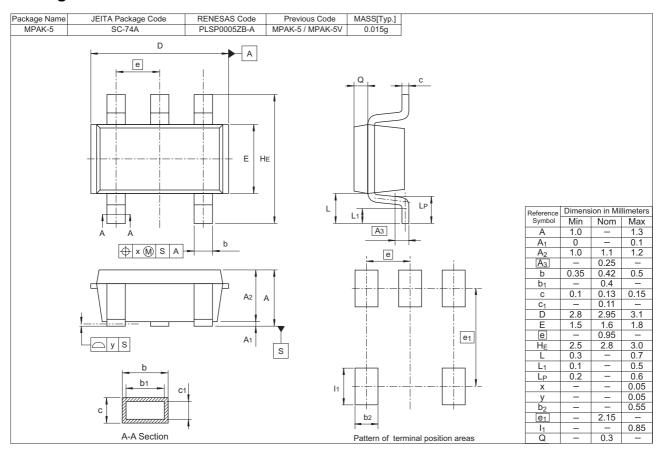
9. Slew Rate, SR

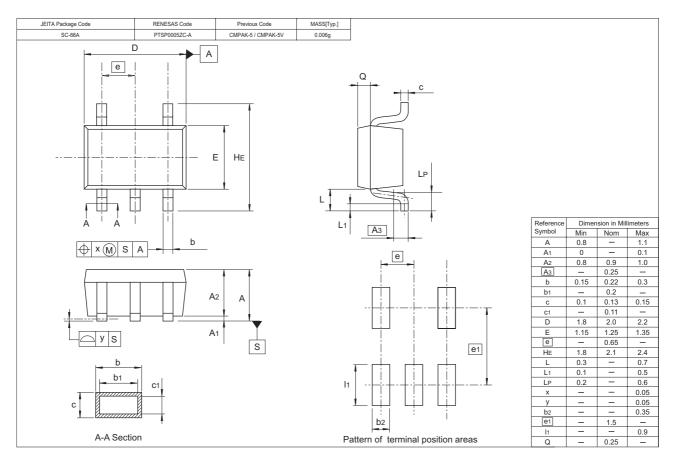


10. Gain, A<sub>V</sub> & Phase, GBW

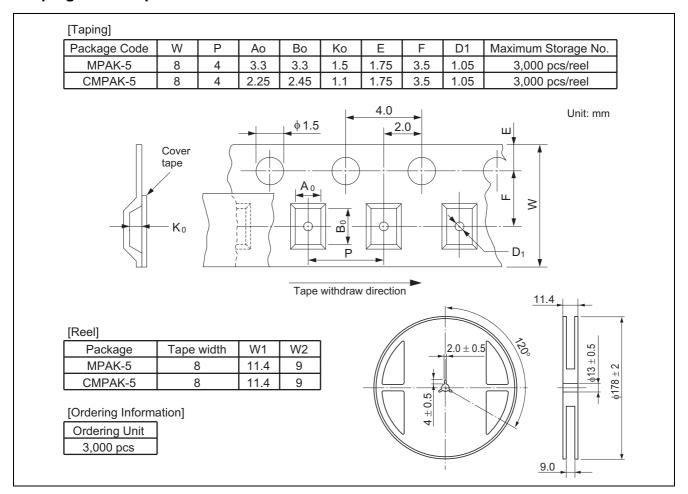


#### **Package Dimensions**

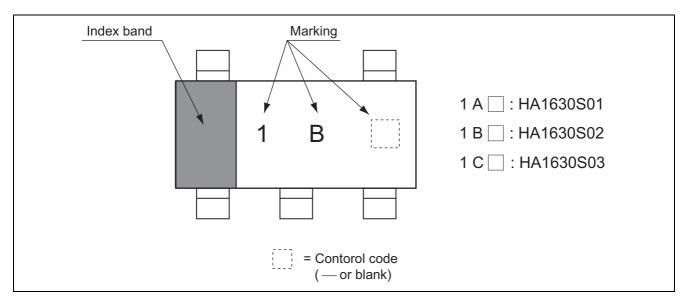




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**Renesas Technology America, Inc.** 450 Holger Way, San Jose, CA 95134-1368, U.S.A Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology (Shanghai) Co., Ltd.
Unit 204, 205, AZIACenter, No.1233 Lujiazui Ring Rd, Pudong District, Shanghai, China 200120 Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7898

Renesas Technology Hong Kong Ltd.
7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong Tel: <852> 2265-6688, Fax: <852> 2730-6071

**Renesas Technology Taiwan Co., Ltd.**10th Floor, No.99, Fushing North Road, Taipei, Taiwan Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology Singapore Pte. Ltd.
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632 Tel: <65> 6213-0200, Fax: <65> 6278-8001

**Renesas Technology Korea Co., Ltd.**Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

Renesas Technology Malaysia Sdn. Bhd
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia Tel: <603> 7955-9390, Fax: <603> 7955-9510

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