



20-MHz, Low-Noise, 1.8-V, RRI/O, CMOS Operational Amplifier with Shutdown

Check for Samples: [OPA322](#), [OPA322S](#), [OPA2322](#), [OPA2322S](#), [OPA4322](#), [OPA4322S](#)

FEATURES

- **Gain Bandwidth:** 20 MHz
- **Low Noise:** 8.5 nV/ $\sqrt{\text{Hz}}$ at 1 kHz
- **Slew Rate:** 10 V/ μs
- **Low THD+N:** 0.0005%
- **Rail-to-Rail I/O**
- **Offset Voltage:** 2 mV (max)
- **Supply Voltage:** 1.8 V to 5.5 V
- **Supply Current:** 1.5 mA/ch
 - Shutdown: 0.1 μA /ch
- **Unity-Gain Stable**
- **Small Packages:**
 - SOT23, DFN, MSOP, TSSOP

APPLICATIONS

- **Sensor Signal Conditioning**
- **Consumer Audio**
- **Multi-Pole Active Filters**
- **Control-Loop Amplifiers**
- **Communications**
- **Security**
- **Scanners**

DESCRIPTION

The OPA322 series consists of single, dual, and quad-channel CMOS operational amplifiers featuring low noise and rail-to-rail inputs/outputs optimized for low-power, single-supply applications. Specified over a wide supply range of 1.8 V to 5.5 V, the low quiescent current of only 1.5 mA per channel makes these devices well-suited for power-sensitive applications.

The combination of very low noise (8.5 nV/ $\sqrt{\text{Hz}}$ at 1 kHz), high gain-bandwidth (20 MHz), and fast slew rate (10 V/ μs) make the OPA322 family ideal for a wide range of applications, including signal conditioning and sensor amplification requiring high gains. Featuring low THD+N, the OPA322 series is also excellent for consumer audio applications, particularly for single-supply systems.

The OPAx322S models include a shutdown mode allowing the amplifiers to be switched from normal operation to a standby current that is typically less than 0.1 μA .

The OPA322 (single version) is available in SOT23-5 and SOT23-6, while the OPA2322 (dual version) is offered in MSOP-8, MSOP-10, SO-8, and DFN-8 packages. The quad versions OPA4322 come in TSSOP-14 and TSSOP-16 packages. All versions are specified for operation from -40°C to $+125^{\circ}\text{C}$.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION⁽¹⁾

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
OPA322	SOT23-5	DBV	RAD
OPA322S	SOT23-6	DBV	RAF
OPA2322	SO-8	D	O2322A
	MSOP-8	DGK	OOZI
	DFN-8	DRG	OPCI
OPA2322S	MSOP-10	DGS	OPBI
OPA4322	TSSOP-14	PW	O4322
OPA4322S	TSSOP-16	PW	O4322SA

- (1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Over operating free-air temperature range, unless otherwise noted.

		OPA322, OPA322S, OPA2322, OPA2322S, OPA4322, OPA4322S	UNIT
Supply voltage, $V_S = (V+) - (V-)$		6	V
Signal input pins	Voltage ⁽²⁾	$(V-) - 0.5$ to $(V+) + 0.5$	V
	Current ⁽²⁾	± 10	mA
Output short-circuit current ⁽³⁾		Continuous	mA
Operating temperature, T_A		-40 to $+150$	$^{\circ}\text{C}$
Storage temperature, T_{stg}		-65 to $+150$	$^{\circ}\text{C}$
Junction temperature, T_J		$+150$	$^{\circ}\text{C}$
ESD ratings	Human body model (HBM)	4000	V
	Charged device model (CDM)	1000	V
	Machine model (MM)	200	V

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
- (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails should be current limited to 10 mA or less.
- (3) Short-circuit to ground, one amplifier per package.

ELECTRICAL CHARACTERISTICS: $V_S = +1.8\text{ V}$ to $+5.5\text{ V}$, or $\pm 0.9\text{ V}$ to $\pm 2.75\text{ V}$
Boldface limits apply over the specified temperature range, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$.

At $T_A = +25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ connected to $V_S/2$, $V_{CM} = V_S/2$, $V_{OUT} = V_S/2$, and $\text{SHDN}_x = V_S$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	OPA322, OPA322S, OPA2322, OPA2322S, OPA4322, OPA4322S			UNIT
			MIN	TYP	MAX	
OFFSET VOLTAGE						
Input offset voltage	V _{OS}			0.5	2	mV
vs Temperature	dV _{OS} /dT	V _S = +5.5 V		1.8	6	μV/°C
vs Power supply	PSR	V _S = +1.8 V to +5.5 V		10	50	μV/V
Over temperature		V _S = +1.8 V to +5.5 V		20	65	μV/V
Channel separation		At 1 kHz		130		dB
INPUT VOLTAGE						
Common-mode voltage range	V _{CM}		(V−) − 0.1		(V+) + 0.1	V
Common-mode rejection ratio	CMRR	(V−) − 0.1 V < V _{CM} < (V+) + 0.1 V	90	100		dB
Over temperature			90			dB
INPUT BIAS CURRENT						
Input bias current	I _B			±0.2	±10	pA
Over temperature		T _A = −40°C to +85°C			±50	pA
		OPA322, OPA322S, T _A = −40°C to +125°C			±800	pA
		OPA2322, OPA2322S, T _A = −40°C to +125°C			±400	pA
		OPA4322, OPA4322S, T _A = −40°C to +125°C			±400	pA
Input offset current	I _{OS}			±0.2	±10	pA
Over temperature		T _A = −40°C to +85°C			±50	pA
		T _A = −40°C to +125°C			±400	pA
NOISE						
Input voltage noise		f = 0.1 Hz to 10 Hz		2.8		μV _{PP}
Input voltage noise density	e _n	f = 1 kHz		8.5		nV/√Hz
		f = 10 kHz		7		nV/√Hz
Input current noise density	i _n	f = 1 kHz		0.6		fA/√Hz
INPUT CAPACITANCE						
Differential				5		pF
Common-mode				4		pF
OPEN-LOOP GAIN						
Open-loop voltage gain	A _{OL}	0.1 V < V _O < (V+) − 0.1 V, R _L = 10 kΩ	100	130		dB
		0.1 V < V _O < (V+) − 0.1 V, R _L = 10 kΩ	94			dB
Phase margin	PM	V _S = 5 V, C _L = 50 pF		47		Degrees
FREQUENCY RESPONSE						
V _S = 5.0 V, C _L = 50 pF						
Gain bandwidth product	GBP	Unity gain		20		MHz
Slew rate	SR	G = +1		10		V/μs
Settling time	t _S	To 0.1%, 2-V step, G = +1		0.25		μs
		To 0.01%, 2-V step, G = +1		0.32		μs
Overload recovery time		V _{IN} × G > V _S		100		ns
Total harmonic distortion + noise ⁽¹⁾	THD+N	V _O = 4 V _{PP} , G = +1, f = 10 kHz, R _L = 10 kΩ		0.0005		%
		V _O = 2 V _{PP} , G = +1, f = 10 kHz, R _L = 600 Ω		0.0011		%

(1) Third-order filter; bandwidth = 80 kHz at -3 dB .

ELECTRICAL CHARACTERISTICS: $V_S = +1.8\text{ V to }+5.5\text{ V}$, or $\pm 0.9\text{ V to } \pm 2.75\text{ V}$ (continued)

Boldface limits apply over the specified temperature range, $T_A = -40^\circ\text{C to }+125^\circ\text{C}$.

At $T_A = +25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ connected to $V_S/2$, $V_{CM} = V_S/2$, $V_{OUT} = V_S/2$, and $\overline{\text{SHDN}}_X = V_{S+}$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	OPA322, OPA322S, OPA2322, OPA2322S, OPA4322, OPA4322S			UNIT	
		MIN	TYP	MAX		
OUTPUT						
Voltage output swing from both rails	V_O	$R_L = 10\text{ k}\Omega$		10	20	mV
Over temperature		$R_L = 10\text{ k}\Omega$			30	mV
Short-circuit current	I_{SC}	$V_S = 5.5\text{ V}$		± 65		mA
Capacitive load drive	C_L		See Typical Characteristics			
Open-loop output resistance	R_O	$I_O = 0\text{ mA}$, $f = 1\text{ MHz}$		90		Ω
POWER SUPPLY						
Specified voltage range	V_S		1.8		5.5	V
Quiescent current per amplifier	I_Q	$I_O = 0\text{ mA}$, $V_S = +5.5\text{ V}$				
OPA322, OPA322S		$I_O = 0\text{ mA}$, $V_S = +5.5\text{ V}$		1.6	1.9	mA
Over temperature		$I_O = 0\text{ mA}$, $V_S = +5.5\text{ V}$			2	mA
OPA2322, OPA2322S		$I_O = 0\text{ mA}$, $V_S = +5.5\text{ V}$		1.5	1.75	mA
Over temperature		$I_O = 0\text{ mA}$, $V_S = +5.5\text{ V}$			1.85	mA
OPA4322, OPA4322S		$I_O = 0\text{ mA}$, $V_S = +5.5\text{ V}$		1.4	1.65	mA
Over temperature		$I_O = 0\text{ mA}$, $V_S = +5.5\text{ V}$			1.75	mA
Power-on time		$V_{S+} = 0\text{ V}$ to 5 V , to 90% I_Q level		28		μs
SHUTDOWN ⁽²⁾ $V_S = 1.8\text{ V}$ to 5.5 V						
Quiescent current, per amplifier	I_{QSD}	All amplifiers disabled, $\overline{\text{SHDN}} = V_{S-}$		0.1	0.5	μA
High voltage (enabled)	V_{IH}	Amplifier enabled	$(V+) - 0.1$			V
Low voltage (disabled)	V_{IL}	Amplifier disabled			$(V-) + 0.1$	V
Amplifier enable time (full shutdown) ⁽³⁾	t_{ON}	Full shutdown; $G = 1$, $V_{OUT} = 0.9 \times V_S/2$ ⁽⁴⁾		10		μs
Amplifier enable time (partial shutdown) ⁽³⁾	t_{ON}	Partial shutdown; $G = 1$, $V_{OUT} = 0.9 \times V_S/2$ ⁽⁴⁾		6		μs
Amplifier disable time ⁽³⁾	t_{OFF}	$G = 1$, $V_{OUT} = 0.1 \times V_S/2$		3		μs
$\overline{\text{SHDN}}$ pin input bias current (per pin)		$V_{IH} = 5.0\text{ V}$		0.13		μA
		$V_{IL} = 0\text{ V}$		0.04		μA
TEMPERATURE						
Specified range			-40		+125	$^{\circ}\text{C}$
Operating range			-40		+150	$^{\circ}\text{C}$

(2) Ensured by design and characterization; not production tested.

(3) Disable time (t_{OFF}) and enable time (t_{ON}) are defined as the time interval between the 50% point of the signal applied to the $\overline{\text{SHDN}}$ pin and the point at which the output voltage reaches the 10% (disable) or 90% (enable) level.

(4) Full shutdown refers to the dual OPA2322S having both channels A and B disabled ($\overline{\text{SHDN}}_A = \overline{\text{SHDN}}_B = V_{S-}$) and the quad OPA4322S having all channels A to D disabled ($\overline{\text{SHDN}}_{A/B} = \overline{\text{SHDN}}_{C/D} = V_{S-}$). For partial shutdown, only one $\overline{\text{SHDN}}$ pin is exercised; in this mode, the internal biasing and oscillator remain operational and the enable time is shorter.

THERMAL INFORMATION: OPA322

THERMAL METRIC ⁽¹⁾		OPA322	OPA322S	UNITS
		DBV	DBV	
		5 PINS	6 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	219.3	177.5	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	107.5	108.9	
θ_{JB}	Junction-to-board thermal resistance	57.5	27.4	
ψ_{JT}	Junction-to-top characterization parameter	7.4	13.3	
ψ_{JB}	Junction-to-board characterization parameter	56.9	26.9	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	n/a	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

THERMAL INFORMATION: OPA2322

THERMAL METRIC ⁽¹⁾		OPA2322			OPA2322S	UNITS
		D	DRG	DGK	DGS	
		8 PINS	8 PINS	8 PINS	10 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	122.6	50.6	174.8	171.5	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	67.1	54.9	43.9	43.0	
θ_{JB}	Junction-to-board thermal resistance	64.0	25.2	95.0	91.4	
ψ_{JT}	Junction-to-top characterization parameter	13.2	0.6	2.0	1.9	
ψ_{JB}	Junction-to-board characterization parameter	63.4	25.3	93.5	89.9	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	n/a	5.7	n/a	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

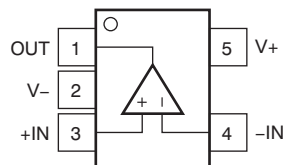
THERMAL INFORMATION: OPA4322

THERMAL METRIC ⁽¹⁾		OPA4322	OPA4322S	UNITS
		PW	PW	
		14 PINS	16 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	109.8	105.9	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	34.9	28.1	
θ_{JB}	Junction-to-board thermal resistance	52.5	51.1	
ψ_{JT}	Junction-to-top characterization parameter	2.2	0.8	
ψ_{JB}	Junction-to-board characterization parameter	51.8	50.4	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	n/a	n/a	

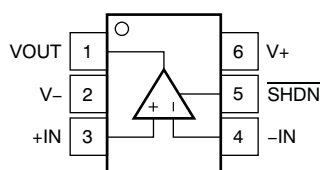
(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

PIN CONFIGURATIONS

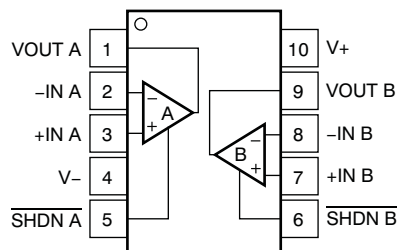
**DBV PACKAGE
SOT23-5
(TOP VIEW)**



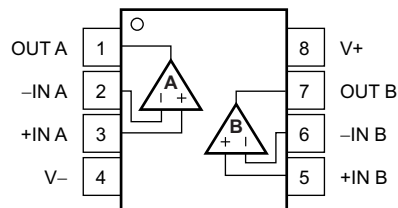
**DBV PACKAGE
SOT23-6
(TOP VIEW)**



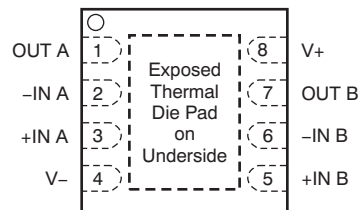
**DGS PACKAGE
MSOP-10
(TOP VIEW)**



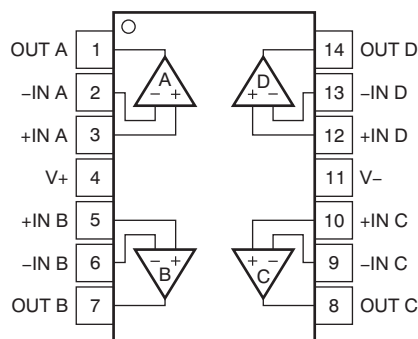
**D, DGK PACKAGES
SO-8, MSOP-8
(TOP VIEW)**



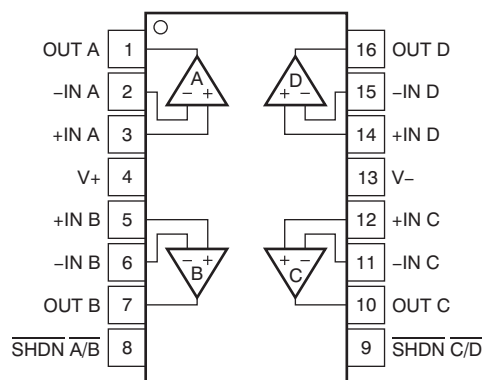
**DRG PACKAGE⁽¹⁾⁽²⁾
DFN-8
(TOP VIEW)**



**PW PACKAGE
TSSOP-14
(TOP VIEW)**



**PW PACKAGE
TSSOP-16
(TOP VIEW)**



- (1) Connect thermal pad to V-.
- (2) Pad size: 2mm × 1.2mm.

TYPICAL CHARACTERISTICS

At $T_A = +25^\circ\text{C}$, $V_{CM} = V_{OUT} = \text{mid-supply}$, and $R_L = 10\text{ k}\Omega$, unless otherwise noted.

OPEN-LOOP GAIN/PHASE vs FREQUENCY

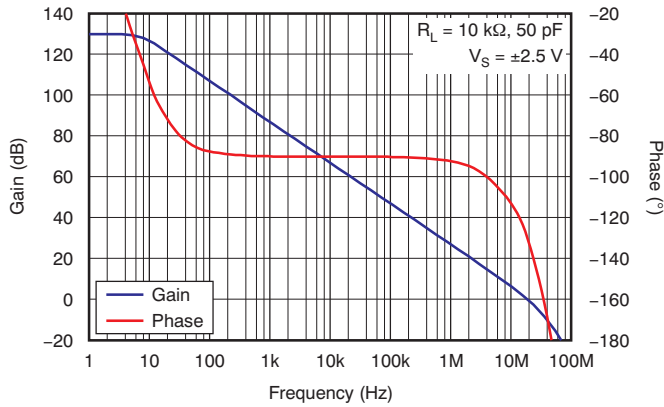


Figure 1.

OPEN-LOOP GAIN vs TEMPERATURE

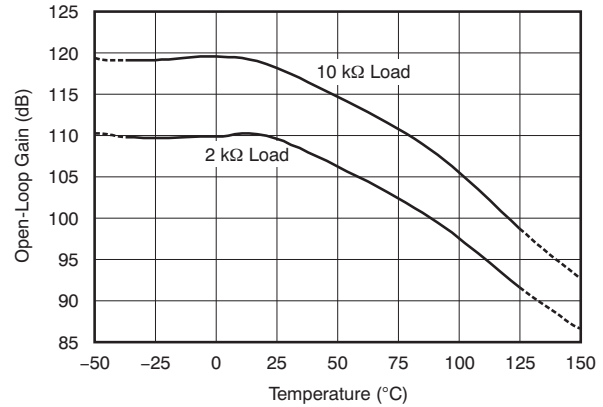


Figure 2.

INPUT BIAS CURRENT vs SUPPLY VOLTAGE

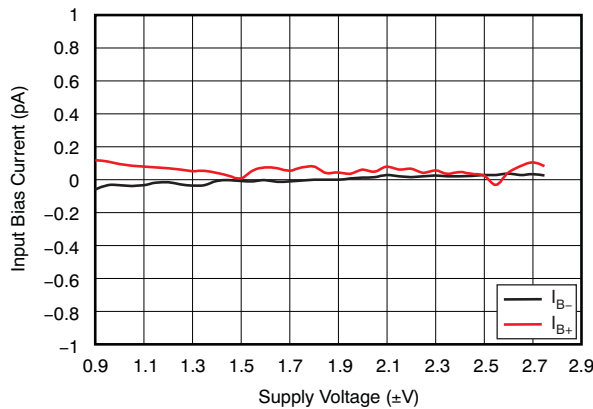


Figure 3.

INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE

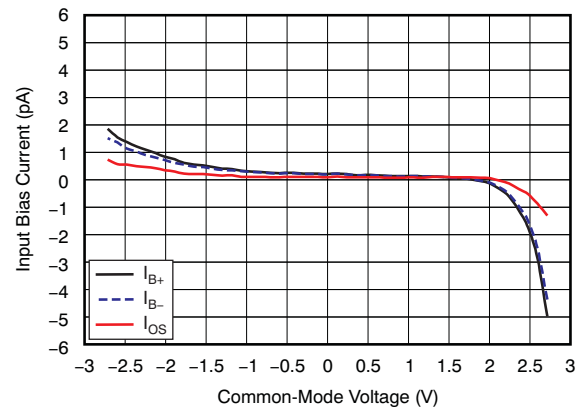


Figure 4.

INPUT BIAS CURRENT vs TEMPERATURE

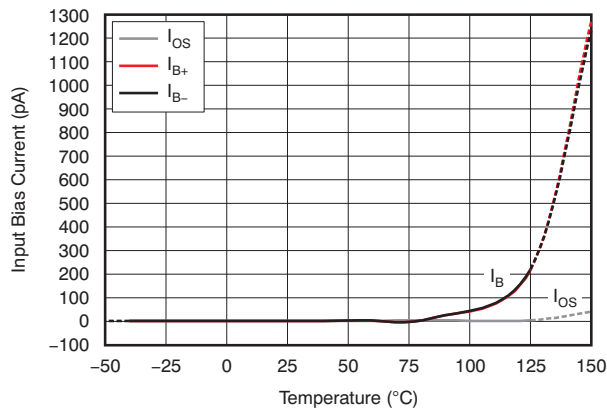


Figure 5.

QUIESCENT CURRENT vs SUPPLY VOLTAGE

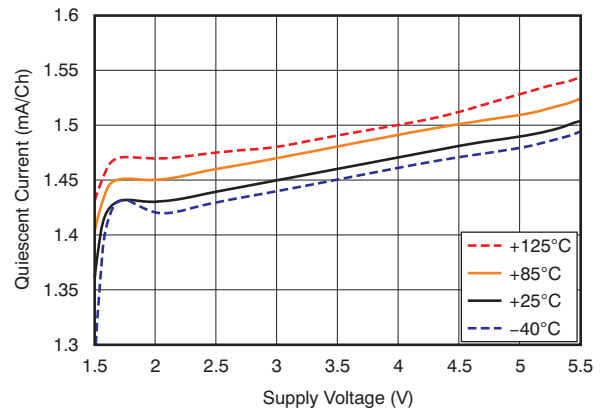


Figure 6.

TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $V_{CM} = V_{OUT} = \text{mid-supply}$, and $R_L = 10\text{ k}\Omega$, unless otherwise noted.

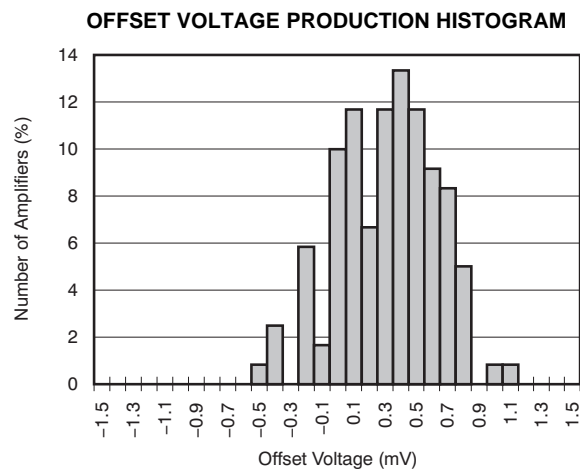


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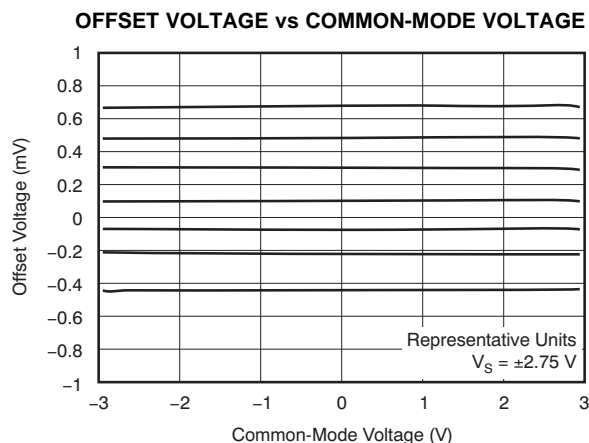


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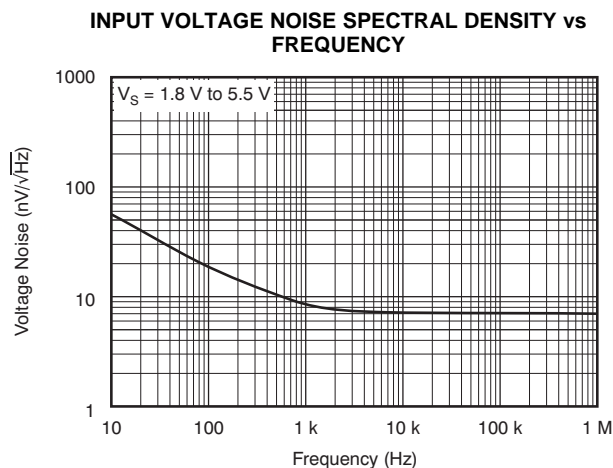


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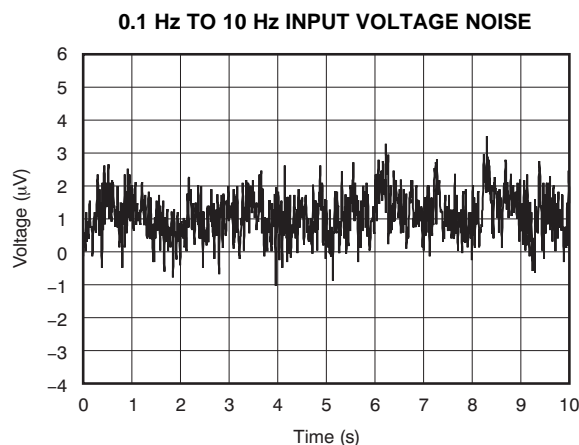


Figure 10.

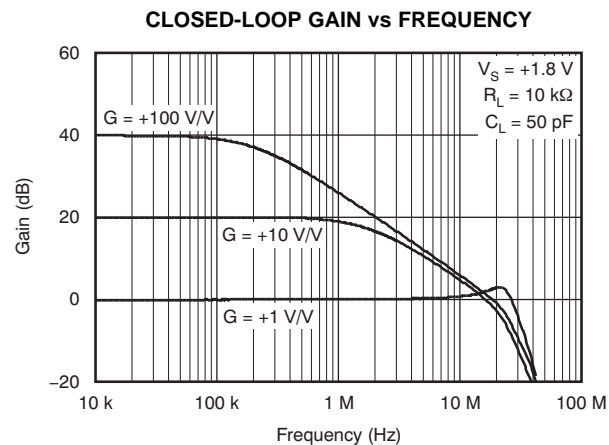


Figure 11.

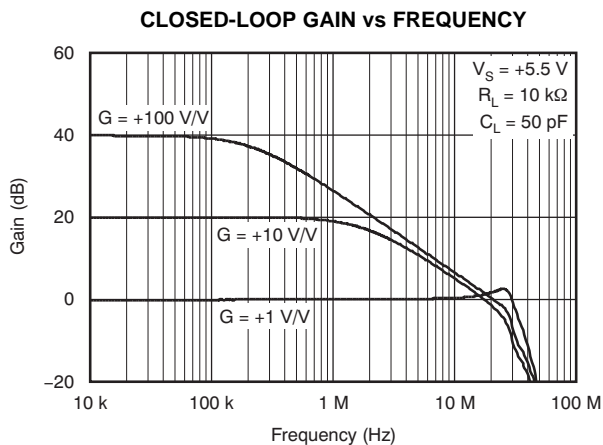


Figure 12.

TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $V_{CM} = V_{OUT} = \text{mid-supply}$, and $R_L = 10\text{ k}\Omega$, unless otherwise noted.

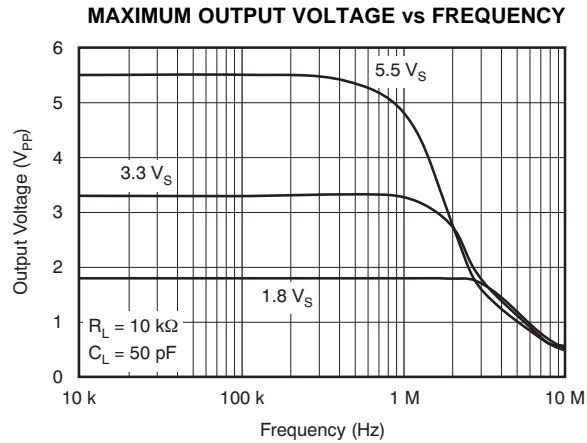


Figure 13.

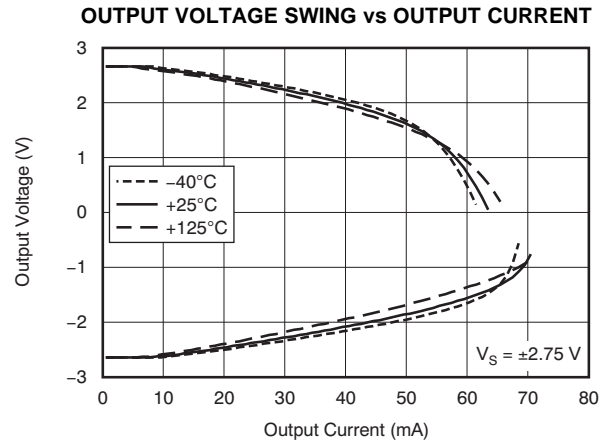


Figure 14.

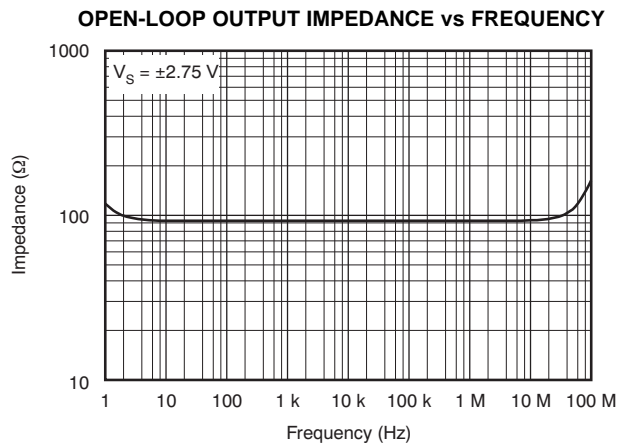


Figure 15.

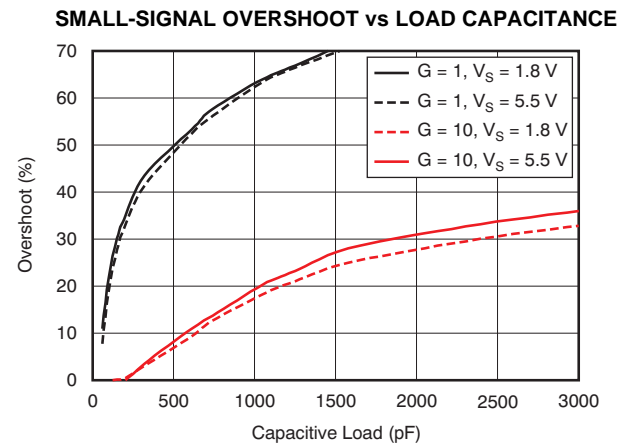


Figure 16.

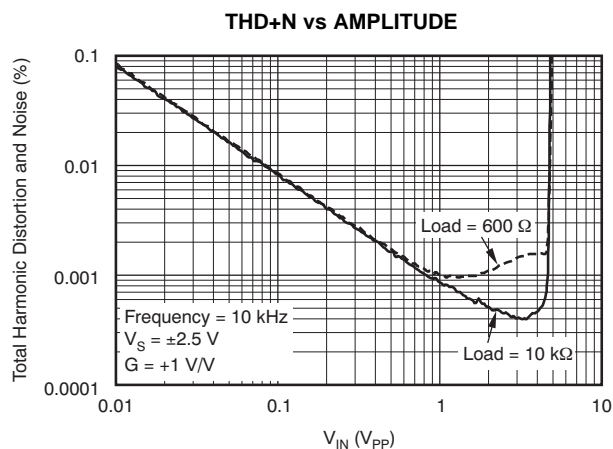


Figure 17.

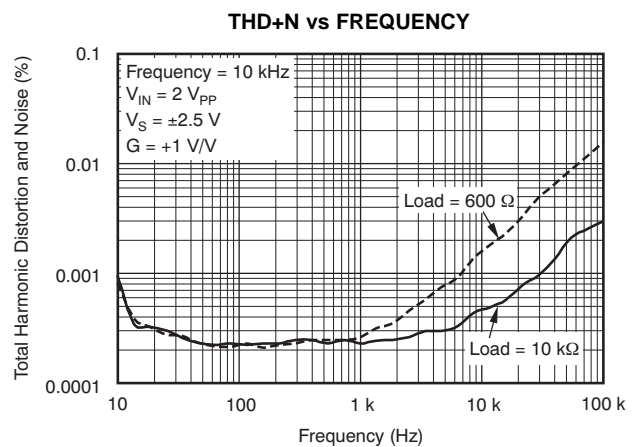


Figure 18.

TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $V_{CM} = V_{OUT} = \text{mid-supply}$, and $R_L = 10\text{ k}\Omega$, unless otherwise noted.

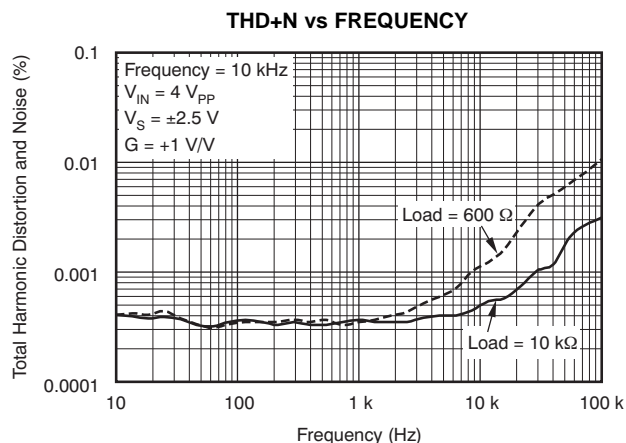


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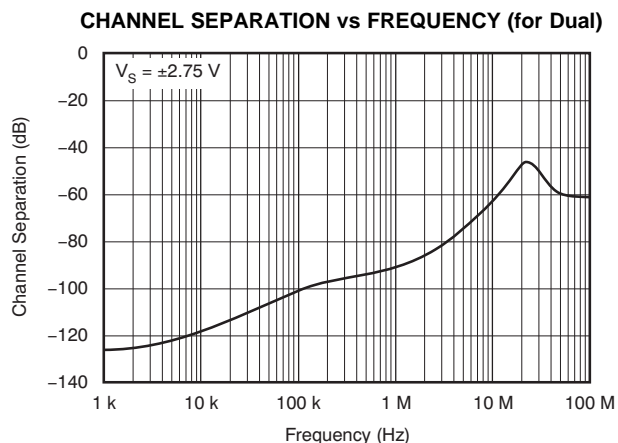


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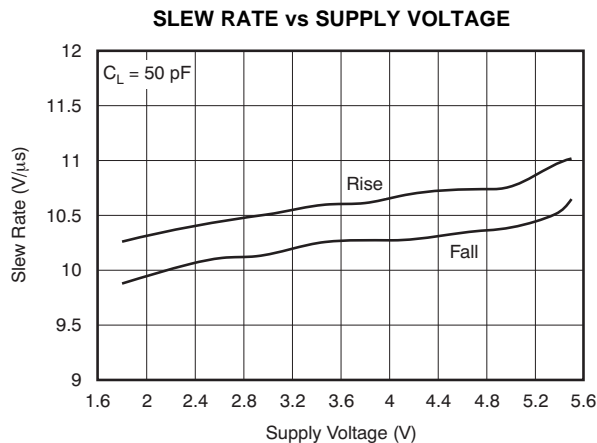


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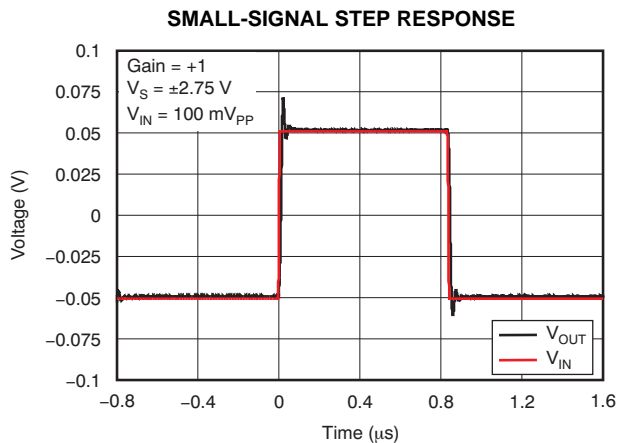


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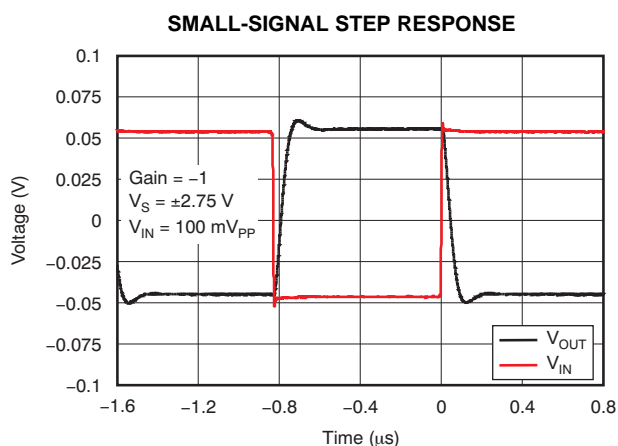


Figure 23.

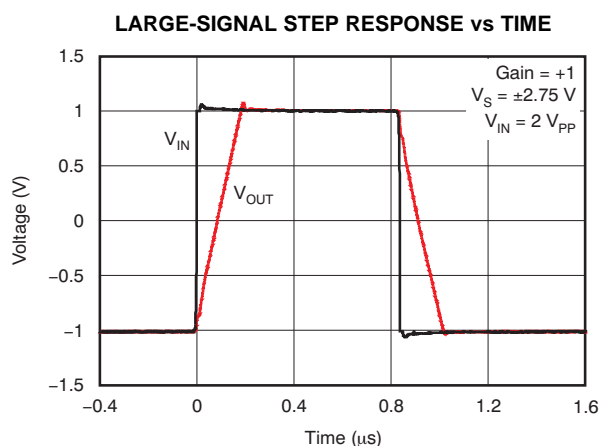


Figure 24.

TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $V_{CM} = V_{OUT} = \text{mid-supply}$, and $R_L = 10\text{ k}\Omega$, unless otherwise noted.

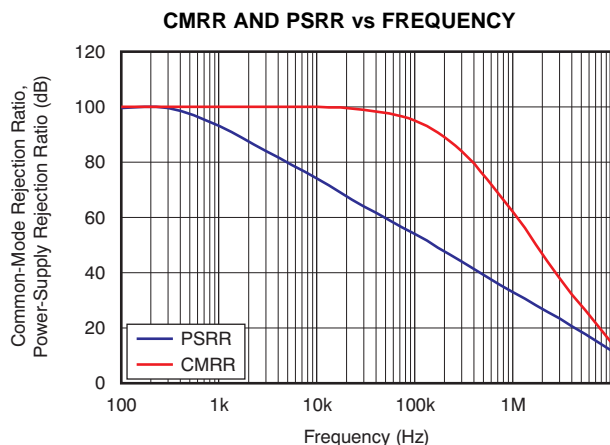


Figure 25.

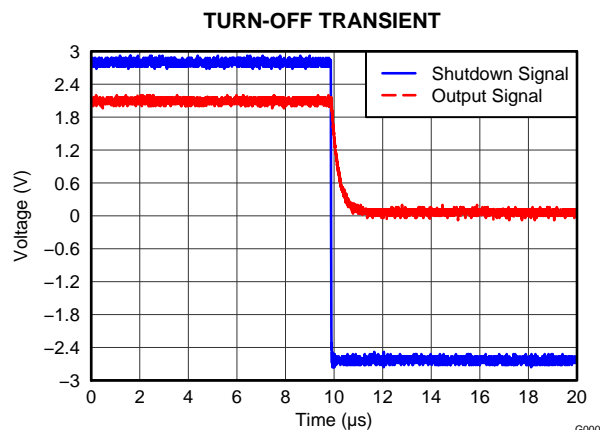


Figure 26.

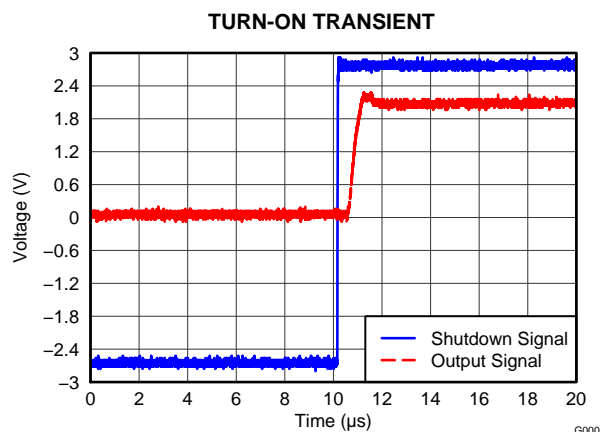


Figure 27.

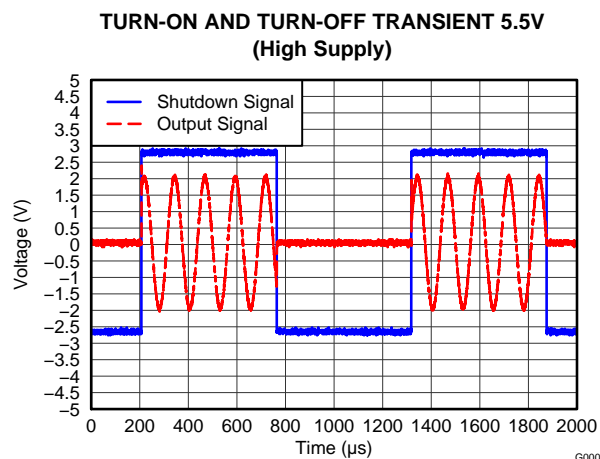


Figure 28.

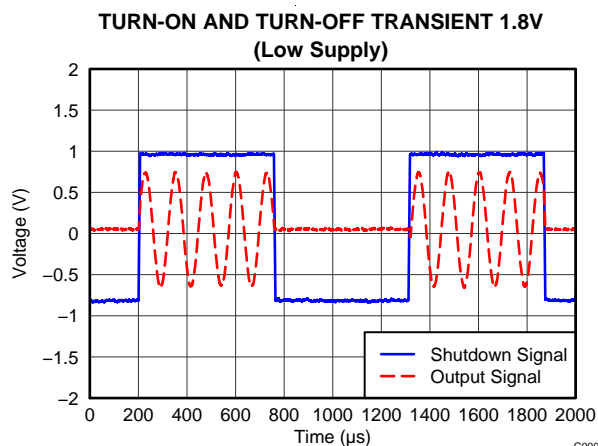


Figure 29.

APPLICATION INFORMATION

OPERATING VOLTAGE

The OPA322 series op amps are unity-gain stable and can operate on a single-supply voltage (1.8 V to 5.5 V), or a split-supply voltage (± 0.9 V to ± 2.75 V), making them highly versatile and easy to use. The power-supply pins should have local bypass ceramic capacitors (typically 0.001 μ F to 0.1 μ F). These amplifiers are fully specified from +1.8 V to +5.5 V and over the extended temperature range of -40°C to $+125^{\circ}\text{C}$. Parameters that can exhibit variance with regard to operating voltage or temperature are presented in the [Typical Characteristics](#).

INPUT AND ESD PROTECTION

The OPA322 incorporates internal electrostatic discharge (ESD) protection circuits on all pins. In the case of input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes also provide in-circuit input overdrive protection, as long as the current is limited to 10 mA as stated in the [Absolute Maximum Ratings](#) table. Many input signals are inherently current-limited to less than 10 mA; therefore, a limiting resistor is not required. [Figure 30](#) shows how a series input resistor (R_S) may be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value should be kept to the minimum in noise-sensitive applications.

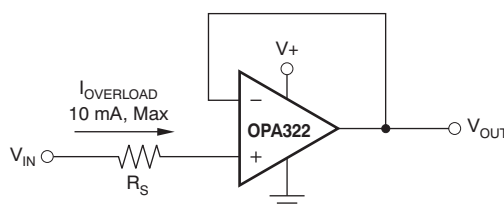


Figure 30. Input Current Protection

PHASE REVERSAL

The OPA322 op amps are designed to be immune to phase reversal when the input pins exceed the supply voltages, therefore providing further in-system stability and predictability. [Figure 31](#) shows the input voltage exceeding the supply voltage without any phase reversal.

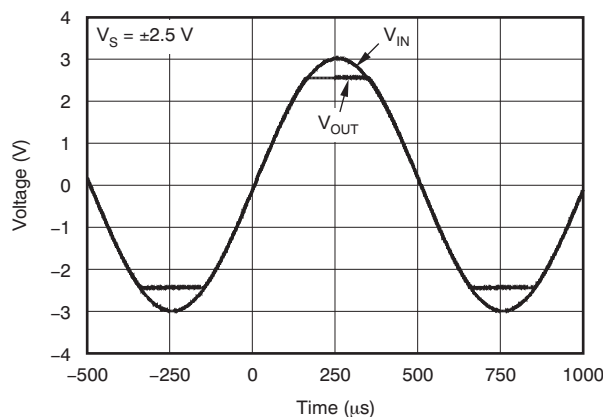
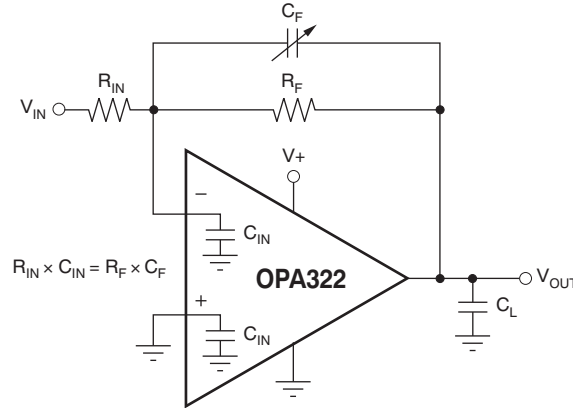


Figure 31. No Phase Reversal

FEEDBACK CAPACITOR IMPROVES RESPONSE

For optimum settling time and stability with high-impedance feedback networks, it may be necessary to add a feedback capacitor across the feedback resistor, R_F , as shown in Figure 32. This capacitor compensates for the zero created by the feedback network impedance and the OPA322 input capacitance (and any parasitic layout capacitance). The effect becomes more significant with higher impedance networks.



NOTE: Where C_{IN} is equal to the OPA322 input capacitance (approximately 9 pF) plus any parasitic layout capacitance.

Figure 32. Feedback Capacitor Improves Dynamic Performance

It is suggested that a variable capacitor be used for the feedback capacitor because input capacitance may vary between op amps and layout capacitance is difficult to determine. For the circuit shown in Figure 32, the value of the variable feedback capacitor should be chosen so that the input resistance times the input capacitance of the OPA322 (typically 9 pF) plus the estimated parasitic layout capacitance equals the feedback capacitor times the feedback resistor:

$$R_{IN} \times C_{IN} = R_F \times C_F$$

Where:

C_{IN} is equal to the OPA322 input capacitance (sum of differential and common-mode) plus the layout capacitance.

The capacitor value can be adjusted until optimum performance is obtained.

EMI SUSCEPTIBILITY AND INPUT FILTERING

Operational amplifiers vary in susceptibility to electromagnetic interference (EMI). If conducted EMI enters the device, the dc offset observed at the amplifier output may shift from the nominal value while EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. While all operational amplifier pin functions can be affected by EMI, the input pins are likely to be the most susceptible. The OPA322 operational amplifier family incorporates an internal input low-pass filter that reduces the amplifier response to EMI. Both common-mode and differential mode filtering are provided by the input filter. The filter is designed for a cutoff frequency of approximately 580 MHz (–3 dB), with a roll-off of 20 dB per decade.

OUTPUT IMPEDANCE

The open-loop output impedance of the OPA322 common-source output stage is approximately 90 Ω . When the op amp is connected with feedback, this value is reduced significantly by the loop gain. For each decade rise in the closed-loop gain, the loop gain is reduced by the same amount, which results in a ten-fold increase in effective output impedance. While the OPA322 output impedance remains very flat over a wide frequency range, at higher frequencies the output impedance rises as the open-loop gain of the op amp drops. However, at these frequencies the output also becomes capacitive as a result of parasitic capacitance. This characteristic, in turn, prevents the output impedance from becoming too high, which can cause stability problems when driving large capacitive loads. As mentioned previously, the OPA322 has excellent capacitive load drive capability for an op amp with its bandwidth.

CAPACITIVE LOAD AND STABILITY

The OPA322 is designed to be used in applications where driving a capacitive load is required. As with all op amps, there may be specific instances where the OPA322 can become unstable. The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier is stable in operation. An op amp in the unity-gain (+1 V/V) buffer configuration and driving a capacitive load exhibits a greater tendency to become unstable than an amplifier operated at a higher noise gain. The capacitive load, in conjunction with the op amp output resistance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases as the capacitive loading increases. When operating in the unity-gain configuration, the OPA322 remains stable with a pure capacitive load up to approximately 1 nF.

The equivalent series resistance (ESR) of some very large capacitors ($C_L > 1 \mu\text{F}$) is sufficient to alter the phase characteristics in the feedback loop such that the amplifier remains stable. Increasing the amplifier closed-loop gain allows the amplifier to drive increasingly larger capacitance. This increased capability is evident when observing the overshoot response of the amplifier at higher voltage gains, as shown in Figure 33. One technique for increasing the capacitive load drive capability of the amplifier operating in unity gain is to insert a small resistor (R_S), typically 10Ω to 20Ω , in series with the output, as shown in Figure 34.

This resistor significantly reduces the overshoot and ringing associated with large capacitive loads. A possible problem with this technique is that a voltage divider is created with the added series resistor and any resistor connected in parallel with the capacitive load. The voltage divider introduces a gain error at the output that reduces the output swing. The error contributed by the voltage divider, however, may be insignificant. For instance, with a load resistance, $R_L = 10 \text{ k}\Omega$ and $R_S = 20 \Omega$, the gain error is only about 0.2%. However, when R_L is decreased to 600Ω , which the OPA322 is able to drive, the error increases to 7.5%.

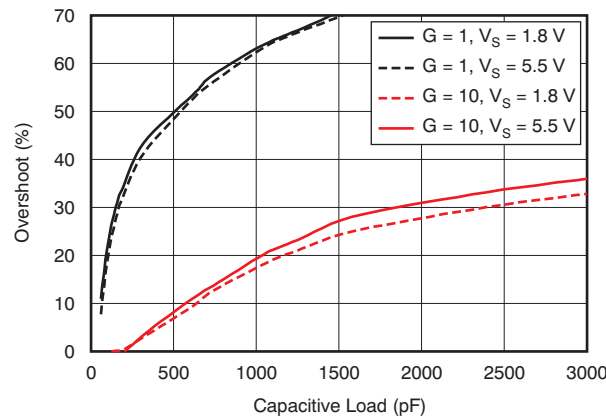


Figure 33. Small-Signal Overshoot versus Capacitive Load (100-mV_{PP} output step)

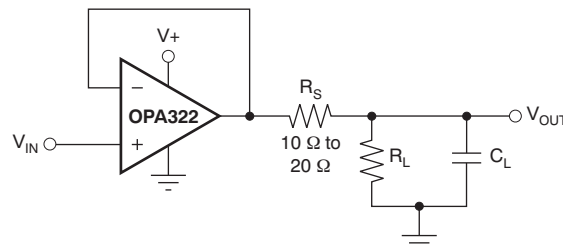


Figure 34. Improving Capacitive Load Drive

OVERLOAD RECOVERY TIME

Overload recovery time is the time required for the output of the amplifier to come out of saturation and recover to the linear region. Overload recovery is particularly important in applications where small signals must be amplified in the presence of large transients. Figure 35 and Figure 36 show the positive and negative overload recovery times of the OPA322, respectively. In both cases, the time elapsed before the OPA322 comes out of saturation is less than 100 ns. In addition, the symmetry between the positive and negative recovery times allows excellent signal rectification without distortion of the output signal.

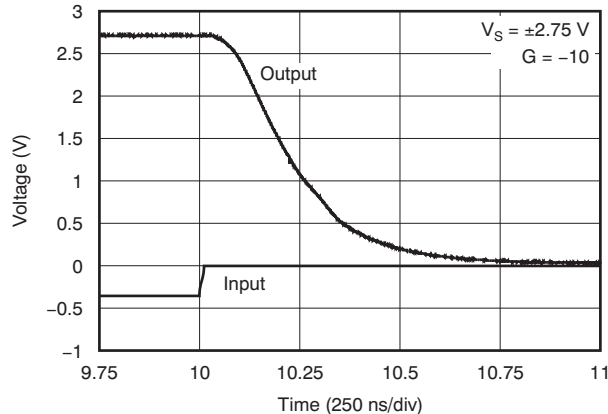


Figure 35. Positive Recovery Time

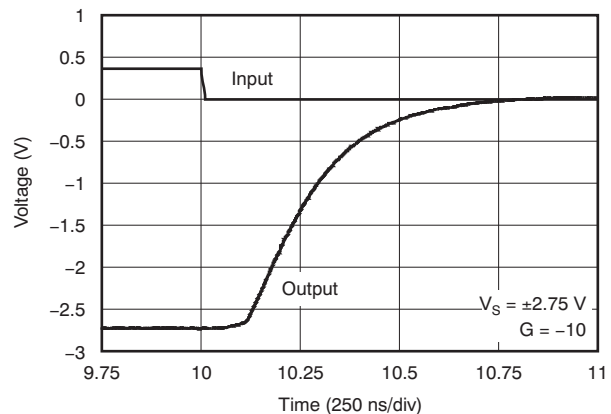


Figure 36. Negative Recovery Time

SHUTDOWN FUNCTION

The SHDN (enable) pin function of the OPAx322S is referenced to the negative supply voltage of the operational amplifier. A logic level high enables the op amp. A valid logic high is defined as voltage $[(V+) - 0.1 \text{ V}]$, up to $(V+)$, applied to the SHDN pin. A valid logic low is defined as $[(V-) + 0.1 \text{ V}]$, down to $(V-)$, applied to the enable pin. The maximum allowed voltage applied to SHDN is 5.5 V with respect to the negative supply, independent of the positive supply voltage. This pin should either be connected to a valid high or a low voltage or driven, and not left as an open circuit.

The logic input is a high-impedance CMOS input. Dual op amp versions are independently controlled and quad op amp versions are controlled in pairs with logic inputs. For battery-operated applications, this feature may be used to greatly reduce the average current and extend battery life. The enable time is 10 μs for full shutdown of all channels; disable time is 3 μs . When disabled, the output assumes a high-impedance state. This architecture allows the OPAx322S to be operated as a *gated* amplifier (or to have the device output multiplexed onto a common analog output bus). Shutdown time (t_{OFF}) depends on loading conditions and increases with increased load resistance. To ensure shutdown (disable) within a specific shutdown time, the specified 10-k Ω load to mid-supply ($V_S / 2$) is required. If using the OPAx322S without a load, the resulting turn-off time is significantly increased.

GENERAL LAYOUT GUIDELINES

The OPA322 is a wideband amplifier. To realize the full operational performance of the device, follow good high-frequency printed circuit board (PCB) layout practices. The bypass capacitors must be connected between each supply pin and ground as close to the device as possible. The bypass capacitor traces should be designed for minimum inductance.

LEADLESS DFN PACKAGE

The OPA2322 uses the DFN style package (also known as SON), which is a QFN with contacts on only two sides of the package bottom. This leadless package maximizes PCB space and offers enhanced thermal and electrical characteristics through an exposed pad. One of the primary advantages of the DFN package is its low height (0.8 mm).

DFN packages are physically small, and have a smaller routing area. Additionally, they offer improved thermal performance, reduced electrical parasitics, and a pinout scheme that is consistent with other commonly-used packages (such as SO and MSOP). The absence of external leads also eliminates bent-lead issues.

The DFN package can easily be mounted using standard PCB assembly techniques. See the application reports, [QFN/SON PCB Attachment \(SLUA271\)](#) and [Quad Flatpack No-Lead Logic Packages \(SCBA017\)](#), both available for download at [www.ti.com](#). **The exposed leadframe die pad on the bottom of the DFN package should be connected to the most negative potential (V₋).** The dimension of the exposed thermal die pad is 2 mm x 1,2 mm and is centered.

APPLICATION EXAMPLES

ACTIVE FILTER

The OPA322 is well-suited for active filter applications that require a wide bandwidth, fast slew rate, low-noise, single-supply operational amplifier. [Figure 37](#) shows a 500-kHz, second-order, low-pass filter using the multiple-feedback (MFB) topology. The components have been selected to provide a maximally-flat Butterworth response. Beyond the cutoff frequency, roll-off is -40 dB/dec. The Butterworth response is ideal for applications that require predictable gain characteristics, such as the anti-aliasing filter used in front of an ADC.

One point to observe when considering the MFB filter is that the output is inverted, relative to the input. If this inversion is not required, or not desired, a noninverting output can be achieved through one of these options:

1. adding an inverting amplifier;
2. adding an additional second-order MFB stage; or
3. using a noninverting filter topology, such as the Sallen-Key (shown in [Figure 38](#)).

MFB and Sallen-Key, low-pass and high-pass filter synthesis is quickly accomplished using TI's [FilterPro™](#) program. This software is available as a free download at [www.ti.com](#).

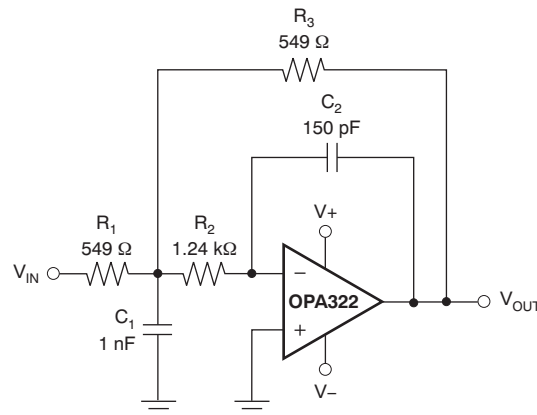


Figure 37. Second-Order Butterworth 500-kHz Low-Pass Filter

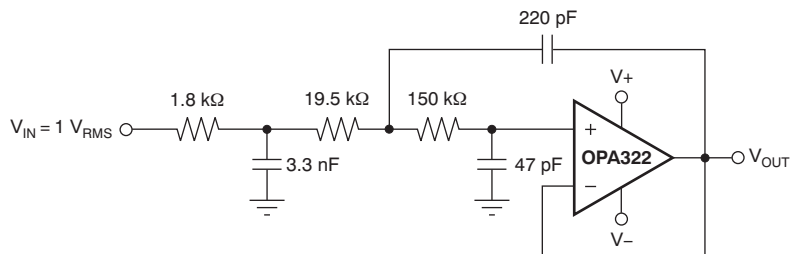


Figure 38. OPA322 Configured as a Three-Pole, 20-kHz, Sallen-Key Filter

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (March 2012) to Revision E	Page
• Changed product status from Production Data to Mixed Status	1
• Updated D, DGK pinout drawing	6
• Added Figure 26 to Figure 29	11
• Added <i>Shutdown Function</i> section	15

Changes from Revision C (November 2011) to Revision D	Page
• Changed product status from Mixed Status to Production Data	1
• Deleted shading and footnote 2 from Package/Ordering Information table	2
• Added OPA4322, OPA4322S to the Input Bias Current, <i>Input bias current</i> , <i>Over temperature</i> parameter in Electrical Characteristics table	3
• Changed Power Supply, OPA4322, OPA4322S <i>Over temperature</i> parameter maximum specification in the Electrical Characteristics table	4

Changes from Revision B (July 2011) to Revision C	Page
• Changed status of OPA2322 SO-8 (D) to production data from product preview	2

Changes from Revision A (May 2011) to Revision B	Page
• Updated OPA322 SOT23-5 device status from product preview to production data in Package/Ordering Information table	2
• Changed Input Bias Current <i>Input bias current</i> , <i>Over temperature</i> parameter in Electrical Characteristics table	3
• Changed Open-Loop Gain, <i>Open-loop voltage gain</i> parameter typical specification in the Electrical Characteristics table	3
• Changed Open-Loop Gain, <i>Phase margin</i> parameter test conditions in the Electrical Characteristics table	3
• Added test conditions to <i>Power Supply</i> section in Electrical Characteristics table	4
• Changed Power Supply, Quiescent current per amplifier OPA322/S parameter maximum specification in the Electrical Characteristics	4
• Changed Power Supply, OPA322 <i>Over temperature</i> parameter maximum specification in the Electrical Characteristics table	4
• Changed Power Supply, Quiescent current per amplifier OPA4322/S parameter typical specification in the Electrical Characteristics	4
• Changed Shutdown, <i>Quiescent current</i> , <i>per amplifier</i> parameter maximum specification in Electrical Characteristics table	4
• Added OPA322S thermal information to Thermal Information: OPA322 table	5
• Added OPA2322S thermal information to Thermal Information: OPA2322 table	5
• Added OPA4322S thermal information to Thermal Information: OPA4322 table	5
• Updated Figure 1	7
• Added Figure 25	11
• Changed <i>Overload Recovery Time</i> section	15

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2322AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2322A	Samples
OPA2322AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OOZI	Samples
OPA2322AIDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OOZI	Samples
OPA2322AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2322A	Samples
OPA2322AIDRGR	ACTIVE	SON	DRG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPCI	Samples
OPA2322AIDRGT	ACTIVE	SON	DRG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPCI	Samples
OPA2322SAIDGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPBI	Samples
OPA2322SAIDGST	ACTIVE	VSSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPBI	Samples
OPA322AIDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	RAD	Samples
OPA322AIDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	RAD	Samples
OPA322SAIDBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	RAF	Samples
OPA322SAIDBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	RAF	Samples
OPA4322AIPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O4322A	Samples
OPA4322AIPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O4322A	Samples
OPA4322SAIPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O4322SA	Samples
OPA4322SAIPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O4322SA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2322AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2322AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2322AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2322AIDRGR	SON	DRG	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA2322SAIDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2322SAIDGST	VSSOP	DGS	10	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA4322AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
OPA4322SAIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2322AIDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
OPA2322AIDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
OPA2322AIDR	SOIC	D	8	2500	367.0	367.0	35.0
OPA2322AIDRGR	SON	DRG	8	3000	367.0	367.0	35.0
OPA2322SAIDGSR	VSSOP	DGS	10	2500	367.0	367.0	35.0
OPA2322SAIDGST	VSSOP	DGS	10	250	210.0	185.0	35.0
OPA4322AIPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
OPA4322SAIPWR	TSSOP	PW	16	2000	367.0	367.0	35.0

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)

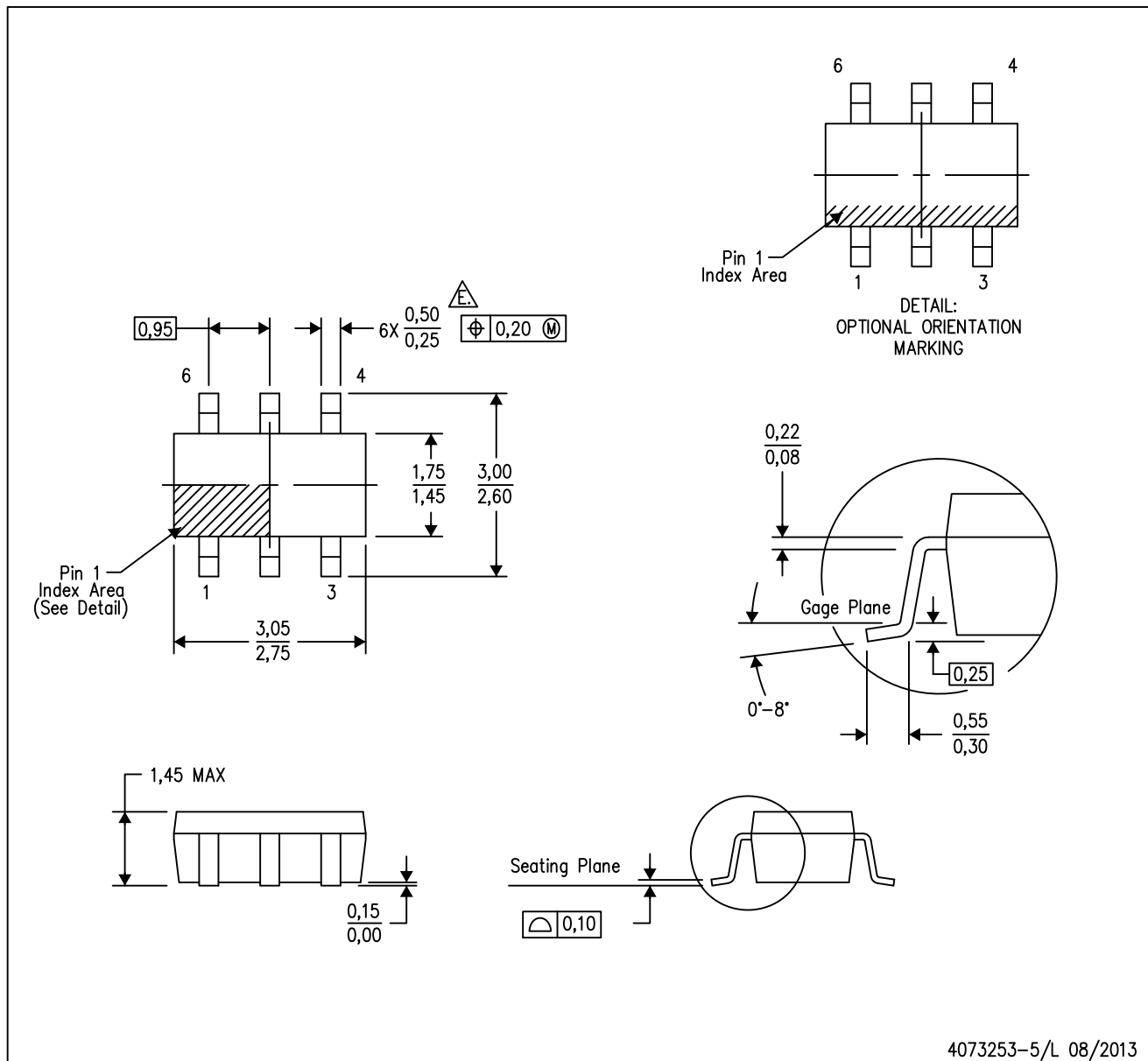
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DBV (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
 - E. Falls within JEDEC MO-178 Variation AB, except minimum lead width.

DBV (R-PDSO-G6)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE

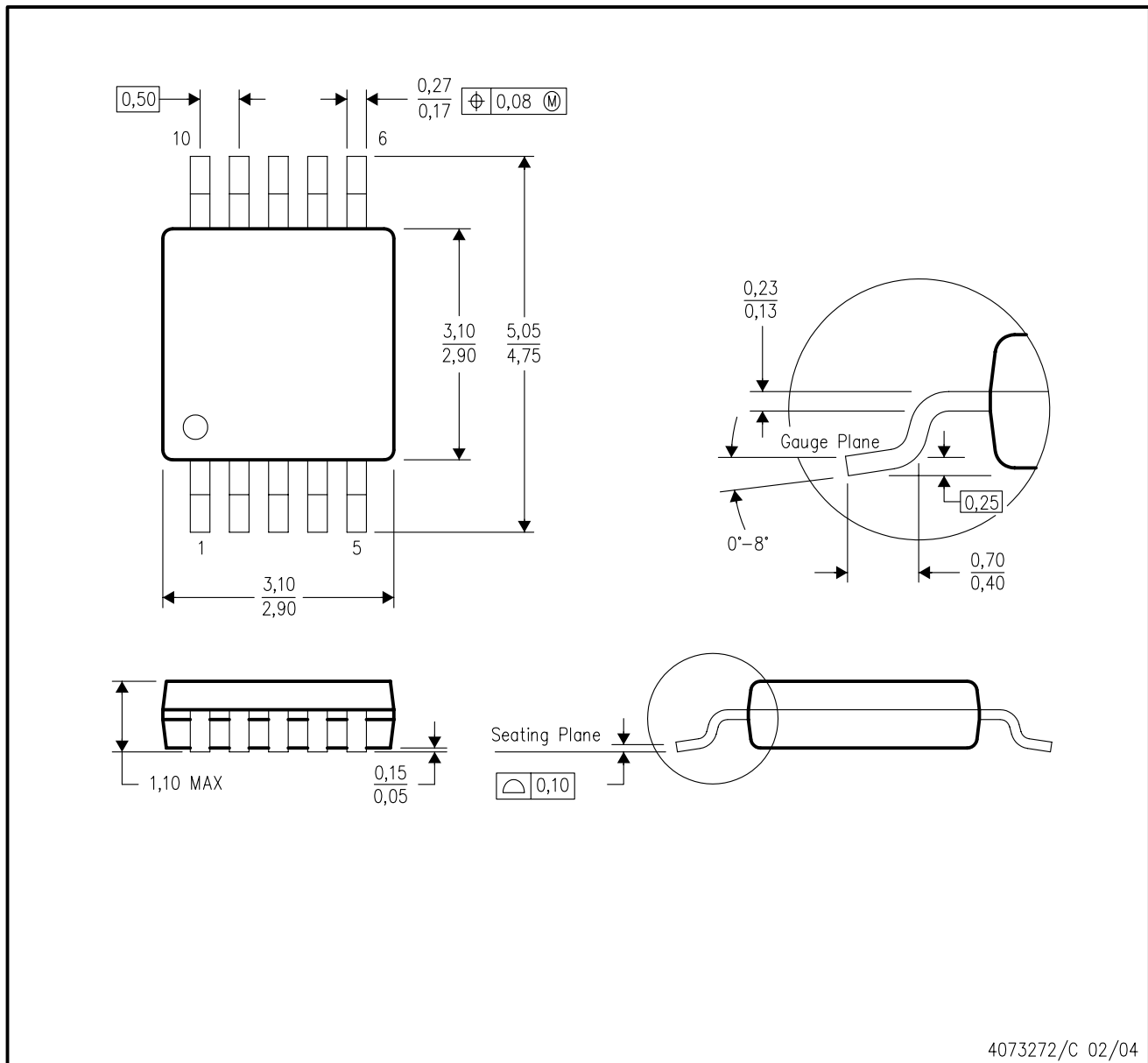


NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.

DGS (S-PDSO-G10)

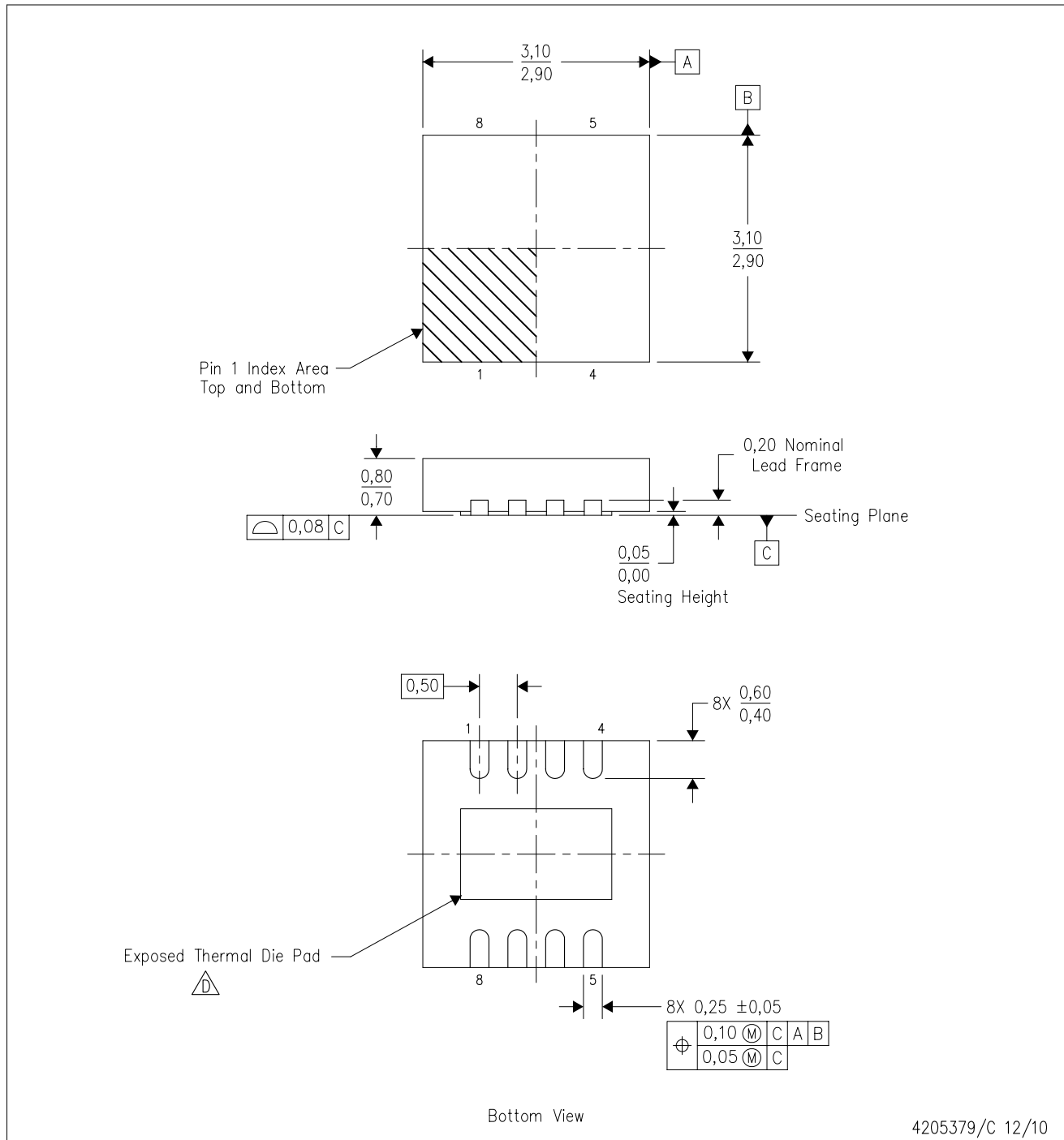
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion.
 - Falls within JEDEC MO-187 variation BA.

DRG (S-PWSON-N8)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. SON (Small Outline No-Lead) package configuration.
 - D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
 - E. JEDEC MO-229 package registration pending.

DRG (S-PWSON-N8)

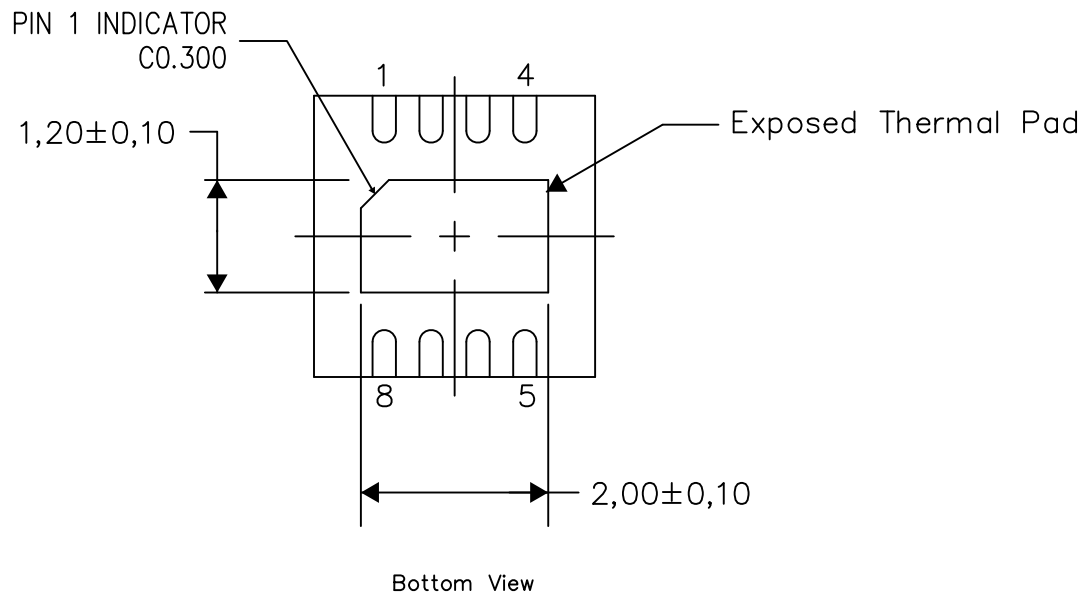
PLASTIC SMALL OUTLINE NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



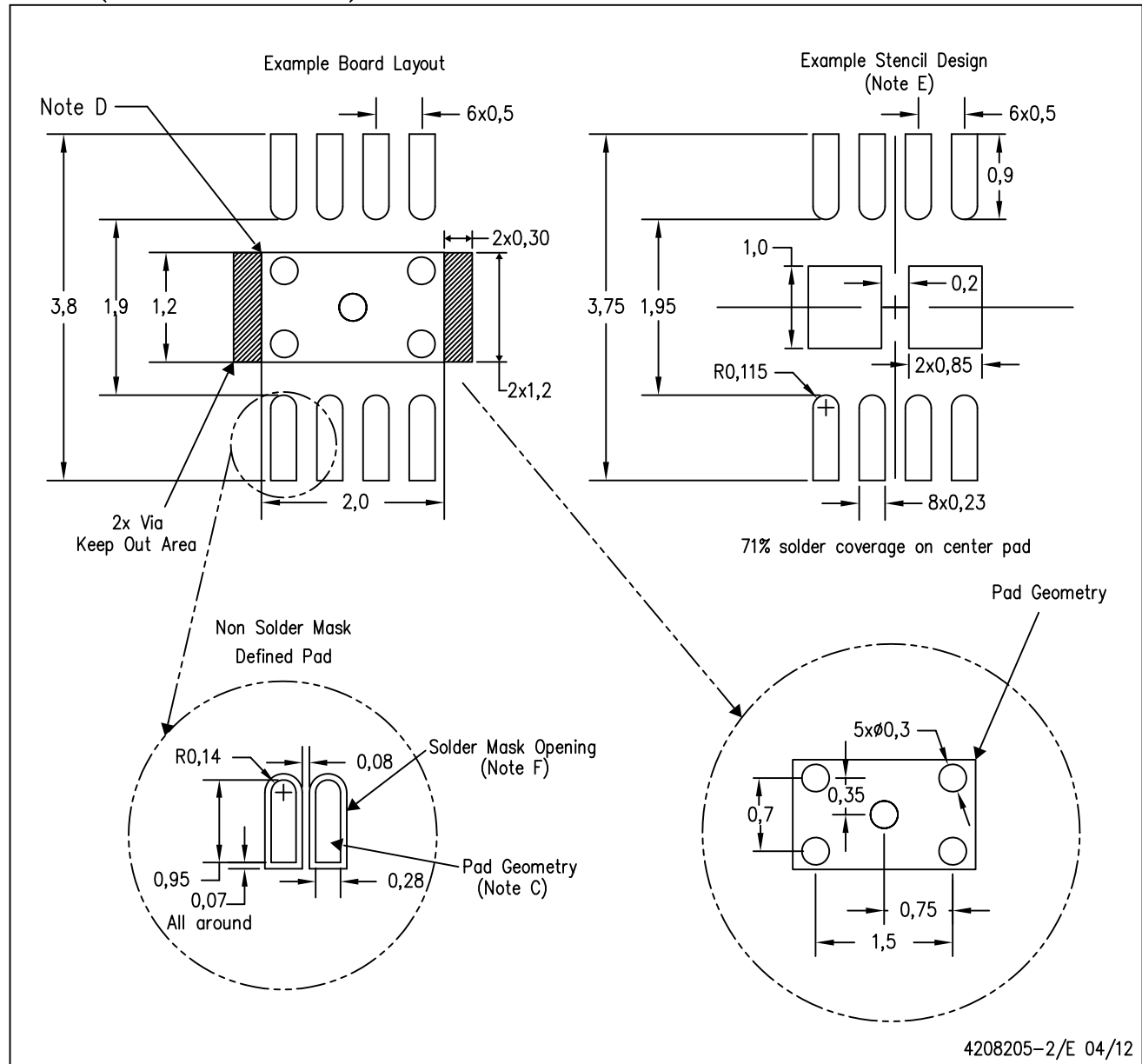
Exposed Thermal Pad Dimensions

4206881-2/G 04/12

NOTE: All linear dimensions are in millimeters

DRG (S-PWSON-N8)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-SM-782 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211284-2/F 12/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - ⚠ C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - ⚠ D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4211284-3/F 12/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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