

## Low Power, Precision FET-INPUT OPERATIONAL AMPLIFIERS

### FEATURES

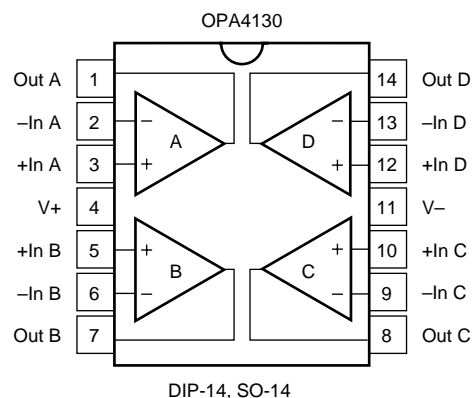
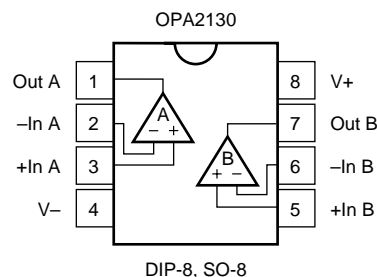
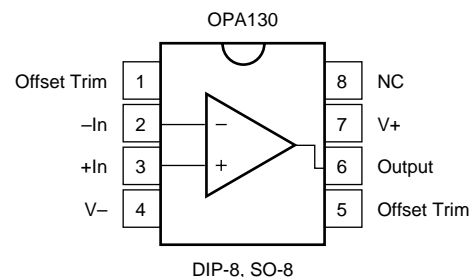
- **LOW QUIESCENT CURRENT:** 530 $\mu$ A/amp
- **LOW OFFSET VOLTAGE:** 1mV max
- **HIGH OPEN-LOOP GAIN:** 120dB min
- **HIGH CMRR:** 90dB min
- **FET INPUT:**  $I_B = 20$ pA max
- **EXCELLENT BANDWIDTH:** 1MHz
- **WIDE SUPPLY RANGE:**  $\pm 2.25$  to  $\pm 18$ V
- **SINGLE, DUAL, AND QUAD VERSIONS**

### DESCRIPTION

The OPA130 series of FET-input op amps combine precision dc performance with low quiescent current. Single, dual, and quad versions have identical specifications for maximum design flexibility. They are ideal for general-purpose, portable, and battery operated applications, especially with high source impedance.

OPA130 op amps are easy to use and free from phase inversion and overload problems often found in common FET-input op amps. Input cascode circuitry provides excellent common-mode rejection and maintains low input bias current over its wide input voltage range. OPA130 series op amps are stable in unity gain and provide excellent dynamic behavior over a wide range of load conditions, including high load capacitance. Dual and quad designs feature completely independent circuitry for lowest crosstalk and freedom from interaction, even when overdriven or overloaded.

Single and dual versions are available in DIP-8 and SO-8 surface-mount packages. Quad is available in DIP-14 and SO-14 surface-mount packages. All are specified for  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  operation.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Supply Voltage, V+ to V- .....	36V
Input Voltage .....	(V-) -0.7V to (V+) +0.7V
Output Short-Circuit <sup>(2)</sup> .....	Continuous
Operating Temperature .....	-40°C to +125°C
Storage Temperature .....	-40°C to +125°C
Junction Temperature .....	150°C

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. (2) Short-circuit to ground, one amplifier per package.

**PACKAGE/ORDERING INFORMATION**

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).



**ELECTROSTATIC  
DISCHARGE SENSITIVITY**

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

# ELECTRICAL CHARACTERISTICS

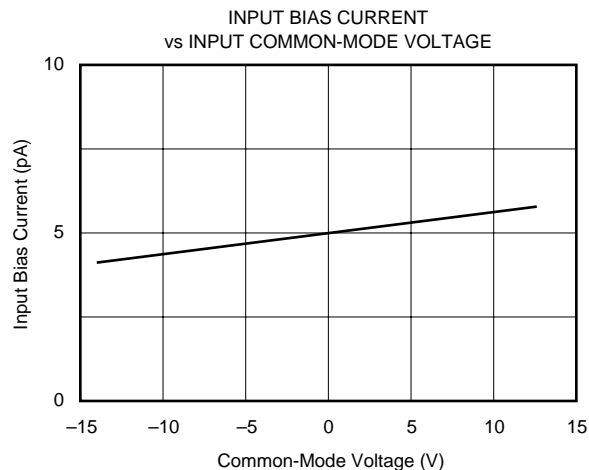
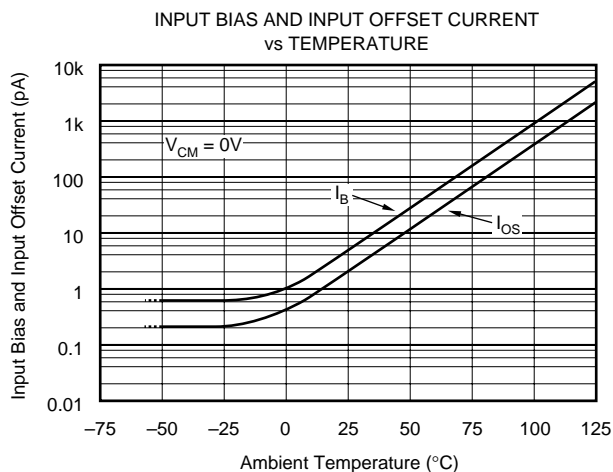
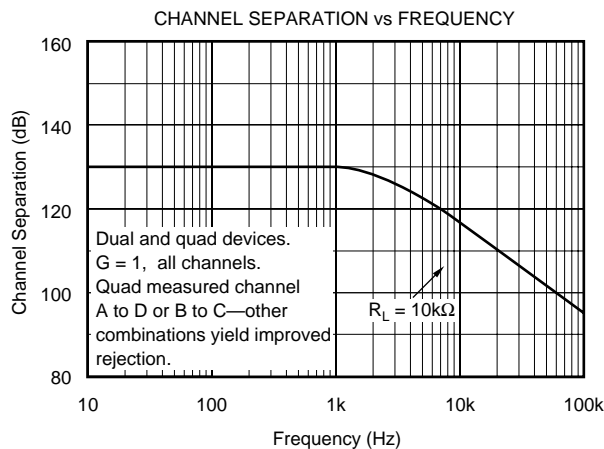
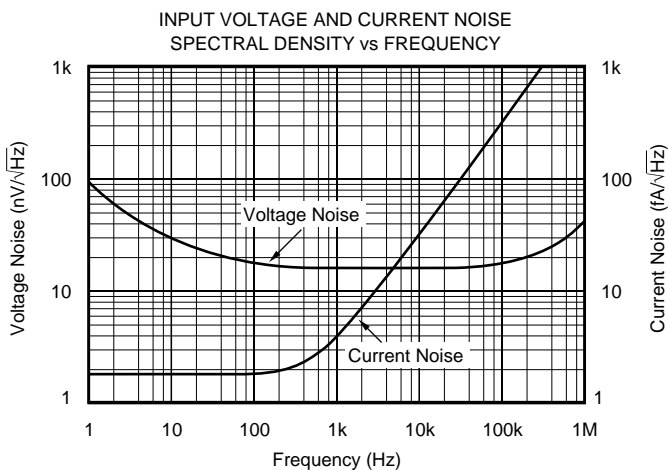
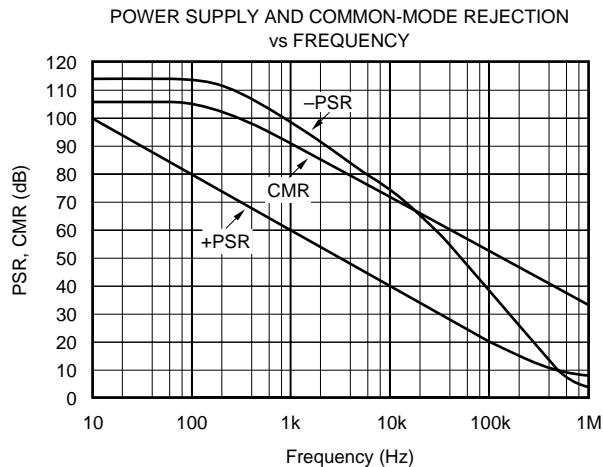
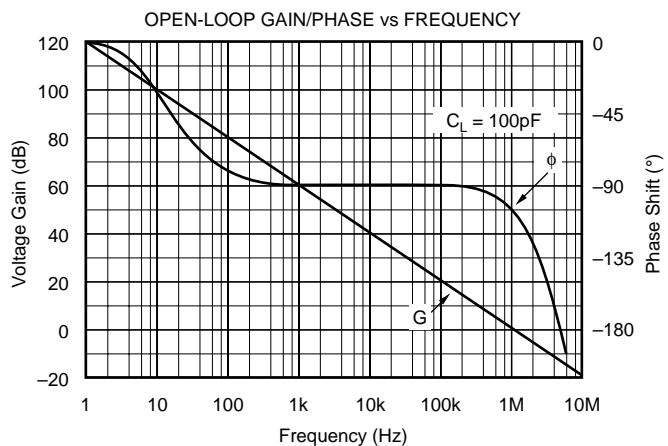
At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$ , and  $R_L = 10\text{k}\Omega$ , unless otherwise noted.

PARAMETER	CONDITION	OPA130PA, UA OPA2130PA, UA OPA4130PA, UA			UNITS
		MIN	TYP	MAX	
<b>OFFSET VOLTAGE</b> Input Offset Voltage vs Temperature <sup>(1)</sup> vs Power Supply Channel Separation (dual and quad)	Operating Temperature Range $V_S = \pm 2.25\text{V to } \pm 18\text{V}$		$\pm 0.2$ $\pm 2$ 2 0.3	$\pm 1$ $\pm 10$ 20	mV $\mu\text{V}/^\circ\text{C}$ $\mu\text{V/V}$ $\mu\text{V/V}$
<b>INPUT BIAS CURRENT</b> <sup>(2)</sup> Input Bias Current vs Temperature Input Offset Current	$V_{CM} = 0\text{V}$ $V_{CM} = 0\text{V}$		+5 See Typical Characteristics $\pm 2$	$\pm 20$ $\pm 20$	pA pA
<b>NOISE</b> Input Voltage Noise Noise Density, $f = 10\text{Hz}$ $f = 100\text{Hz}$ $f = 1\text{kHz}$ $f = 10\text{kHz}$ Current Noise Density, $f = 1\text{kHz}$			30 18 16 16 4		$\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ $\text{fA}/\sqrt{\text{Hz}}$
<b>INPUT VOLTAGE RANGE</b> Common-Mode Voltage Range, Positive Negative Common-Mode Rejection	$V_{CM} = -13\text{V to } +13\text{V}$	(V+)-2 (V-)+2 90	(V+)-1.5 (V-)+1.2 105		V V dB
<b>INPUT IMPEDANCE</b> Differential Common-Mode	$V_{CM} = -13\text{V to } +13\text{V}$		$10^{13} \parallel 1$ $10^{13} \parallel 3$		$\Omega \parallel \text{pF}$ $\Omega \parallel \text{pF}$
<b>OPEN-LOOP GAIN</b> Open-loop Voltage Gain	$V_O = -13.8\text{V to } +13\text{V}$ $R_L = 2\text{k}\Omega$ , $V_O = -13\text{V to } +12\text{V}$	120 120	135 135		dB dB
<b>FREQUENCY RESPONSE</b> Gain-Bandwidth Product Slew Rate Settling Time: 0.1% 0.01% Overload Recovery Time Total Harmonic Distortion + Noise	$G = 1$ , 10V Step, $C_L = 100\text{pF}$ $G = 1$ , 10V Step, $C_L = 100\text{pF}$ $G = 1$ , $V_{IN} = \pm 15\text{V}$ 1kHz, $G = 1$ , $V_O = 3.5\text{Vrms}$		1 2 5.5 7 2 0.0003		MHz V/ $\mu\text{s}$ $\mu\text{s}$ $\mu\text{s}$ $\mu\text{s}$ %
<b>OUTPUT</b> Voltage Output, Positive Negative Positive Negative Short-Circuit Current Capacitive Load Drive (Stable Operation)	$R_L = 2\text{k}\Omega$ $R_L = 2\text{k}\Omega$	(V+)-2 (V-)+1.2 (V+)-3 (V-)+2	(V+)-1.5 (V-)+1 (V+)-2.5 (V-)+1.5 $\pm 18$ 10		V V V V mA nF
<b>POWER SUPPLY</b> Specified Operating Voltage Operating Voltage Range Quiescent Current (per amplifier)	$I_O = 0$	$\pm 2.25$	$\pm 15$ $\pm 530$	$\pm 18$ $\pm 650$	V V $\mu\text{A}$
<b>TEMPERATURE RANGE</b> Operating Range Storage Thermal Resistance, $\theta_{JA}$ DIP-8 SO-8 Surface-Mount DIP-14 SO-14 Surface-Mount		-40 -40		+85 +125	$^\circ\text{C}$ $^\circ\text{C}$ $^\circ\text{C/W}$ $^\circ\text{C/W}$ $^\circ\text{C/W}$ $^\circ\text{C/W}$

NOTES: (1) Ensured by wafer test. (2) High-speed test at  $T_J = 25^\circ\text{C}$ .

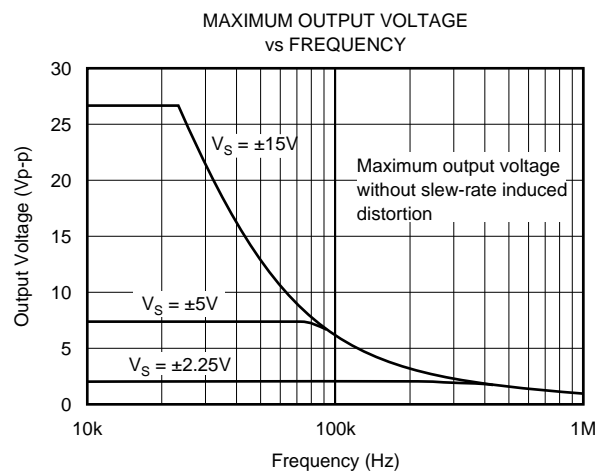
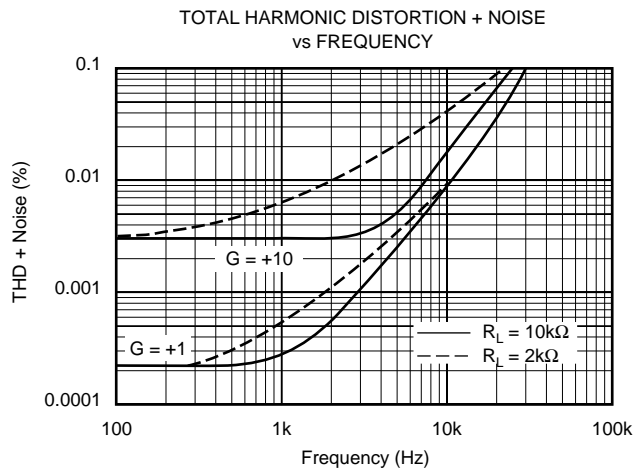
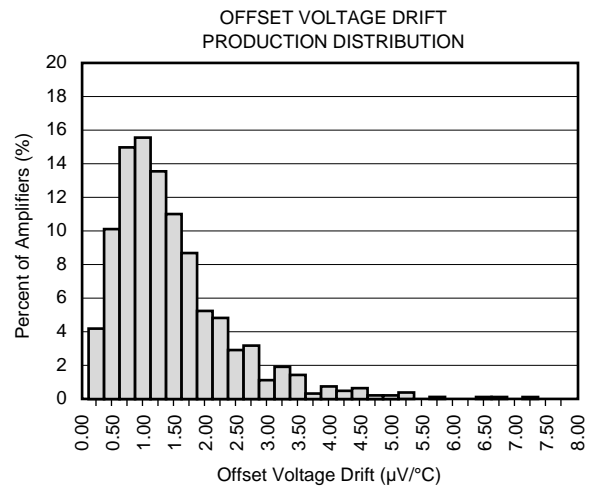
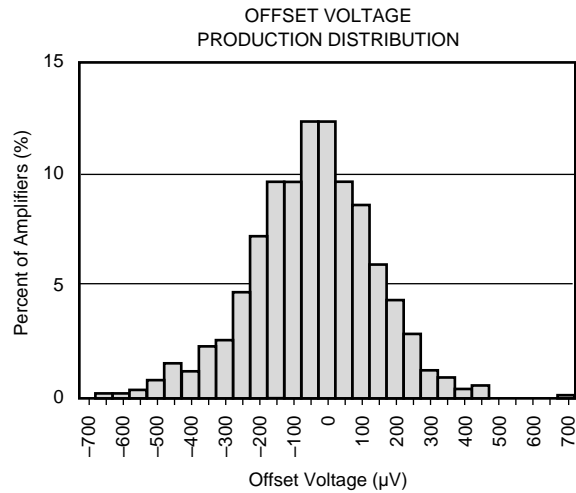
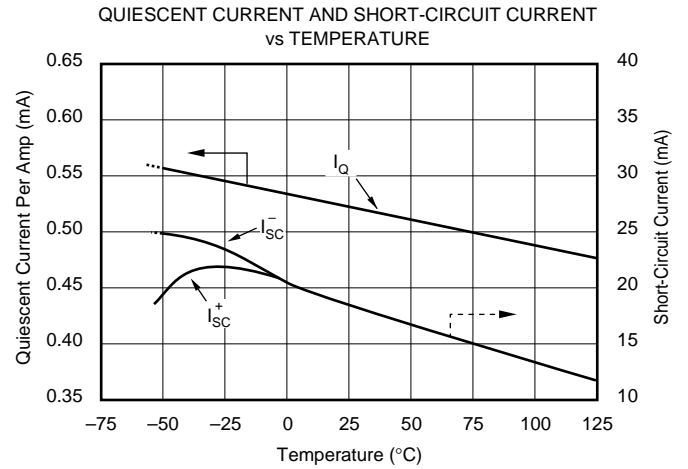
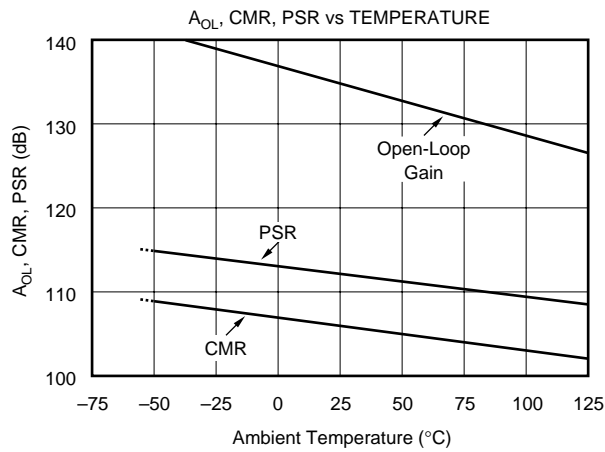
# TYPICAL CHARACTERISTICS

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$ , and  $R_L = 10\text{k}\Omega$ , unless otherwise noted.



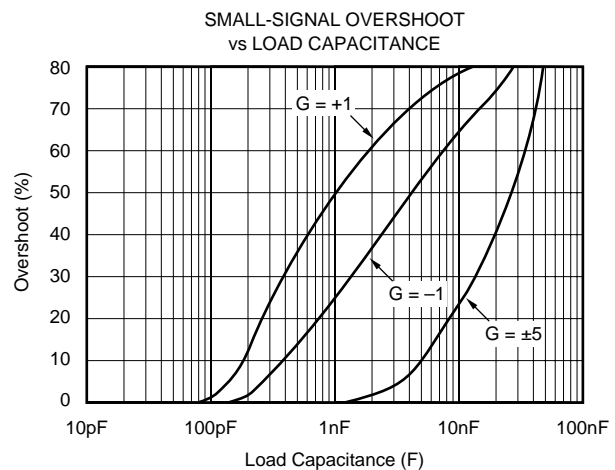
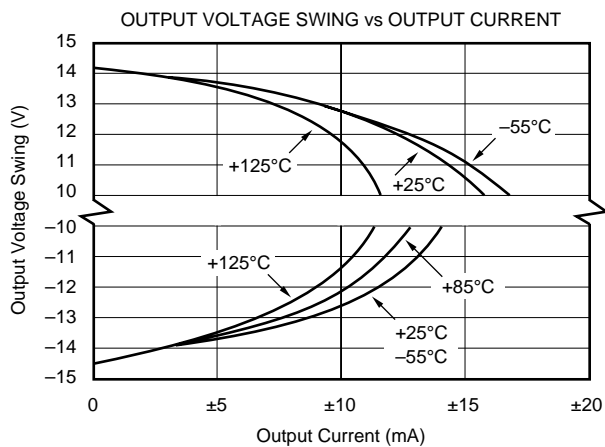
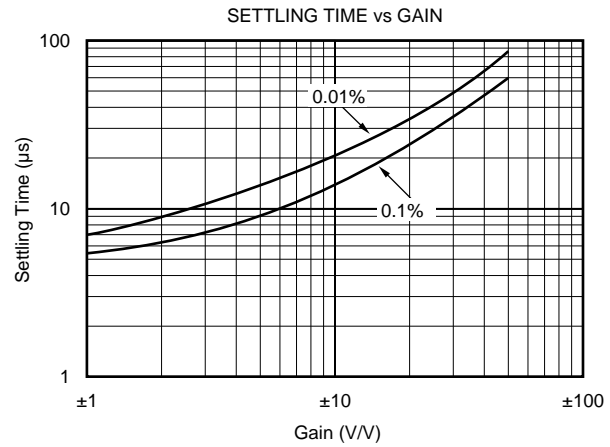
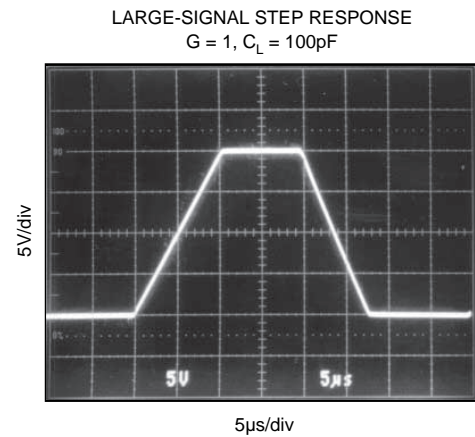
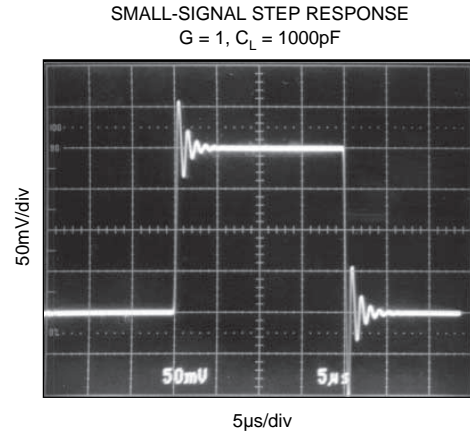
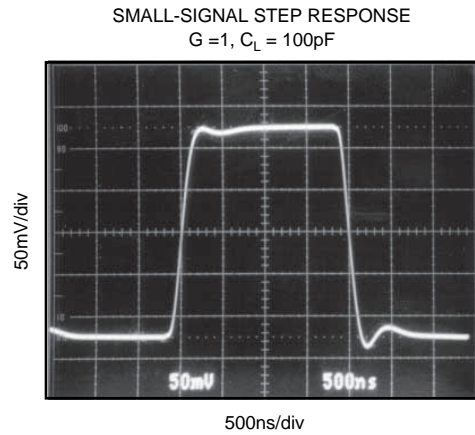
# TYPICAL CHARACTERISTICS (Cont.)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$ , and  $R_L = 10\text{k}\Omega$ , unless otherwise noted.



# TYPICAL CHARACTERISTICS (Cont.)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$ , and  $R_L = 10\text{k}\Omega$ , unless otherwise noted.



# APPLICATIONS INFORMATION

OPA130 series op amps are unity-gain stable and suitable for a wide range of general-purpose applications. Power supply pins should be bypassed with 10nF ceramic capacitors or larger.

OPA130 op amps are free from unexpected output phase-reversal common with FET op amps. Many FET-input op amps exhibit phase-reversal of the output when the input common-mode voltage range is exceeded. This can occur in voltage-follower circuits, causing serious problems in control loop applications. OPA130 series op amps are free from this undesirable behavior. All circuitry is completely independent in dual and quad versions, assuring normal behavior when one amplifier in a package is overdriven or short-circuited.

## OPERATING VOLTAGE

OPA130 series op amps operate with power supplies from  $\pm 2.25\text{V}$  to  $\pm 18\text{V}$  with excellent performance. Although specifications are production tested with  $\pm 15\text{V}$  supplies, most behavior remains unchanged throughout the full operating voltage range. Parameters which vary significantly with operating voltage are shown in the typical performance curves.

## OFFSET VOLTAGE TRIM

Offset voltage of OPA130 series amplifiers is laser trimmed and usually requires no user adjustment. The OPA130 (single op amp version) provides offset voltage trim connections on pins 1 and 5. Offset voltage can be adjusted by connecting a potentiometer as shown in Figure 1. This adjustment should be used only to null the offset of the op amp, not to adjust system offset or offset produced by the signal source. Nulling offset that is not produced by the amplifier will change the offset voltage drift behavior of the op amp.

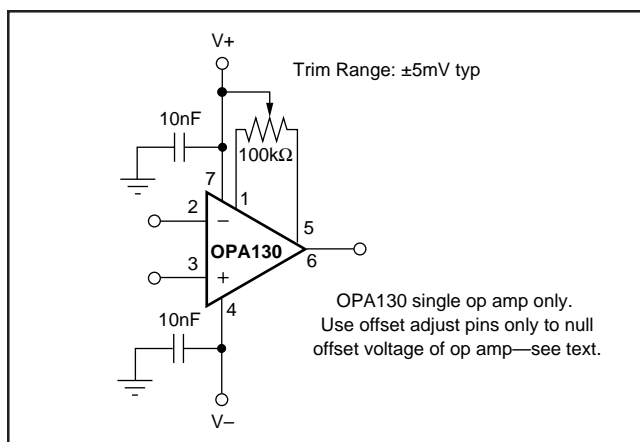


FIGURE 1. OPA130 Offset Voltage Trim Circuit.

## INPUT BIAS CURRENT

The input bias current is approximately 5pA at room temperature and increases with temperature as shown in the Typical Characteristic curve *Input Bias Current vs Temperature*.

Input stage cascode circuitry assures that the input bias current remains virtually unchanged throughout the full input common-mode range of the OPA130. See the Typical Characteristic curve *Input Bias Current vs Common-Mode Voltage*.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
OPA130UA	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 130UA	<a href="#">Samples</a>
OPA130UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 130UA	<a href="#">Samples</a>
OPA130UA/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 130UA	<a href="#">Samples</a>
OPA130UAE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 130UA	<a href="#">Samples</a>
OPA2130PA	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI			
OPA2130UA	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA 2130UA	<a href="#">Samples</a>
OPA2130UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA 2130UA	<a href="#">Samples</a>
OPA2130UA/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA 2130UA	<a href="#">Samples</a>
OPA2130UAE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA 2130UA	<a href="#">Samples</a>
OPA4130PA	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI			
OPA4130UA	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA4130UA	<a href="#">Samples</a>
OPA4130UA/2K5	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA4130UA	<a href="#">Samples</a>
OPA4130UA/2K5E4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA4130UA	<a href="#">Samples</a>
OPA4130UAE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA4130UA	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.



(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA130UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2130UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4130UA/2K5	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA130UA/2K5	SOIC	D	8	2500	367.0	367.0	35.0
OPA2130UA/2K5	SOIC	D	8	2500	367.0	367.0	35.0
OPA4130UA/2K5	SOIC	D	14	2500	367.0	367.0	38.0

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



4040047-3/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

### Products

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
OMAP Applications Processors	<a href="http://www.ti.com/omap">www.ti.com/omap</a>
Wireless Connectivity	<a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a>

### Applications

Automotive and Transportation	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Communications and Telecom	<a href="http://www.ti.com/communications">www.ti.com/communications</a>
Computers and Peripherals	<a href="http://www.ti.com/computers">www.ti.com/computers</a>
Consumer Electronics	<a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>
Energy and Lighting	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Space, Avionics and Defense	<a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a>
Video and Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>

### TI E2E Community

[e2e.ti.com](http://e2e.ti.com)