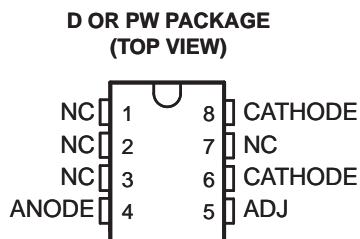


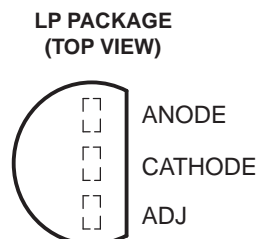
## 2.5-V INTEGRATED REFERENCE CIRCUIT

### FEATURES

- Excellent Temperature Stability
- Initial Tolerance: 0.2% Max
- Dynamic Impedance: 0.6  $\Omega$  Max
- Wide Operating Current Range
- Directly Interchangeable With LM136
- Needs No Adjustment for Minimum Temperature Coefficient



NC – No internal connection



### DESCRIPTION/ORDERING INFORMATION

The LT1009 reference circuit is a precision-trimmed 2.5-V shunt regulator featuring low dynamic impedance and a wide operating current range. The maximum initial tolerance is  $\pm 5$  mV in the LP package and  $\pm 10$  mV in the D and PW packages. The reference tolerance is achieved by on-chip trimming, which minimizes the initial voltage tolerance and the temperature coefficient,  $\alpha_{VZ}$ .

Although the LT1009 needs no adjustments, a third terminal (ADJ) allows the reference voltage to be adjusted  $\pm 5\%$  to eliminate system errors. In many applications, the LT1009 can be used as a terminal-for-terminal replacement for the LM136-2.5, which eliminates the external trim network.

The LT1009 uses include 5-V system references, 8-bit analog-to-digital converter (ADC) and digital-to-analog converter (DAC) references, and power-supply monitors. The device also can be used in applications such as digital voltmeters and current-loop measurement and control systems.

The LT1009C is characterized for operation from 0°C to 70°C. The LT1009I is characterized for operation from –40°C to 85°C.

### SYMBOL



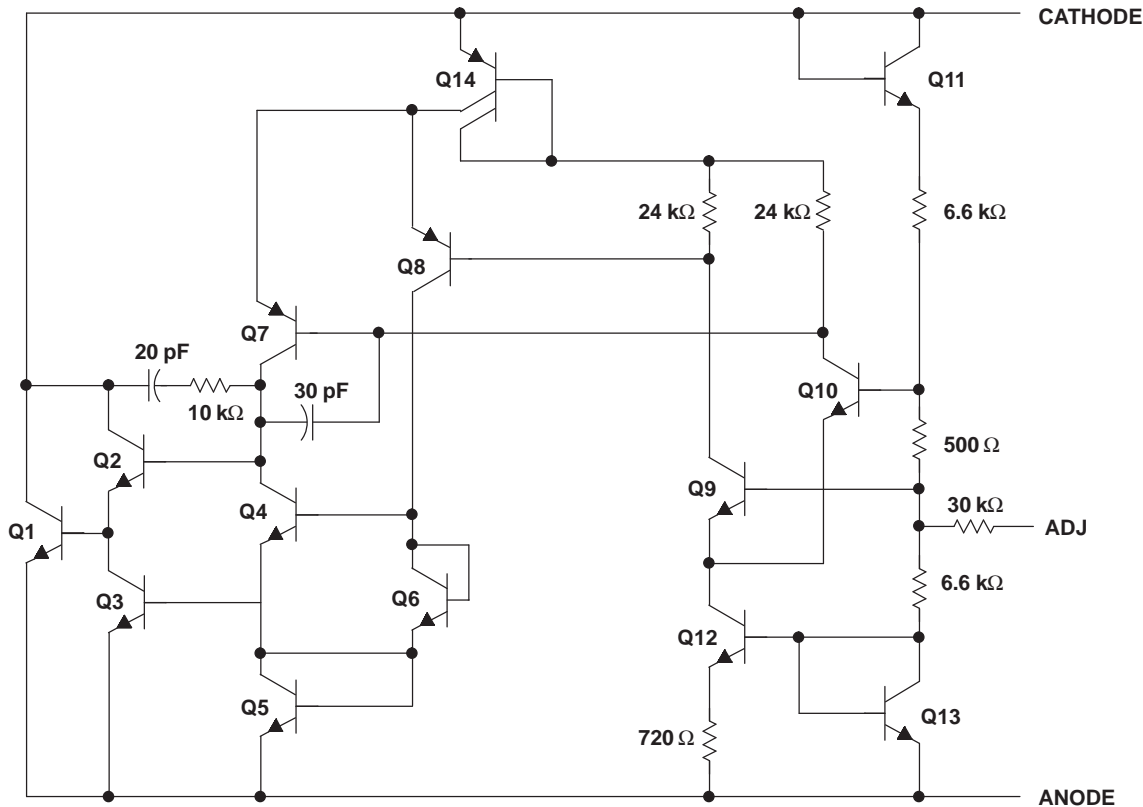
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ORDERING INFORMATION<sup>(1)</sup>

T <sub>A</sub>	PACKAGE <sup>(2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	SOIC – D	Tube of 75	LT1009CD	1009C
		Reel of 2500	LT1009CDR	
	TO-226/TO-92 – LP	Bulk of 1000	LT1009CLP	LT1009C
		Ammo of 2000	LT1009CLPM	
		Reel of 2000	LT1009CLPR	
	TSSOP – PW	Tube of 150	LT1009CPW	1009C
		Reel of 2000	LT1009CPWR	
–40°C to 85°C	SOIC – D	Tube of 75	LT1009ID	1009I
		Reel of 2500	LT1009IDR	
	TO-226/TO-92 – LP	Bulk of 1000	LT1009ILP	LT1009I
		Ammo of 2000	LT1009ILPM	
		Reel of 2000	LT1009ILPR	
	TSSOP – PW	Tube of 150	LT1009IPW	1009I
		Reel of 2000	LT1009IPWR	

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).
- (2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

SCHEMATIC



NOTE: All component values shown are nominal.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$I_R$	Reverse current		20	mA
$I_F$	Forward current		10	mA
$\theta_{JA}$	Package thermal impedance <sup>(2)(3)</sup>	D package	97	°C/W
		LP package	140	
		PW package	149	
$T_J$	Operating virtual junction temperature		150	°C
$T_{stg}$	Storage temperature range	–65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Maximum power dissipation is a function of  $T_J(\text{max})$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(\text{max}) - T_A)/\theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

## RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
$T_A$	Operating free-air temperature range	LT1009C	0	°C
		LT1009I	–40	

## ELECTRICAL CHARACTERISTICS

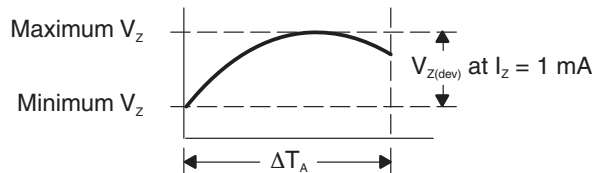
at specified free-air temperature

PARAMETER	TEST CONDITIONS		T <sub>A</sub> <sup>(1)</sup>	LT1009C			LT1009I			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>Z</sub> Reference voltage	I <sub>Z</sub> = 1 mA	D/PW package	25°C	2.49	2.5	2.51	2.49	2.5	2.51	V
		LP package		2.495	2.5	2.505	2.495	2.5	2.505	
		D/PW package	Full range	2.485		2.515	2.475		2.525	
		LP package		2.491		2.509	2.48		2.52	
V <sub>F</sub> Forward voltage	I <sub>F</sub> = 2 mA		25°C	0.4		1	0.4		1	V
Adjustment range	I <sub>Z</sub> = 1 mA, V <sub>ADJ</sub> = GND to V <sub>Z</sub>		25°C	125			125			mV
	I <sub>Z</sub> = 1 mA, V <sub>ADJ</sub> = 0.6 V to V <sub>Z</sub> – 0.6 V			45			45			
ΔV <sub>Z(temp)</sub>	Change in reference voltage with temperature	D/PW package	Full range	5			15			mV
		LP package		4			15			
αV <sub>Z</sub>	Average temperature coefficient of reference voltage <sup>(2)</sup>	I <sub>Z</sub> = 1 mA, V <sub>ADJ</sub> = open	0°C to 70°C	15    25			15    25			ppm/°C
			–40°C to 85°C				20    35			
ΔV <sub>Z</sub>	Change in reference voltage with current	I <sub>Z</sub> = 400 μA to 10 mA	25°C	2.6    10			2.6    6			mV
			Full range	12			10			
ΔV <sub>Z</sub> /Δt	Long-term change in reference voltage	I <sub>Z</sub> = 1 mA	25°C	20			20			ppm/khr
Z <sub>Z</sub>	Reference impedance	I <sub>Z</sub> = 1 mA	25°C	0.3    1			0.3    1			Ω
			Full range	1.4			1.4			

(1) Full range is 0°C to 70°C for the LT1009C and –40°C to 85°C for the LT1009I.

(2) The deviation parameter V<sub>Z(dev)</sub> is defined as the difference between the maximum and minimum values obtained over the recommended operating temperature range, measured at I<sub>Z</sub> = 1 mA. The average full-range temperature coefficient of the reference voltage (αV<sub>Z</sub>) is defined as:

$$|\alpha V_Z| \left( \frac{\text{ppm}}{^\circ\text{C}} \right) = \frac{\left( \frac{V_{Z(\text{dev})}}{V_Z \text{ at } 25^\circ\text{C}} \right) \times 10^6}{\Delta T_A}$$



αV<sub>Z</sub> can be positive or negative, depending upon whether the minimum V<sub>Z</sub> or maximum V<sub>Z</sub>, respectively, occurs at the lower temperature.

For example, at I<sub>Z</sub> = 1 mA, maximum V<sub>Z</sub> = 2501 mV at 30°C, minimum V<sub>Z</sub> = 2497 mV at 0°C, V<sub>Z</sub> = 2500 mV at 25°C, ΔT<sub>A</sub> = 70°C for LT1009C:

$$|\alpha V_Z| = \frac{\left( \frac{4 \text{ mV}}{2500 \text{ mV}} \right) \times 10^6}{70^\circ\text{C}} \approx 23 \frac{\text{ppm}}{^\circ\text{C}}$$

Because minimum V<sub>Z</sub> occurs at the lower temperature, the coefficient in this example is positive.

## TYPICAL CHARACTERISTICS

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

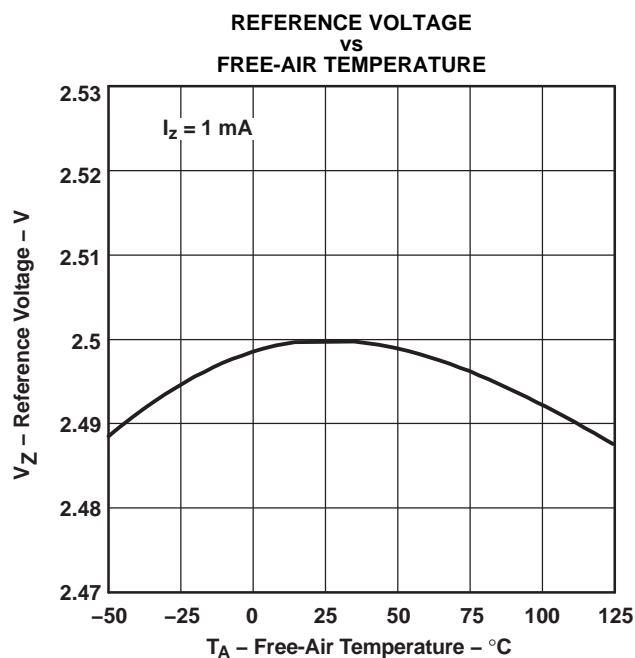


Figure 1.

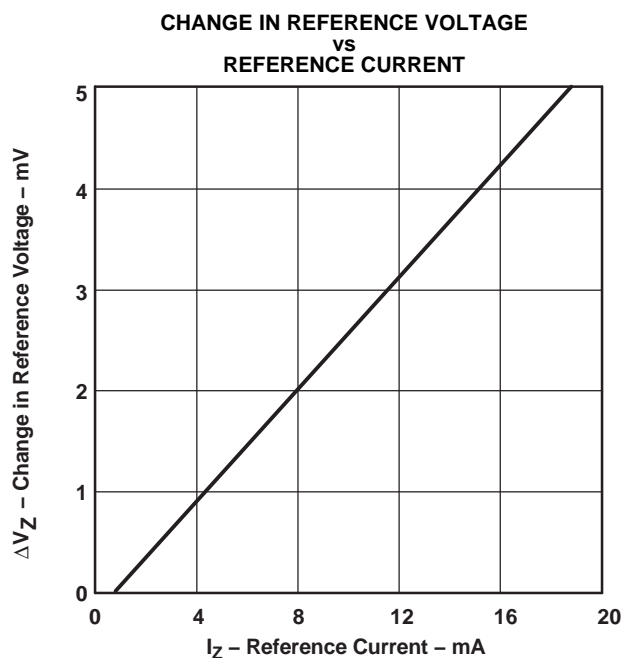


Figure 2.

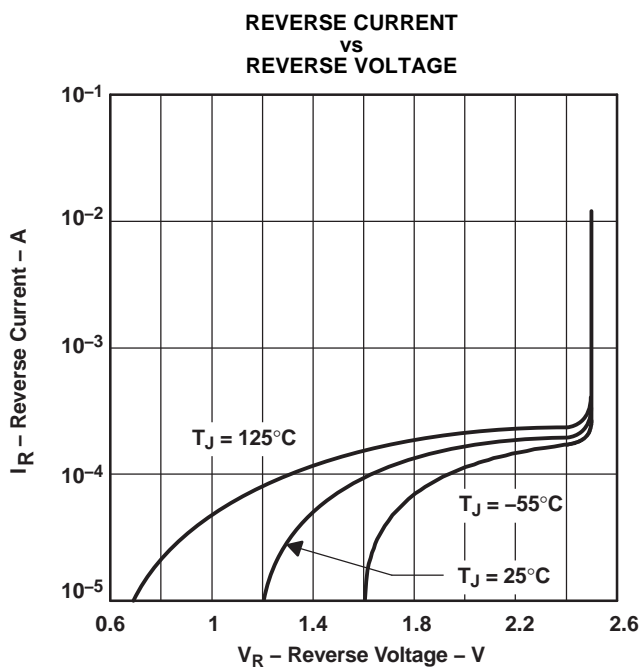


Figure 3.

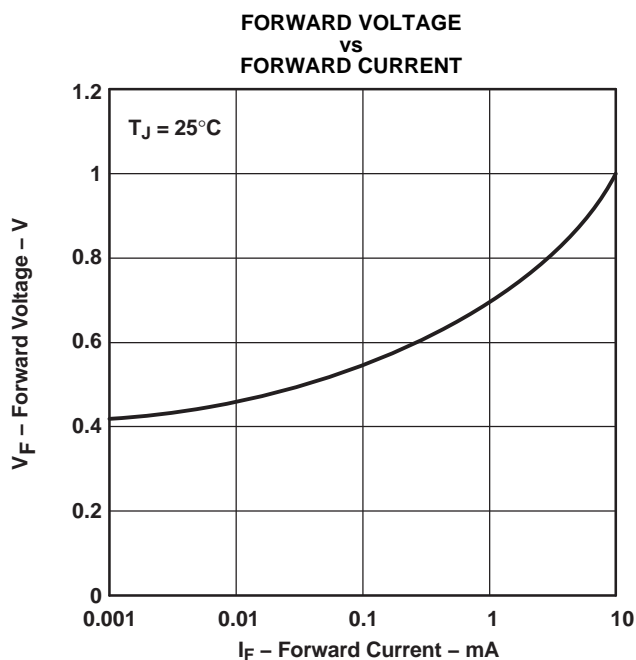


Figure 4.

# TYPICAL CHARACTERISTICS (continued)

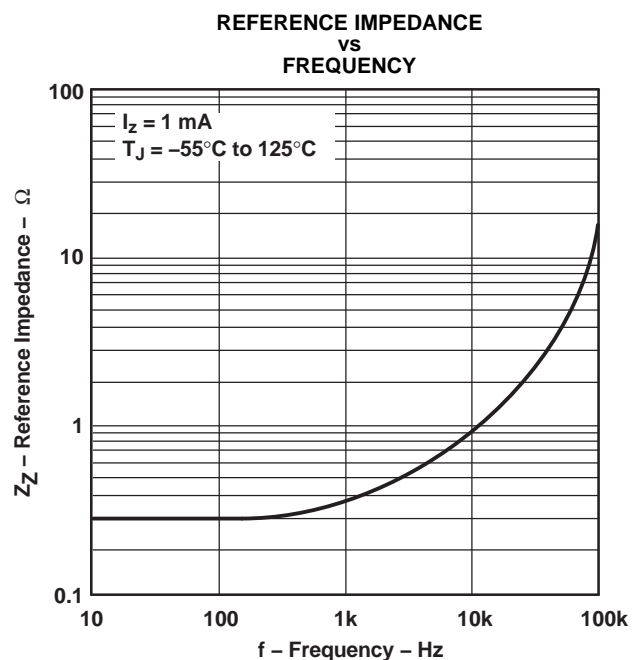


Figure 5.

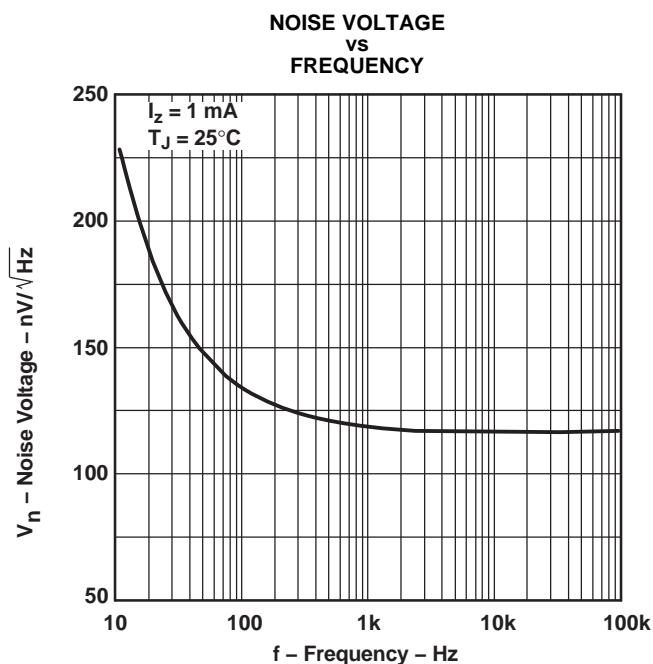


Figure 6.

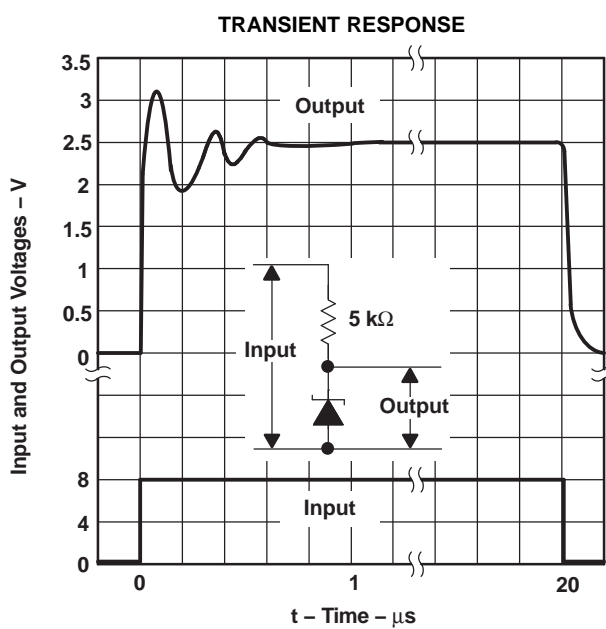
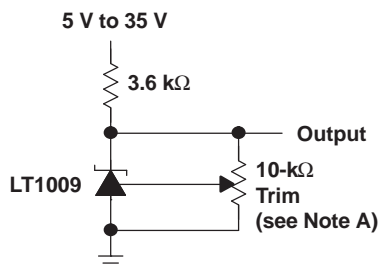


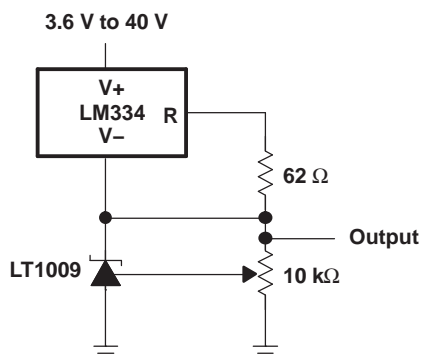
Figure 7.

## APPLICATION INFORMATION

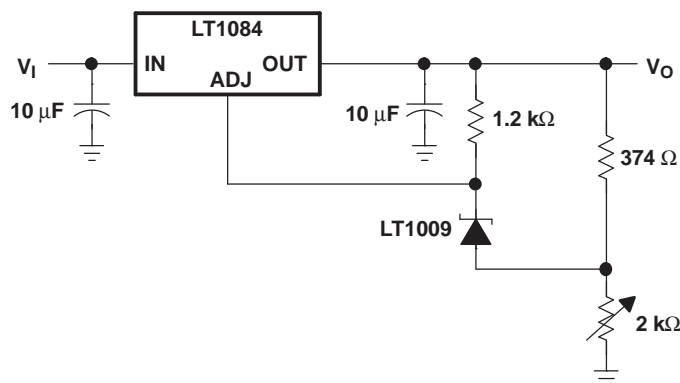


A. This does not affect temperature coefficient. It provides  $\pm 5\%$  trim range.

**Figure 8. 2.5-V Reference**



**Figure 9. Adjustable Reference With Wide Supply Range**



**Figure 10. Power Regulator With Low Temperature Coefficient**

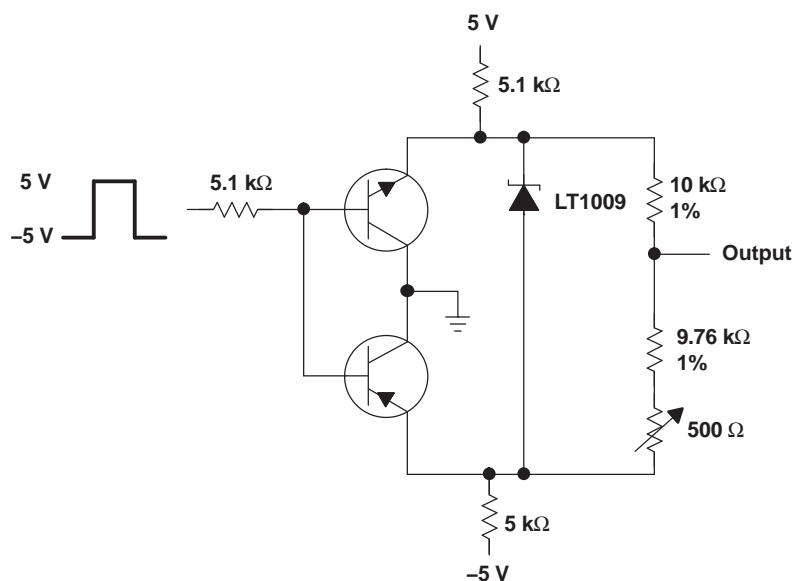
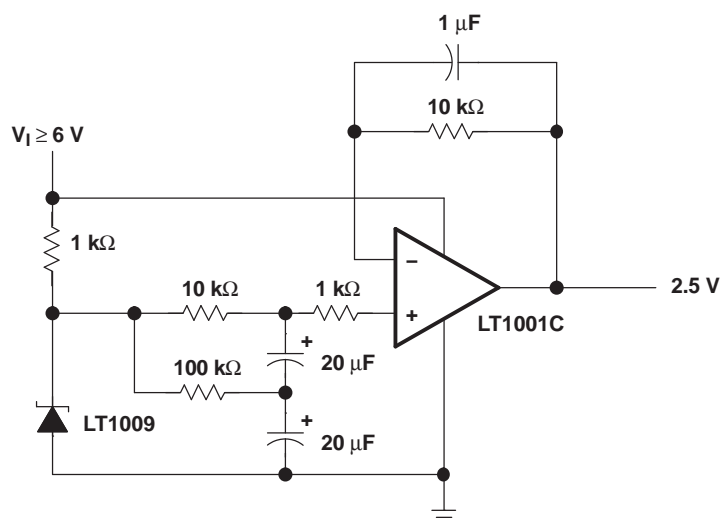
Figure 11. Switchable  $\pm 1.25$ -V Bipolar Reference

Figure 12. Low-Noise 2.5-V Buffered Reference



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LT1009CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	1009C	<a href="#">Samples</a>
LT1009CDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	1009C	<a href="#">Samples</a>
LT1009CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	1009C	<a href="#">Samples</a>
LT1009CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	1009C	<a href="#">Samples</a>
LT1009CDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	1009C	<a href="#">Samples</a>
LT1009CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	1009C	<a href="#">Samples</a>
LT1009CLP	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 70	LT1009C	<a href="#">Samples</a>
LT1009CLPE3	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 70	LT1009C	<a href="#">Samples</a>
LT1009CLPM	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 70	LT1009C	<a href="#">Samples</a>
LT1009CLPME3	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 70	LT1009C	<a href="#">Samples</a>
LT1009CLPR	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 70	LT1009C	<a href="#">Samples</a>
LT1009CLPRE3	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	0 to 70	LT1009C	<a href="#">Samples</a>
LT1009CPK	OBSOLETE	SOT-89	PK	3		TBD	Call TI	Call TI	0 to 70		
LT1009CPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	1009C	<a href="#">Samples</a>
LT1009CPWRE4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	1009C	<a href="#">Samples</a>
LT1009CPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	1009C	<a href="#">Samples</a>
LT1009ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	1009I	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LT1009IDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	1009I	<a href="#">Samples</a>
LT1009IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	1009I	<a href="#">Samples</a>
LT1009IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	1009I	<a href="#">Samples</a>
LT1009IDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	1009I	<a href="#">Samples</a>
LT1009IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	1009I	<a href="#">Samples</a>
LT1009ILP	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	-40 to 85	LT1009I	<a href="#">Samples</a>
LT1009ILPE3	ACTIVE	TO-92	LP	3	1000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	-40 to 85	LT1009I	<a href="#">Samples</a>
LT1009ILPR	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	-40 to 85	LT1009I	<a href="#">Samples</a>
LT1009ILPRE3	ACTIVE	TO-92	LP	3	2000	Pb-Free (RoHS)	CU SN	N / A for Pkg Type	-40 to 85	LT1009I	<a href="#">Samples</a>
LT1009IPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	1009I	<a href="#">Samples</a>
LT1009IPWRE4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	1009I	<a href="#">Samples</a>
LT1009IPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	1009I	<a href="#">Samples</a>
LT1009QDR	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 125		
LT1009Y	OBSOLETE	DIESALE	Y	0		TBD	Call TI	Call TI			

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

#### **OTHER QUALIFIED VERSIONS OF LT1009 :**

- Military: [LT1009M](#)

NOTE: Qualified Version Definitions:

- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LT1009CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LT1009CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LT1009IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LT1009IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS

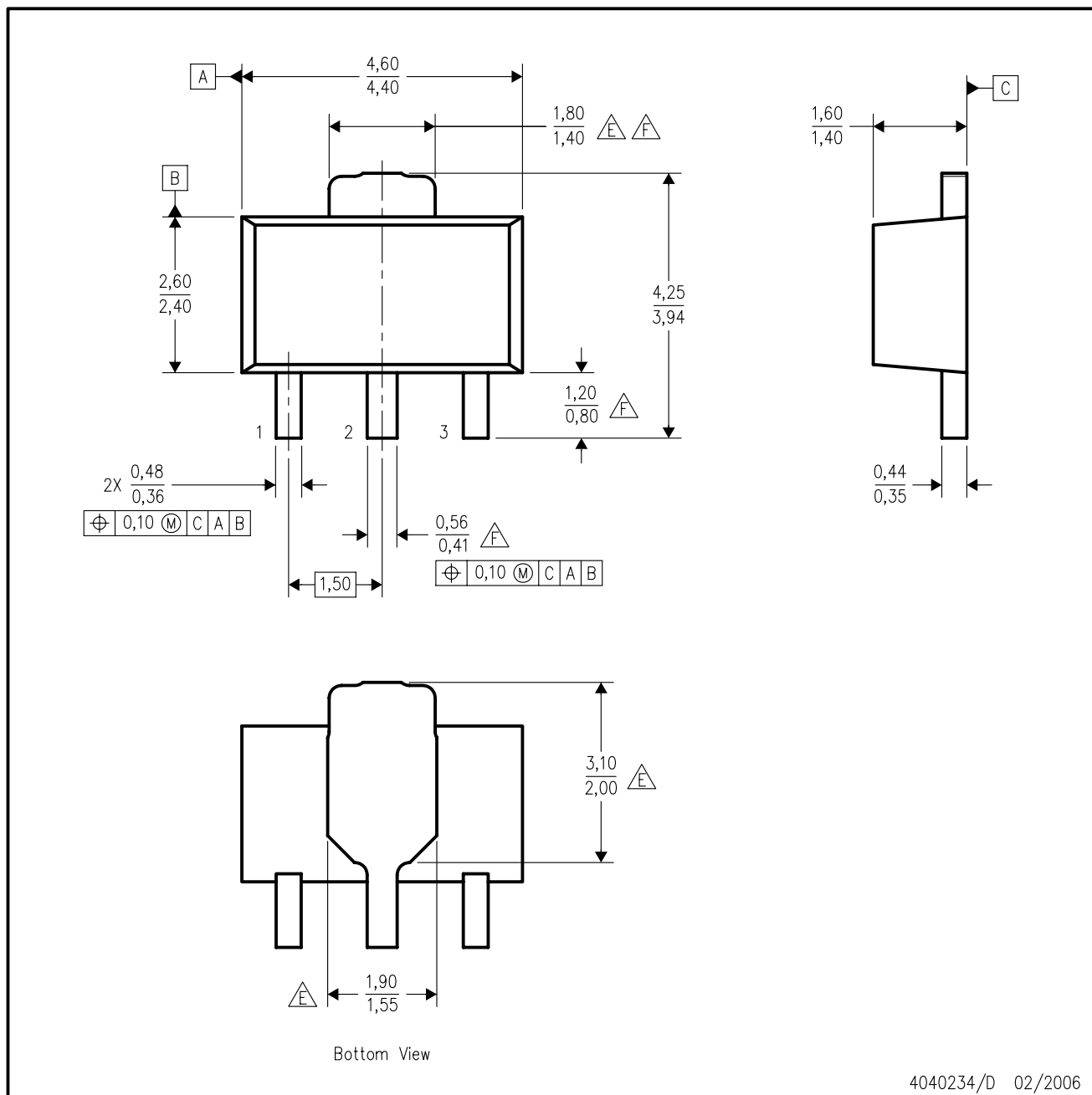


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LT1009CDR	SOIC	D	8	2500	340.5	338.1	20.6
LT1009CPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
LT1009IDR	SOIC	D	8	2500	340.5	338.1	20.6
LT1009IPWR	TSSOP	PW	8	2000	367.0	367.0	35.0

PK (R-PSSO-F3)

PLASTIC SINGLE-IN-LINE PACKAGE



4040234/D 02/2006

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - The center lead is in electrical contact with the tab.
  - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion not to exceed 0.15 per side.
- △E Thermal pad contour optional within these dimensions.
- △F Falls within JEDEC TO-243 variation AA, except minimum lead length, pin 2 minimum lead width, minimum tab width.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE

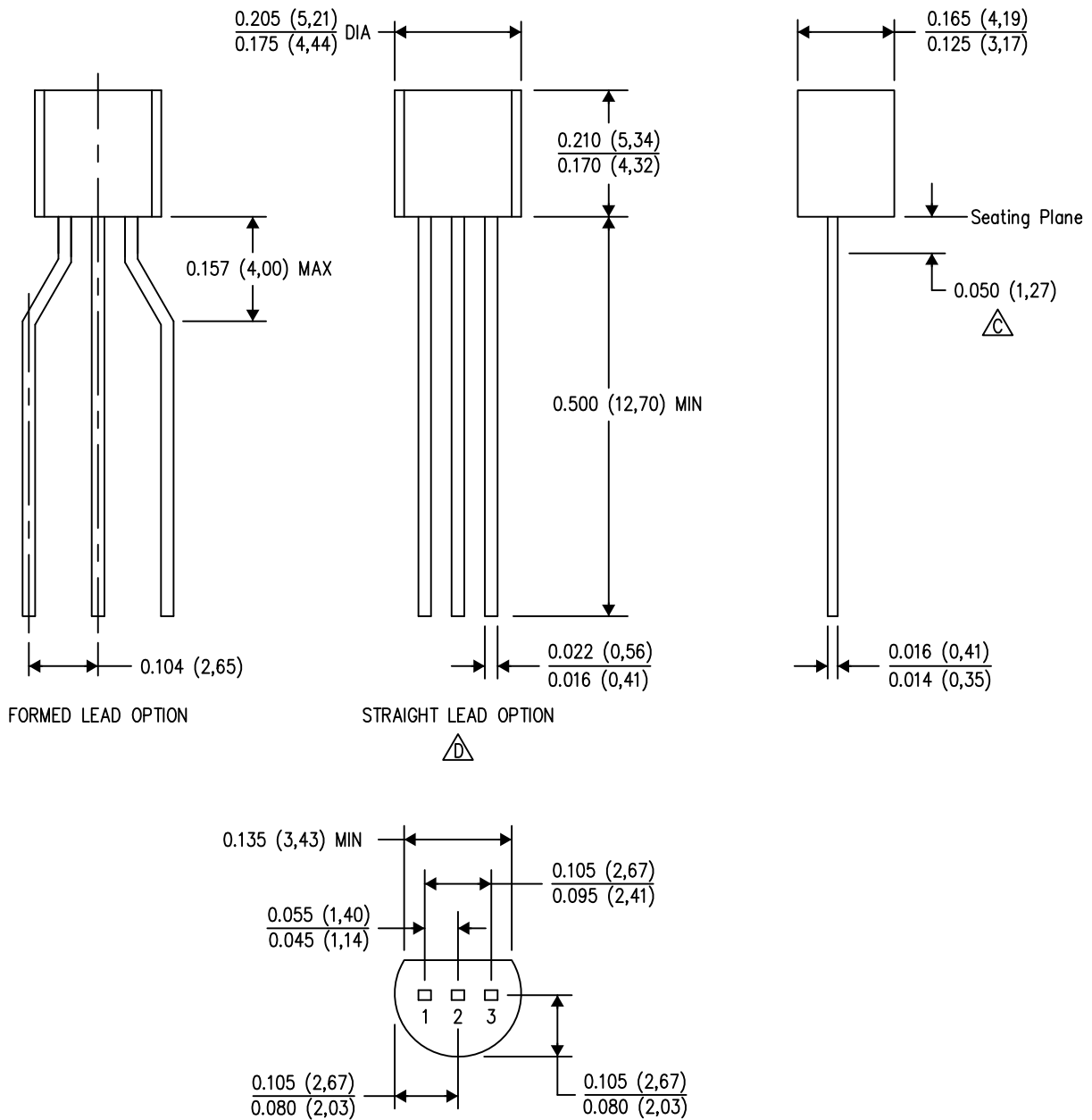


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



LP (O-PBCY-W3)

PLASTIC CYLINDRICAL PACKAGE

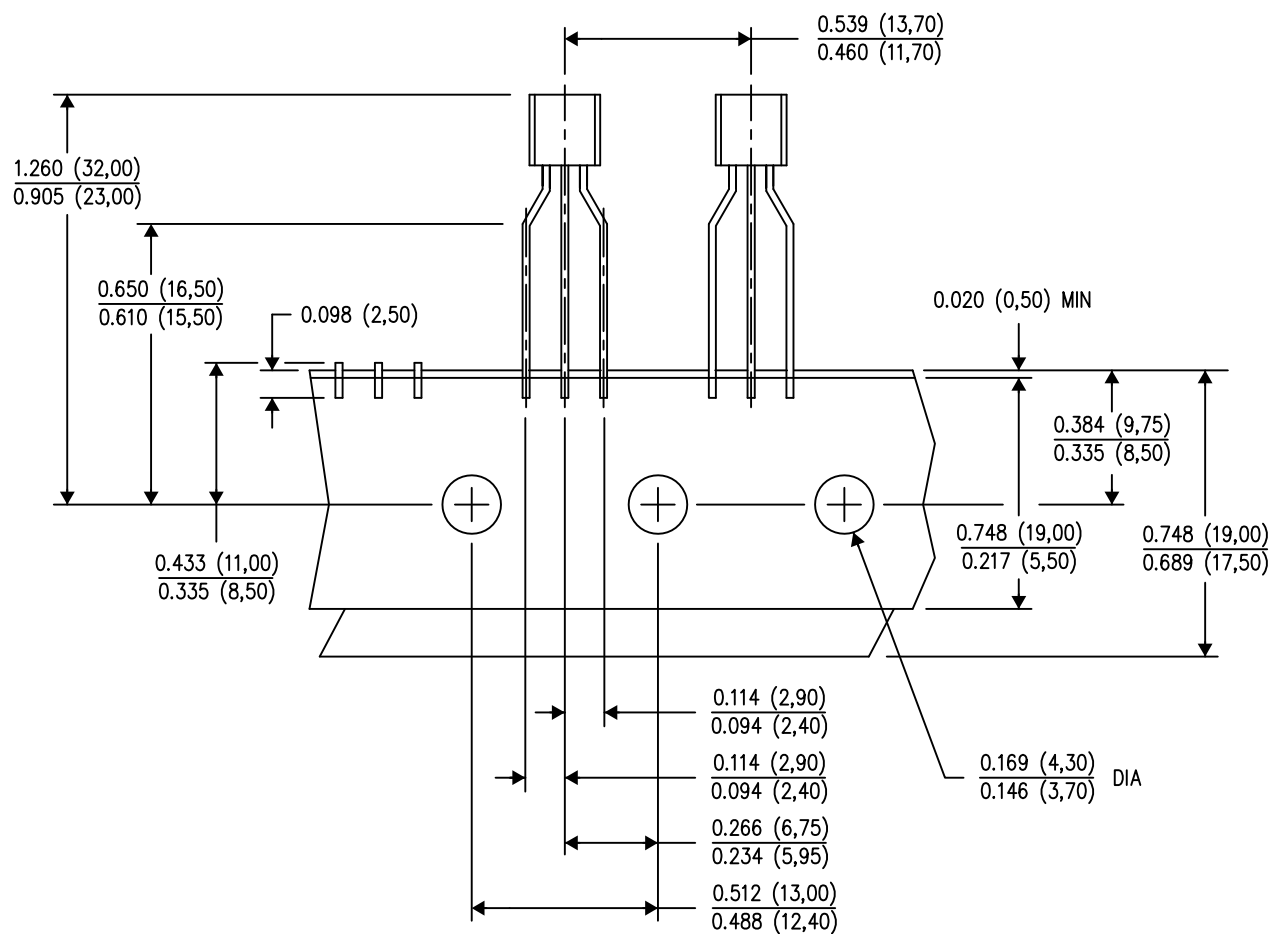


4040001-2/E 08/13

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Lead dimensions are not controlled within this area.
  - D. Falls within JEDEC TO-226 Variation AA (TO-226 replaces TO-92).
  - E. Shipping Method:  
 Straight lead option available in bulk pack only.  
 Formed lead option available in tape & reel or ammo pack.  
 Specific products can be offered in limited combinations of shipping mediums and lead options.  
 Consult product folder for more information on available options.

LP (O-PBCY-W3)

PLASTIC CYLINDRICAL PACKAGE



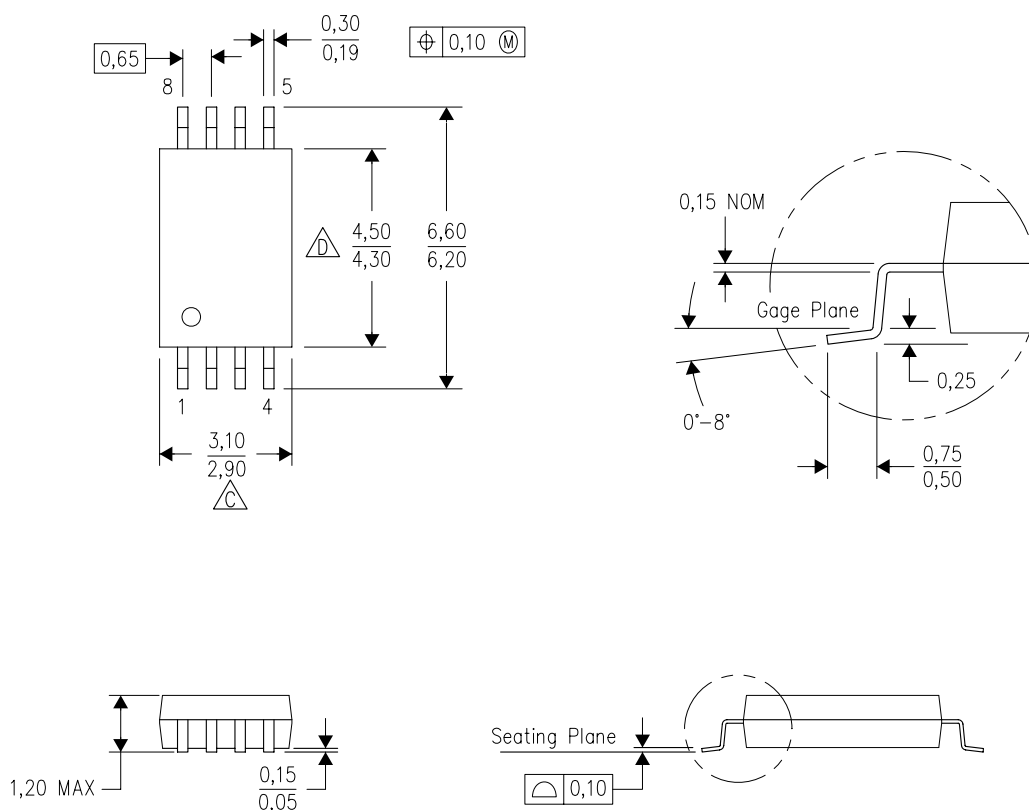
TAPE &amp; REEL

4040001-3/E 08/13

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Tape and Reel information for the Formed Lead Option package.

PW (R-PDSO-G8)

PLASTIC SMALL OUTLINE



4040064-2/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

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