

# LMV721-N/LMV722 10MHz, Low Noise, Low Voltage, and Low Power Operational Amplifier

Check for Samples: [LMV721-N](#), [LMV722-N](#)

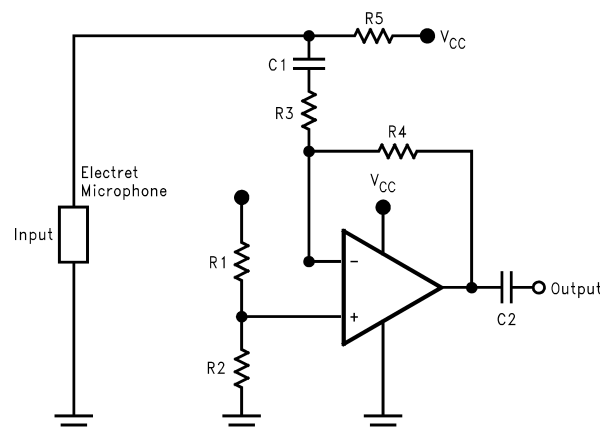
## FEATURES

- (For Typical, 5 V Supply Values; Unless Otherwise Noted)
- Ensured 2.2V and 5.0V Performance
- Low Supply Current LMV721-N/2 930 $\mu$ A/Amplifier at 2.2V
- High Unity-Gain Bandwidth 10MHz
- Rail-to-Rail Output Swing
  - at 600 $\Omega$  Load 120mV from Either Rail at 2.2V
  - at 2k $\Omega$  Load 50mV from Either Rail at 2.2V
- Input Common Mode Voltage Range Includes Ground
- Silicon Dust, SC70-5 Package 2.0x2.0x1.0 mm
- Input Voltage Noise 9 nV/ $\sqrt{\text{Hz}}$  at f = 1KHz

## APPLICATIONS

- Cellular an Cordless Phones
- Active Filter and Buffers
- Laptops and PDAs
- Battery Powered Electronics

## Typical Application



**Figure 1. A Battery Powered Microphone Preamplifier**



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.



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**Absolute Maximum Ratings** <sup>(1)(2)</sup>

ESD Tolerance <sup>(3)</sup>	
Human Body Model	2000V
Machine Model	100V
Differential Input Voltage	± Supply Voltage
Supply Voltage ( $V^+ - V^-$ )	6V
Soldering Information	
Infrared or Convection (20 sec.)	235°C
Storage Temp. Range	-65°C to 150°C
Junction Temperature <sup>(4)</sup>	150°C

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical Characteristics.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (3) Human body model, 1.5 k $\Omega$  in series with 100 pF. Machine model, 200 $\Omega$  in series with 100 pF.
- (4) The maximum power dissipation is a function of  $T_{J(max)}$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any ambient temperature is  $P_D = (T_{J(max)} - T_A) / \theta_{JA}$ . All numbers apply for packages soldered directly into a PC board.

**Operating Ratings** <sup>(1)</sup>

Supply Voltage	2.2V to 5.5V
Temperature Range	-40°C $\leq T_J \leq$ 85°C
Thermal Resistance ( $\theta_{JA}$ )	
Silicon Dust SC70-5 Pkg	440°C/W
Tiny SOT-23 package	265 °C/W
SOIC package, 8-pin Surface Mount	190°C/W
VSSOP package, 8-Pin Mini Surface Mount	235 °C/W
SOIC package, 14-Pin Surface Mount	145°C/W

- (1) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of 30 mA over long term may adversely affect reliability.

**2.2V DC Electrical Characteristics**

Unless otherwise specified, all limits specified for  $T_J = 25^\circ\text{C}$ .  $V^+ = 2.2\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{CM} = V^+/2$ ,  $V_O = V^+/2$  and  $R_L > 1\text{M}\Omega$ .

**Boldface** limits apply at the temperature extremes.

Parameter		Test Conditions	Typ <sup>(1)</sup>	Limit <sup>(2)</sup>	Units
$V_{OS}$	Input Offset Voltage		0.02	<b>3</b> <b>3.5</b>	mV max
$TCV_{OS}$	Input Offset Voltage Average Drift		0.6		$\mu\text{V}/^\circ\text{C}$
$I_B$	Input Bias Current		260		nA
$I_{OS}$	Input Offset Current		25		nA
CMRR	Common Mode Rejection Ratio	$0\text{V} \leq V_{CM} \leq 1.3\text{V}$	88	<b>70</b> <b>64</b>	dB min
PSRR	Power Supply Rejection Ratio	$2.2\text{V} \leq V^+ \leq 5\text{V}$ , $V_O = 0$ , $V_{CM} = 0$	90	<b>70</b> <b>64</b>	dB min
$V_{CM}$	Input Common-Mode Voltage Range	For CMRR $\geq$ 50dB	-0.30		V
			1.3		V
$A_V$	Large Signal Voltage Gain	$R_L = 600\Omega$ $V_O = 0.75\text{V}$ to $2.00\text{V}$	81	<b>75</b> <b>60</b>	dB min
		$R_L = 2\text{k}\Omega$ $V_O = 0.50\text{V}$ to $2.10\text{V}$	84	<b>75</b> <b>60</b>	dB min

(1) Typical Values represent the most likely parametric norm.

(2) All limits are specified by testing or statistical analysis.

## 2.2V DC Electrical Characteristics (continued)

Unless otherwise specified, all limits specified for  $T_J = 25^\circ\text{C}$ .  $V^+ = 2.2\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{CM} = V^+/2$ ,  $V_O = V^+/2$  and  $R_L > 1\text{ M}\Omega$ .

**Boldface** limits apply at the temperature extremes.

Parameter		Test Conditions	Typ <sup>(1)</sup>	Limit <sup>(2)</sup>	Units
$V_O$	Output Swing	$R_L = 600\Omega$ to $V^+/2$	2.125	2.090 <b>2.065</b>	V min
			0.071	0.120 <b>0.145</b>	V max
		$R_L = 2\text{k}\Omega$ to $V^+/2$	2.177	2.150 <b>2.125</b>	V min
			0.056	0.080 <b>0.105</b>	V max
$I_O$	Output Current	Sourcing, $V_O = 0\text{V}$ $V_{IN}(\text{diff}) = \pm 0.5\text{V}$	14.9	10.0 <b>5.0</b>	mA min
		Sinking, $V_O = 2.2\text{V}$ $V_{IN}(\text{diff}) = \pm 0.5\text{V}$	17.6	10.0 <b>5.0</b>	mA min
$I_S$	Supply Current	LMV721-N	0.93	1.2 <b>1.5</b>	mA max
		LMV722	1.81	2.2 <b>2.6</b>	

## 2.2V AC Electrical Characteristics

Unless otherwise specified, all limits specified for  $T_J = 25^\circ\text{C}$ .  $V^+ = 2.2\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{CM} = V^+/2$ ,  $V_O = V^+/2$  and  $R_L > 1\text{ M}\Omega$ .

**Boldface** limits apply at the temperature extremes.

Parameter		Test Conditions	Typ <sup>(1)</sup>	Units
SR	Slew Rate	<sup>(2)</sup>	4.9	V/ $\mu\text{s}$
GBW	Gain-Bandwidth Product		10	MHz
$\Phi_m$	Phase Margin		67.4	Deg
$G_m$	Gain Margin		-9.8	dB
$e_n$	Input-Referred Voltage Noise	$f = 1\text{ kHz}$	9	nV/ $\sqrt{\text{Hz}}$
$i_n$	Input-Referred Current Noise	$f = 1\text{ kHz}$	0.3	pA/ $\sqrt{\text{Hz}}$
THD	Total Harmonic Distortion	$f = 1\text{ kHz}$ $A_V = 1$ $R_L = 600\Omega$ , $V_O = 500\text{ mV}_{PP}$	0.004	%

(1) Typical Values represent the most likely parametric norm.

(2) Connected as voltage follower with 1V step input. Number specified is the slower of the positive and negative slew rate.

## 5V DC Electrical Characteristics

Unless otherwise specified, all limits specified for  $T_J = 25^\circ\text{C}$ .  $V^+ = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{CM} = V^+/2$ ,  $V_O = V^+/2$  and  $R_L > 1\text{ M}\Omega$ .

**Boldface** limits apply at the temperature extremes.

Parameter		Test Conditions	Typ <sup>(1)</sup>	Limit <sup>(2)</sup>	Units
$V_{OS}$	Input Offset Voltage		-0.08	3 <b>3.5</b>	mV max
$TCV_{OS}$	Input Offset Voltage Average Drift		0.6		$\mu\text{V}/^\circ\text{C}$
$I_B$	Input Bias Current		260		nA
$I_{OS}$	Input Offset Current		25		nA
CMRR	Common Mode Rejection Ratio	$0\text{V} \leq V_{CM} \leq 4.1\text{V}$	89	70 <b>64</b>	dB min
PSRR	Power Supply Rejection Ratio	$2.2\text{V} \leq V^+ \leq 5.0\text{V}$ , $V_O = 0$ $V_{CM} = 0$	90	70 <b>64</b>	dB min
$V_{CM}$	Input Common-Mode Voltage Range	For CMRR $\geq 50\text{dB}$	-0.30		V
			4.1		V

(1) Typical Values represent the most likely parametric norm.

(2) All limits are specified by testing or statistical analysis.

## 5V DC Electrical Characteristics (continued)

Unless otherwise specified, all limits specified for  $T_J = 25^\circ\text{C}$ .  $V^+ = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{CM} = V^+/2$ ,  $V_O = V^+/2$  and  $R_L > 1\text{ M}\Omega$ .

**Boldface** limits apply at the temperature extremes.

Parameter		Test Conditions	Typ <sup>(1)</sup>	Limit <sup>(2)</sup>	Units
$A_V$	Large Signal Voltage Gain	$R_L = 600\Omega$ $V_O = 0.75\text{V to } 4.80\text{V}$	87	80 <b>70</b>	dB min
		$R_L = 2\text{k}\Omega$ , $V_O = 0.70\text{V to } 4.90\text{V}$ ,	94	85 <b>70</b>	dB min
$V_O$	Output Swing	$R_L = 600\Omega$ to $V^+/2$	4.882	4.840 <b>4.815</b>	V min
			0.134	0.190 <b>0.215</b>	V max
		$R_L = 2\text{k}\Omega$ to $V^+/2$	4.952	4.930 <b>4.905</b>	V min
			0.076	0.110 <b>0.135</b>	V max
$I_O$	Output Current	Sourcing, $V_O = 0\text{V}$ $V_{IN}(\text{diff}) = \pm 0.5\text{V}$	52.6	25.0 <b>12.0</b>	mA min
		Sinking, $V_O = 5\text{V}$ $V_{IN}(\text{diff}) = \pm 0.5\text{V}$	23.7	15.0 <b>8.5</b>	mA min
$I_S$	Supply Current	LMV721-N	1.03	1.4 <b>1.7</b>	mA max
		LMV722	2.01	2.4 <b>2.8</b>	

## 5V AC Electrical Characteristics

Unless otherwise specified, all limits specified for  $T_J = 25^\circ\text{C}$ .  $V^+ = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{CM} = V^+/2$ ,  $V_O = V^+/2$  and  $R_L > 1\text{ M}\Omega$ .

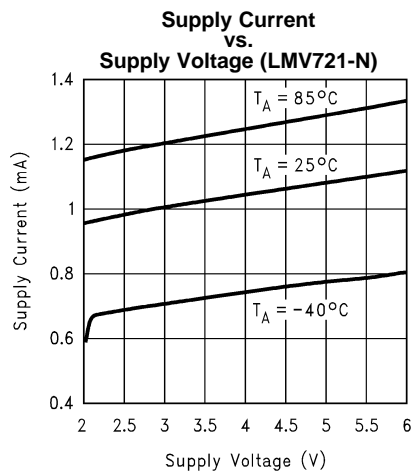
**Boldface** limits apply at the temperature extremes.

Parameter		Test Conditions	Typ <sup>(1)</sup>	Units
SR	Slew Rate	(2)	5.25	V/ $\mu\text{s}$
GBW	Gain-Bandwidth Product		10.0	MHz
$\Phi_m$	Phase Margin		72	Deg
$G_m$	Gain Margin		-11	dB
$e_n$	Input-Related Voltage Noise	$f = 1\text{ kHz}$	8.5	nV/ $\sqrt{\text{Hz}}$
$i_n$	Input-Referred Current Noise	$f = 1\text{ kHz}$	0.2	pa/ $\sqrt{\text{Hz}}$
THD	Total Harmonic Distortion	$f = 1\text{ kHz}$ , $A_V = 1$ $R_L = 600\Omega$ , $V_O = 1\text{ V}_{PP}$	0.001	%

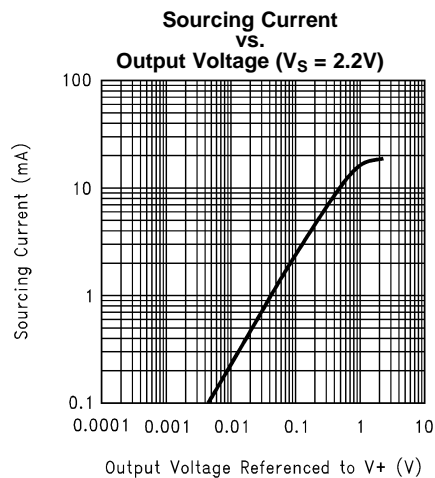
(1) Typical Values represent the most likely parametric norm.

(2) Connected as voltage follower with 1V step input. Number specified is the slower of the positive and negative slew rate.

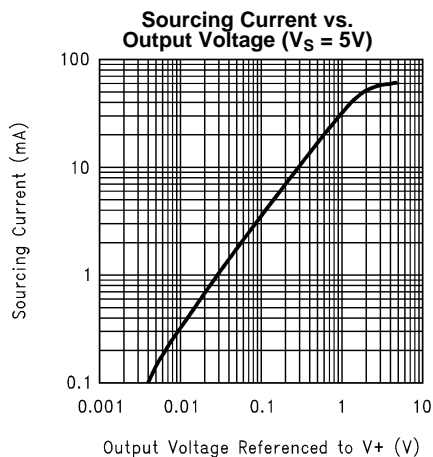
## Typical Performance Characteristics



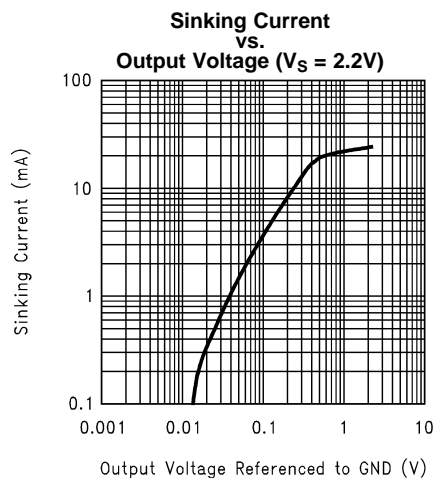
**Figure 2.**



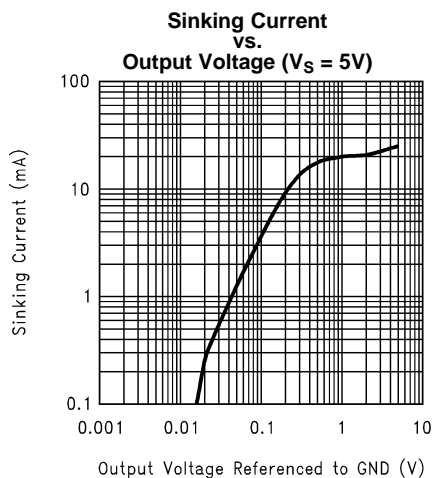
**Figure 3.**



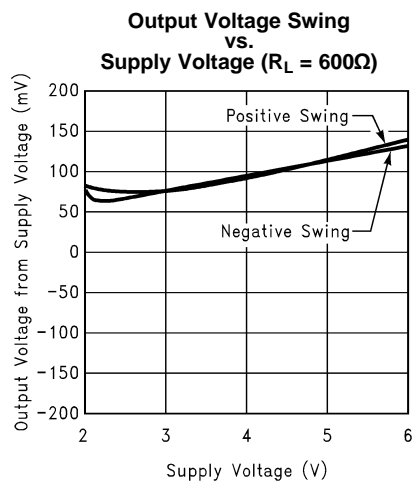
**Figure 4.**



**Figure 5.**

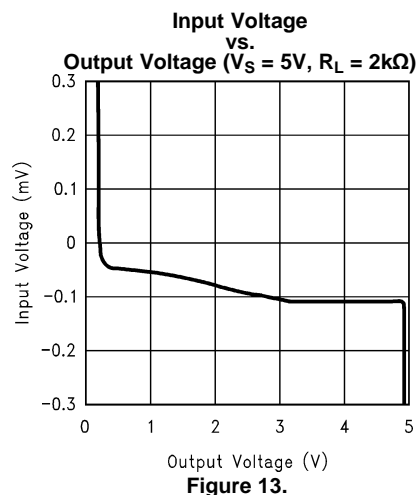
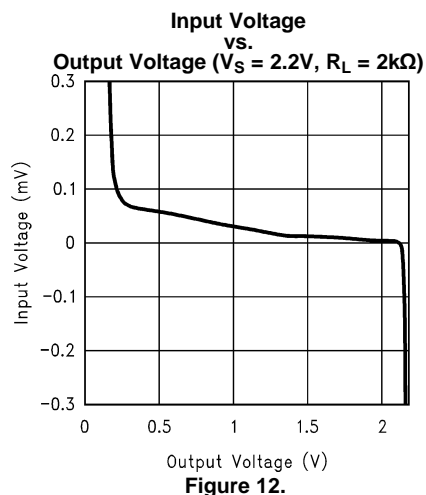
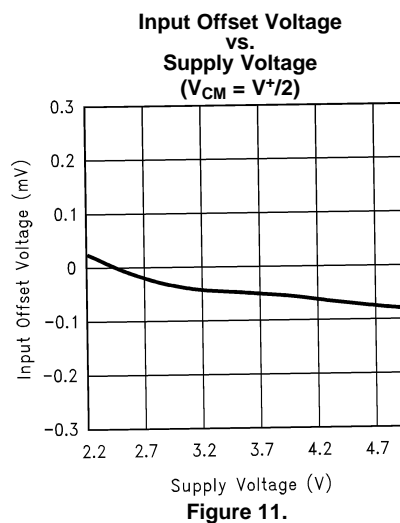
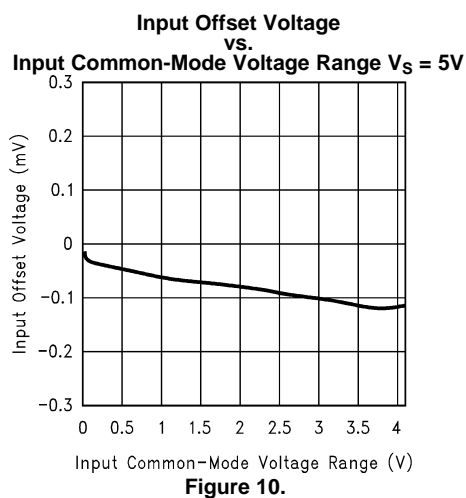
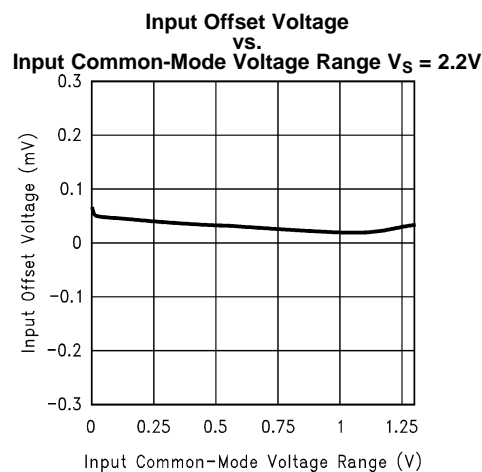
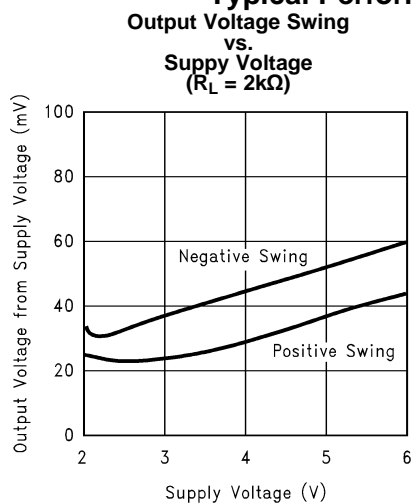


**Figure 6.**



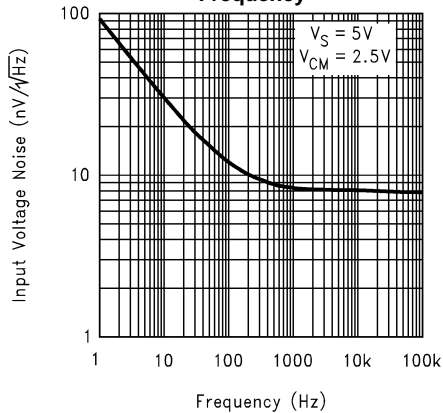
**Figure 7.**

## Typical Performance Characteristics (continued)



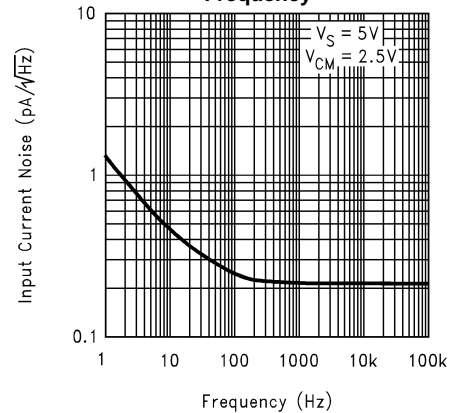
## Typical Performance Characteristics (continued)

**Input Voltage Noise  
vs.  
Frequency**



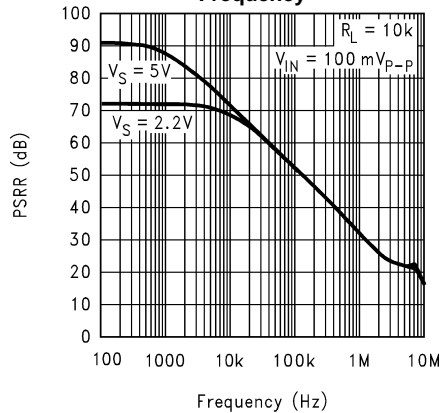
**Figure 14.**

**Input Current Noise  
vs.  
Frequency**



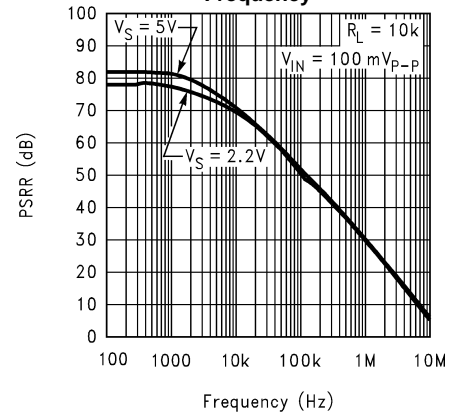
**Figure 15.**

**+PSRR  
vs.  
Frequency**



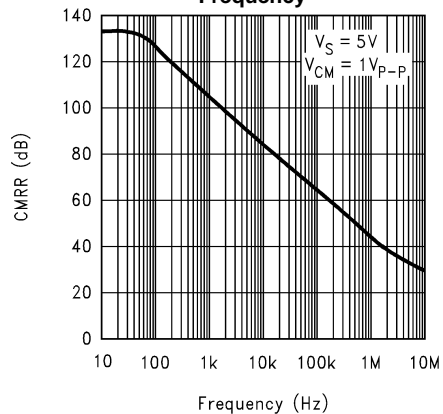
**Figure 16.**

**-PSRR  
vs.  
Frequency**



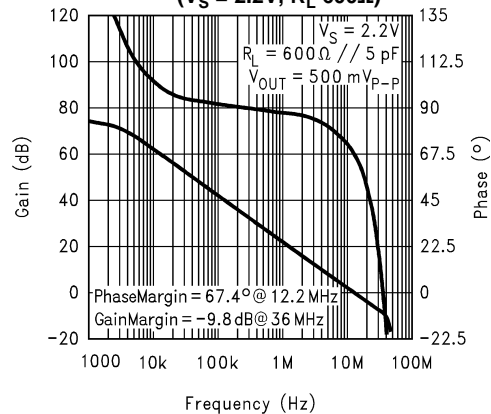
**Figure 17.**

**CMRR  
vs.  
Frequency**



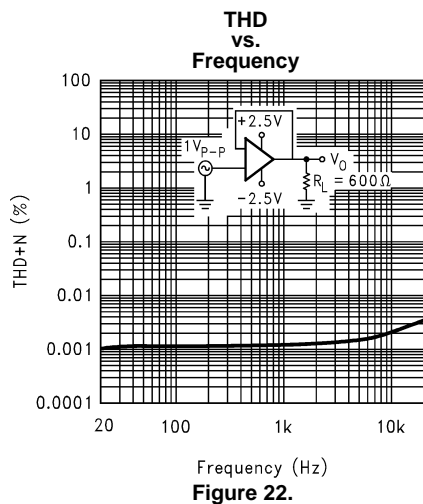
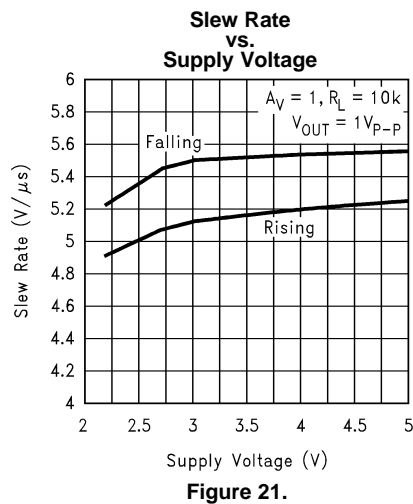
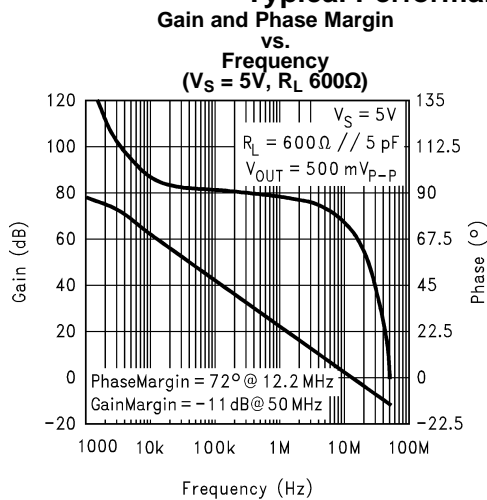
**Figure 18.**

**Gain and Phase Margin  
vs.  
Frequency  
( $V_S = 2.2V$ ,  $R_L = 600\Omega$ )**



**Figure 19.**

## Typical Performance Characteristics (continued)





## APPLICATION NOTES

### BENEFITS OF THE LMV721-N/722 SIZE

The small footprints of the LMV721-N/722 packages save space on printed circuit boards, and enable the design of smaller electronic products, such as cellular phones, pagers, or other portable systems. The low profile of the LMV721-N/722 make them possible to use in PCMCIA type III cards.

**Signal Integrity** Signals can pick up noise between the signal source and the amplifier. By using a physically smaller amplifier package, the LMV721-N/722 can be placed closer to the signal source, reducing noise pickup and increasing signal integrity.

**Simplified Board Layout** These products help you to avoid using long pc traces in your pc board layout. This means that no additional components, such as capacitors and resistors, are needed to filter out the unwanted signals due to the interference between the long pc traces.

**Low Supply Current** These devices will help you to maximize battery life. They are ideal for battery powered systems.

**Low Supply Voltage** TI provides ensured performance at 2.2V and 5V. These specifications ensure operation throughout the battery lifetime.

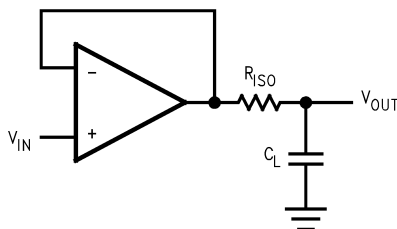
**Rail-to-Rail Output** Rail-to-rail output swing provides maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.

**Input Includes Ground** Allows direct sensing near GND in single supply operation.

Protection should be provided to prevent the input voltages from going negative more than  $-0.3\text{V}$  (at  $25^{\circ}\text{C}$ ). An input clamp diode with a resistor to the IC input terminal can be used.

### CAPACITIVE LOAD TOLERANCE

The LMV721-N/722 can directly drive 4700pF in unity-gain without oscillation. The unity-gain follower is the most sensitive configuration to capacitive loading. Direct capacitive loading reduces the phase margin of amplifiers. The combination of the amplifier's output impedance and the capacitive load induces phase lag. This results in either an underdamped pulse response or oscillation. To drive a heavier capacitive load, circuit in [Figure 23](#) can be used.



**Figure 23. Indirectly Driving A capacitive Load Using Resistive Isolation**

In [Figure 23](#), the isolation resistor  $R_{ISO}$  and the load capacitor  $C_L$  form a pole to increase stability by adding more phase margin to the overall system. the desired performance depends on the value of  $R_{ISO}$ . The bigger the  $R_{ISO}$  resistor value, the more stable  $V_{OUT}$  will be. [Figure 24](#) is an output waveform of [Figure 23](#) using  $100\text{k}\Omega$  for  $R_{ISO}$  and  $2000\mu\text{F}$  for  $C_L$ .

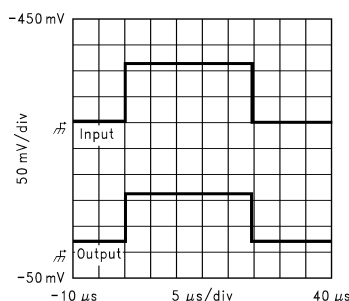


Figure 24. Pulse Response of the LMV721-N Circuit in Figure 23

The circuit in Figure 25 is an improvement to the one in Figure 23 because it provides DC accuracy as well as AC stability. If there were a load resistor in Figure 23, the output would be voltage divided by  $R_{ISO}$  and the load resistor. Instead, in Figure 25,  $R_F$  provides the DC accuracy by using feed-forward techniques to connect  $V_{IN}$  to  $R_L$ . Caution is needed in choosing the value of  $R_F$  due to the input bias current of the LMV721-N/722.  $C_F$  and  $R_{ISO}$  serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop. Increased capacitive drive is possible by increasing the value of  $C_F$ . This in turn will slow down the pulse response.

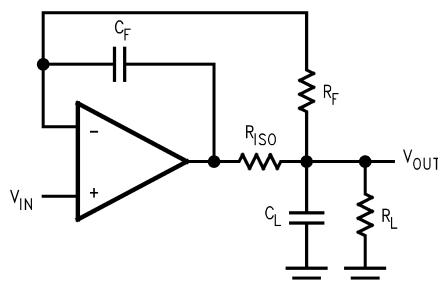


Figure 25. Indirectly Driving A Capacitive Load with DC Accuracy

## INPUT BIAS CURRENT CANCELLATION

The LMV721-N/722 family has a bipolar input stage. The typical input bias current of LMV721-N/722 is 260nA with 5V supply. Thus a 100kΩ input resistor will cause 26mV of error voltage. By balancing the resistor values at both inverting and non-inverting inputs, the error caused by the amplifier's input bias current will be reduced. The circuit in Figure 26 shows how to cancel the error caused by input bias current.

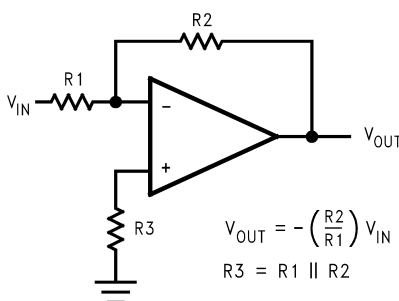
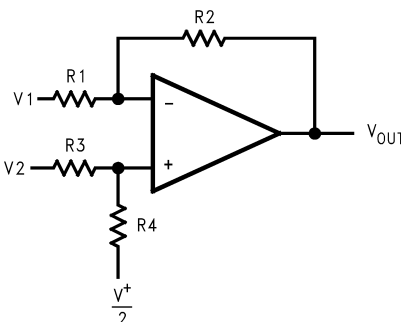


Figure 26. Cancelling the Error Caused by Input Bias Current

## TYPICAL SINGLE-SUPPLY APPLICATION CIRCUITS

### Difference Amplifier

The difference amplifier allows the subtraction of two voltages or, as a special case, the cancellation of a signal common to two inputs. It is useful as a computational amplifier, in making a differential to single-ended conversion or in rejecting a common mode signal.



**Figure 27. Difference Application**

$$V_{OUT} = \left( \frac{R1+R2}{R3+R4} \right) \frac{R4}{R1} V_2 - \frac{R2}{R1} V_1 + \left( \frac{R1+R2}{R3+R4} \right) \frac{R3}{R1} \cdot \frac{V^+}{2}$$

for  $R1 = R3$  and  $R2 = R4$

$$V_{OUT} = \frac{R2}{R1} (V_2 - V_1) + \frac{V^+}{2}$$

(1)

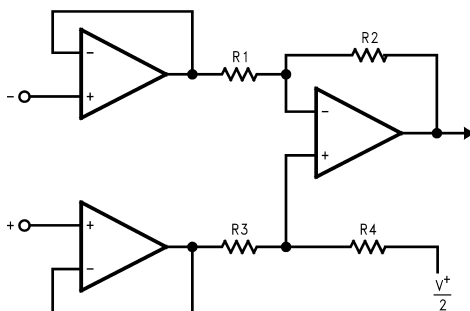
(2)

### Instrumentation Circuits

The input impedance of the previous difference amplifier is set by the resistor  $R_1$ ,  $R_2$ ,  $R_3$  and  $R_4$ . To eliminate the problems of low input impedance, one way is to use a voltage follower ahead of each input as shown in the following two instrumentation amplifiers.

#### Three-op-amp Instrumentation Amplifier

The LMV721-N/722 can be used to build a three-op-amp instrumentation amplifier as shown in [Figure 28](#)



**Figure 28. Three-op-amp Instrumentation Amplifier**

The first stage of this instrumentation amplifier is a differential-input, differential-output amplifier, with two voltage followers. These two voltage followers assure that the input impedance is over 100MΩ. The gain of this instrumentation amplifier is set by the ratio of  $R_2/R_1$ .  $R_3$  should equal  $R_1$  and  $R_4$  equal  $R_2$ . Matching of  $R_3$  to  $R_1$  and  $R_4$  to  $R_2$  affects the CMRR. For good CMRR over temperature, low drift resistors should be used. Making  $R_4$  slightly smaller than  $R_2$  and adding a trim pot equal to twice the difference between  $R_2$  and  $R_4$  will allow the CMRR to be adjusted for optimum.

## Two-op-amp Instrumentation Amplifier

A two-op-amp instrumentation amplifier can also be used to make a high-input impedance DC differential amplifier (Figure 29). As in the two-op-amp circuit, this instrumentation amplifier requires precise resistor matching for good CMRR.  $R_4$  should equal to  $R_1$  and  $R_3$  should equal  $R_2$ .

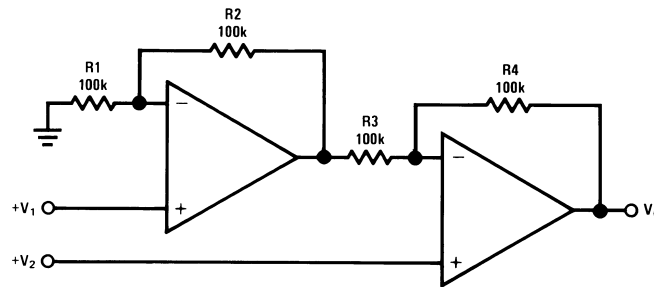


Figure 29. Two-op-amp Instrumentation Amplifier

$$V_O = \left(1 + \frac{R_4}{R_3}\right)(V_2 - V_1), \text{ where } R_1 = R_4 \text{ and } R_2 = R_3$$

$$\text{As shown: } V_O = 2(V_2 - V_1) \quad (3)$$

## Single-Supply Inverting Amplifier

There may be cases where the input signal going into the amplifier is negative. Because the amplifier is operating in single supply voltage, a voltage divider using  $R_3$  and  $R_4$  is implemented to bias the amplifier so the input signal is within the input common-common voltage range of the amplifier. The capacitor  $C_1$  is placed between the inverting input and resistor  $R_1$  to block the DC signal going into the AC signal source,  $V_{IN}$ . The values of  $R_1$  and  $C_1$  affect the cutoff frequency,  $f_c = \frac{1}{2\pi R_1 C_1}$ .

As a result, the output signal is centered around mid-supply (if the voltage divider provides  $V^+/2$  at the non-inverting input). The output can swing to both rails, maximizing the signal-to-noise ratio in a low voltage system.

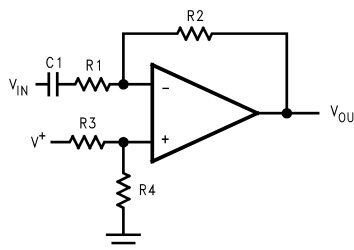


Figure 30. Single-Supply Inverting Amplifier

$$V_{OUT} = -\frac{R_2}{R_1} V_{IN} \quad (4)$$

## Active Filter

### Simple Low-Pass Active Filter

The simple low-pass filter is shown in Figure 31. Its low-pass frequency gain ( $\omega \rightarrow 0$ ) is defined by  $-R_3/R_1$ . This allows low-frequency gains other than unity to be obtained. The filter has a  $-20\text{dB/decade}$  roll-off after its corner frequency  $f_c$ .  $R_2$  should be chosen equal to the parallel combination of  $R_1$  and  $R_3$  to minimize error due to bias current. The frequency response of the filter is shown in Figure 32.

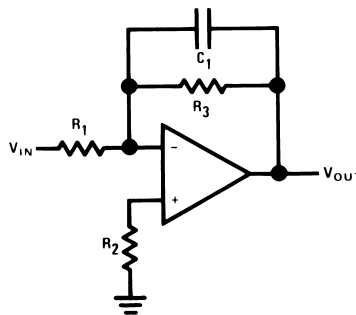


Figure 31. Simple Low-Pass Active Filter

$$A_L = -\frac{R_3}{R_1}$$

$$f_c = \frac{1}{2\pi R_3 C_1}$$

$$R_2 = R_1 \parallel R_3$$

(5)

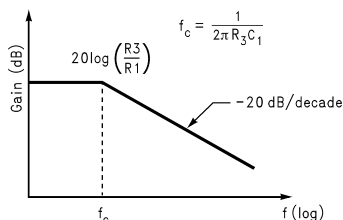


Figure 32. Frequency Response of Simple Low-pass Active Filter in Figure 31

Note that the single-op-amp active filters are used in to the applications that require low quality factor,  $Q(\leq 10)$ , low frequency ( $\leq 5\text{KHz}$ ), and low gain ( $\leq 10$ ), or a small value for the product of gain times  $Q(\leq 100)$ . The op amp should have an open loop voltage gain at the highest frequency of interest at least 50 times larger than the gain of the filter at this frequency. In addition, the selected op amp should have a slew rate that meets the following requirement:

$$\text{Slew Rate} \geq 0.5 \times (\omega_H V_{OPP}) \times 10^{-6} \text{V}/\mu\text{sec}$$

where

- $\omega_H$  is the highest frequency of interest
- $V_{OPP}$  is the output peak-to-peak voltage

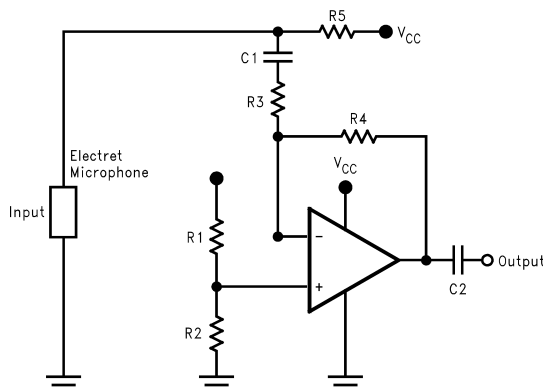
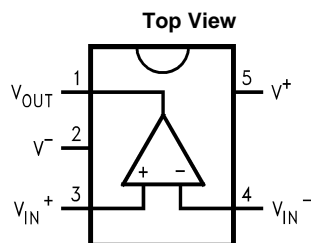


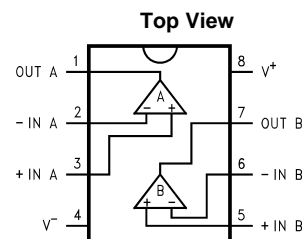
Figure 33. A Battery Powered Microphone Preamplifier

Here is a LMV721-N used as a microphone preamplifier. Since the LMV721-N is a low noise and low power op amp, it makes it an ideal candidate as a battery powered microphone preamplifier. The LMV721-N is connected in an inverting configuration. Resistors,  $R_1 = R_2 = 4.7\text{k}\Omega$ , sets the reference half way between  $V_{CC} = 3\text{V}$  and ground. Thus, this configures the op amp for single supply use. The gain of the preamplifier, which is 50 (34dB), is set by resistors  $R_3 = 10\text{k}\Omega$  and  $R_4 = 500\text{k}\Omega$ . The gain bandwidth product for the LMV721-N is 10 MHz. This is sufficient for most audio application since the audio range is typically from 20 Hz to 20kHz. A resistor  $R_5 = 5\text{k}\Omega$  is used to bias the electret microphone. Capacitors  $C_1 = C_2 = 4.7\mu\text{F}$  placed at the input and output of the op amp to block out the DC voltage offset.

## Connection Diagrams



**Figure 34. 5-Pin SC70 and SOT-23 Packages**  
See Package Numbers DCK0005A AND DBV0005A



**Figure 35. 8-Pin SOIC and VSSOP Packages**  
See Package Numbers D0008A and DGK0008A

## REVISION HISTORY

### Changes from Revision G (March 2013) to Revision H

### Page

- Changed layout of National Data Sheet to TI format ..... [14](#)

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV721M5	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 85	A30A	
LMV721M5/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A30A	<a href="#">Samples</a>
LMV721M5X/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A30A	<a href="#">Samples</a>
LMV721M7	NRND	SC70	DCK	5	1000	TBD	Call TI	Call TI	-40 to 85	A20	
LMV721M7/NOPB	ACTIVE	SC70	DCK	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A20	<a href="#">Samples</a>
LMV721M7X	NRND	SC70	DCK	5	3000	TBD	Call TI	Call TI	-40 to 85	A20	
LMV721M7X/NOPB	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A20	<a href="#">Samples</a>
LMV722M	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 85	LMV 722M	
LMV722M/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMV 722M	<a href="#">Samples</a>
LMV722MM	NRND	VSSOP	DGK	8	1000	TBD	Call TI	Call TI	-40 to 85	V722	
LMV722MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	V722	<a href="#">Samples</a>
LMV722MMX	NRND	VSSOP	DGK	8	3500	TBD	Call TI	Call TI	-40 to 85	V722	
LMV722MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	V722	<a href="#">Samples</a>
LMV722MX	NRND	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 85	LMV 722M	
LMV722MX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LMV 722M	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.



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**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV721M5	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV721M5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV721M5X/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV721M7	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV721M7/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV721M7X	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV721M7X/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV722MM	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV722MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV722MMX	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV722MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV722MX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMV722MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV721M5	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMV721M5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMV721M5X/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMV721M7	SC70	DCK	5	1000	210.0	185.0	35.0
LMV721M7/NOPB	SC70	DCK	5	1000	210.0	185.0	35.0
LMV721M7X	SC70	DCK	5	3000	210.0	185.0	35.0
LMV721M7X/NOPB	SC70	DCK	5	3000	210.0	185.0	35.0
LMV722MM	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMV722MM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LMV722MMX	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMV722MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMV722MX	SOIC	D	8	2500	367.0	367.0	35.0
LMV722MX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

## DCK (R-PDSO-G5)

## PLASTIC SMALL-OUTLINE PACKAGE



4093553-3/G 01/2007

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - Falls within JEDEC MO-203 variation AA.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



4073329/E 05/06

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
  - E. Falls within JEDEC MO-187 variation AA, except interlead flash.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



## NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.



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