

## LMH6574 4:1 High Speed Video Multiplexer

Check for Samples: [LMH6574](#)

### FEATURES

- 500 MHz, 500 mV –3 dB Bandwidth,  $A_V = 2$
- 400 MHz, 2V<sub>PP</sub> –3 dB Bandwidth,  $A_V = 2$
- 8 ns Channel Switching Time
- 70 dB Channel to Channel Isolation @ 10 MHz
- 0.02%, 0.05° Diff. Gain, Phase
- 0.1 dB Gain Flatness to 150 MHz
- 2200 V/μs Slew Rate
- Wide Supply Voltage Range: 6V (±3V) to 12V (±6V)
- -68 dB HD2 @ 5 MHz
- -84 dB HD3 @ 5 MHz

### APPLICATIONS

- Video Router
- Multi Input Video Monitor
- Instrumentation/Test Equipment
- Receiver IF Diversity Switch
- Multi Channel A/D Driver
- Picture in Picture Video Switch

### DESCRIPTION

The LMH™ 6574 is a high performance analog multiplexer optimized for professional grade video and other high fidelity high bandwidth analog applications. The output amplifier selects any one of four buffered input signals based on the state of the two address bits. The LMH6574 provides a 400 MHz bandwidth at 2 V<sub>PP</sub> output signal levels. Multimedia and high definition television (HDTV) applications can benefit from the LMH6574's 0.1 dB bandwidth of 150 MHz and its 2200 V/μs slew rate.

The LMH6574 supports composite video applications with its 0.02% and 0.05° differential gain and phase errors for NTSC and PAL video signals while driving a single, back terminated 75Ω load. An 80 mA linear output current is available for driving multiple video load applications.

The LMH6574 gain is set by external feedback and gain set resistors for maximum flexibility.

The LMH6574 is available in the 14 pin SOIC package.

### Connection Diagram

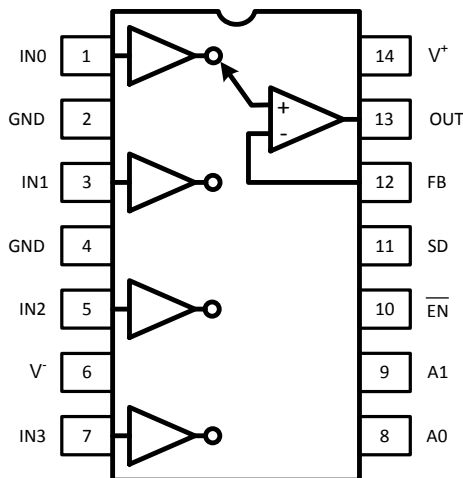


Figure 1. 14-Pin SOIC (Top View)



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**Truth Table**

| A1 | A0 | $\overline{\text{EN}}$ | SD | OUT      |
|----|----|------------------------|----|----------|
| 1  | 1  | 0                      | 0  | CH 3     |
| 1  | 0  | 0                      | 0  | CH2      |
| 0  | 1  | 0                      | 0  | CH1      |
| 0  | 0  | 0                      | 0  | CH 0     |
| X  | X  | 1                      | 0  | Disable  |
| X  | X  | X                      | 1  | Shutdown |



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

**Absolute Maximum Ratings<sup>(1)(2)</sup>**

|                                  |                                 |                 |
|----------------------------------|---------------------------------|-----------------|
| ESD Tolerance <sup>(3)</sup>     | Human Body Model                | 2000V           |
|                                  | Machine Model                   | 200V            |
| Supply Voltage ( $V^+ - V^-$ )   |                                 | 13.2V           |
| $I_{OUT}^{(4)}$                  |                                 | 130 mA          |
| Signal & Logic Input Pin Voltage |                                 | $\pm(V_S+0.6V)$ |
| Signal & Logic Input Pin Current |                                 | $\pm 20$ mA     |
| Maximum Junction Temperature     |                                 | +150°C          |
| Storage Temperature Range        |                                 | -65°C to +150°C |
| Soldering Information            | Infrared or Convection (20 sec) | 235 °C          |
|                                  | Wave Soldering (10 sec)         | 260 °C          |

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications, see the [Electrical Characteristics](#) tables.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
- (3) Human Body model, 1.5 k $\Omega$  in series with 100 pF. Machine model, 0 $\Omega$  In series with 200 pF.
- (4) The maximum output current ( $I_{OUT}$ ) is determined by the device power dissipation limitations (The junction temperature cannot be allowed to exceed 150°C). See the [POWER DISSIPATION](#) section for more details. A short circuit condition should be limited to 5 seconds or less.

**Operating Ratings<sup>(1)</sup>**

|                           |             |                   |                 |
|---------------------------|-------------|-------------------|-----------------|
| Operating Temperature     |             |                   | -40 °C to 85 °C |
| Supply Voltage Range      |             |                   | 6V to 12V       |
| <b>Thermal Resistance</b> |             |                   |                 |
| Package                   | 14-Pin SOIC | ( $\theta_{JA}$ ) | 130°C/W         |
|                           |             | ( $\theta_{JC}$ ) | 40°C/W          |

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications, see the [Electrical Characteristics](#) tables.

## ±5V Electrical Characteristics

$V_S = \pm 5V$ ,  $R_L = 100\Omega$ ,  $A_V = 2 V/V$ ,  $R_F = 575 \Omega$ ,  $T_J = 25^\circ C$ , Unless otherwise specified. **Bold** numbers specify limits at temperature extremes.

| Symbol                              | Parameter                                      | Conditions <sup>(1)</sup>                                     | Min                 | Typ         | Max  | Units            |
|-------------------------------------|--|---|---------------------|-------------|--|------------------|
| <b>Frequency Domain Performance</b> |  |   |                     |             |  |                  |
| SSBW                                | –3 dB Bandwidth                                | $V_{OUT} = 0.5 V_{PP}$  |                     | 500         |  | MHz              |
| LSBW                                | –3 dB Bandwidth                                | $V_{OUT} = 2 V_{PP}$  |                     | 400         |  | MHz              |
| .1 dBBW                             | 0.1 dB Bandwidth                               | $V_{OUT} = 0.25 V_{PP}$                                       |                     | 150         |  | MHz              |
| DG                                  | Differential Gain                              | $R_L = 150\Omega$ , $f = 4.43 \text{ MHz}$                    |                     | 0.02        |  | %                |
| DP                                  | Differential Phase                             | $R_L = 150\Omega$ , $f = 4.43 \text{ MHz}$                    |                     | 0.05        |  | deg              |
| XTLK                                | Channel to Channel Crosstalk                   | All Hostile, 5 MHz  |                     | –85         |  | dB               |
| <b>Time Domain Response</b>         |  |   |                     |             |  |                  |
| TRS                                 | Channel to Channel Switching Time              | Logic Transition to 90% Output                                |                     | 8           |  | ns               |
|                                     | Enable and Disable Times                       | Logic Transition to 90% or 10% Output                         |                     | 10          |  | ns               |
| TRL                                 | Rise and Fall Time                             | 4V Step   |                     | 2.4         |  | ns               |
| TSS                                 | Settling Time to 0.05%                         | 2V Step   |                     | 17          |  | ns               |
| OS                                  | Overshoot                                      | 2V Step   |                     | 5           |  | %                |
| SR                                  | Slew Rate                                      | 4V Step   |                     | 2200        |  | V/ $\mu s$       |
| <b>Distortion</b>                   |  |   |                     |             |  |                  |
| HD2                                 | 2 <sup>nd</sup> Harmonic Distortion            | $2 V_{PP}$ , 5 MHz  |                     | –68         |  | dBc              |
| HD3                                 | 3 <sup>rd</sup> Harmonic Distortion            | $2 V_{PP}$ , 5 MHz  |                     | –84         |  | dBc              |
| IMD                                 | 3 <sup>rd</sup> Order Intermodulation Products | 10 MHz, Two Tones $2 V_{PP}$ at Output                        |                     | –80         |  | dBc              |
| <b>Equivalent Input Noise</b>       |  |   |                     |             |  |                  |
| VN                                  | Voltage  | >1 MHz, Input Referred  |                     | 5           |  | $nV/\sqrt{Hz}$   |
| ICN                                 | Current  | >1 MHz, Input Referred  |                     | 5           |  | $pA/\sqrt{Hz}$   |
| <b>Static, DC Performance</b>       |  |   |                     |             |  |                  |
| CHGM                                | Channel to Channel Gain Difference             | DC, Difference in Gain Between Channels                       |                     | $\pm 0.005$ | $\pm 0.032$<br><b><math>\pm 0.035</math></b> | %                |
| VIO                                 | Input Offset Voltage <sup>(2)</sup>            | $V_{IN} = 0V$   |                     | 1           | $\pm 20$<br><b><math>\pm 25</math></b>       | mV               |
| DVIO                                | Offset Voltage Drift                           |   |                     | 30          |  | $\mu V/^\circ C$ |
| IBN                                 | Input Bias Current <sup>(2)(3)</sup>           | $V_{IN} = 0V$   |                     | –3          | $\pm 5$<br><b><math>\pm 5.6</math></b>       | $\mu A$          |
| DIBN                                | Bias Current Drift                             |   |                     | 11          |  | $nA/^\circ C$    |
|                                     | Inverting Input Bias Current                   | Pin 12, Feedback Point,<br>$V_{IN} = 0V$                      |                     | –7          | $\pm 10$<br><b><math>\pm 13</math></b>       |                  |
| PSRR                                | Power Supply Rejection Ratio <sup>(2)</sup>    | DC, Input Referred  | 47<br><b>45</b>     | 54          |  | dB               |
| ICC                                 | Supply Current <sup>(2)</sup>                  | No Load   |                     | 13          | 16<br><b>18</b>                              | mA               |
|                                     | Supply Current Disabled <sup>(2)</sup>         | $\overline{ENABLE} > 2V$                                      |                     | 4.7         | 5.8<br><b>5.9</b>                            | mA               |
|                                     | Supply Current Shutdown                        | SHUTDOWN > 2V   |                     | 1.8         | 2.5<br><b>2.6</b>                            | mA               |
| VIH                                 | Logic High Threshold <sup>(2)</sup>            | Select & Enable Pins (SD & $\overline{EN}$ )                  | 2.0                 |             |  | V                |
| VIL                                 | Logic Low Threshold <sup>(2)</sup>             | Select & Enable Pins (SD & $\overline{EN}$ )                  |                     |             | 0.8  | V                |
| IiL                                 | Logic Pin Input Current Low <sup>(3)</sup>     | Logic Input = 0V Select & Enable Pins (SD & $\overline{EN}$ ) | –2.9<br><b>–8.5</b> | –1          |  | $\mu A$          |

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that  $T_J = T_A$ . No ensure of parametric performance is indicated in the electrical tables under conditions of internal self heating where  $T_J > T_A$ . See [Application Notes](#) for information on temperature de-rating of this device. Min/Max ratings are based on product testing, characterization and simulation. Individual parameters are tested as noted.

(2) Parameters ensured by electrical testing at 25°C.

(3) Positive Value is current into device.

**±5V Electrical Characteristics (continued)**

$V_S = \pm 5V$ ,  $R_L = 100\Omega$ ,  $A_V = 2\text{ V/V}$ ,  $R_F = 575\Omega$ ,  $T_J = 25^\circ\text{C}$ , Unless otherwise specified. **Bold** numbers specify limits at temperature extremes.

| Symbol                           | Parameter                                   | Conditions <sup>(1)</sup>                               | Min  | Typ       | Max               | Units         |
|----------------------------------|---|---|--|-----------|-------------------|---------------|
| IiH                              | Logic Pin Input Current High <sup>(3)</sup> | Logic Input = 2.0V, Select & Enable Pins (SD & EN)      |  | 47        | 68<br><b>72.5</b> | $\mu\text{A}$ |
| <b>Miscellaneous Performance</b> |   |   |  |           |                   |               |
| RIN+                             | Input Resistance                            |   |  | 5         |                   | k $\Omega$    |
| CIN                              | Input Capacitance                           |   |  | 0.8       |                   | pF            |
| ROUT                             | Output Resistance                           | Output Active, ( $\overline{\text{EN}}$ and SD < 0.8 V) |  | 0.04      |                   | $\Omega$      |
| ROUT                             | Output Resistance                           | Output Disabled, ( $\overline{\text{EN}}$ or SD > 2V)   |  | 3000      |                   | $\Omega$      |
| COU                              | Output Capacitance                          | Output Disabled, ( $\overline{\text{EN}}$ or SD > 2V)   |  | 3.1       |                   | pF            |
| VO                               | Output Voltage Range                        | No Load   | $\pm 3.54$<br><b><math>\pm 3.53</math></b> | $\pm 3.7$ |                   | V             |
| VOL                              |   | $R_L = 100\Omega$                                       | $\pm 3.18$<br><b><math>\pm 3.17</math></b> | $\pm 3.5$ |                   | V             |
| CMIR                             | Input Voltage Range                         |   | $\pm 2.5$                                  | $\pm 2.6$ |                   | V             |
| IO                               | Linear Output Current <sup>(2)(3)</sup>     | $V_{IN} = 0V$   | +60<br>-70<br><b>+50</b><br><b>-60</b>     | $\pm 80$  |                   | mA            |
| ISC                              | Short Circuit Current <sup>(4)</sup>        | $V_{IN} = \pm 2V$ , Output Shorted to Ground            |  | $\pm 230$ |                   | mA            |

- (4) The maximum output current ( $I_{OUT}$ ) is determined by the device power dissipation limitations (The junction temperature cannot be allowed to exceed  $150^\circ\text{C}$ ). See the [POWER DISSIPATION](#) section for more details. A short circuit condition should be limited to 5 seconds or less.

### ±3.3V Electrical Characteristics

 $V_S = \pm 3.3V$ ,  $R_L = 100\Omega$ ,  $A_V = 2\text{ V/V}$ ,  $R_F = 575\Omega$ ; Unless otherwise specified.

| Symbol                              | Parameter                           | Conditions <sup>(1)</sup>                    | Min | Typ       | Max | Units      |
|-------------------------------------|-------------------------------------|--|-----|-----------|-----|------------|
| <b>Frequency Domain Performance</b> |                                     |  |     |           |     |            |
| SSBW                                | –3 dB Bandwidth                     | $V_{OUT} = 0.5\text{ V}_{PP}$                |     | 475       |     | MHz        |
| LSBW                                | –3 dB Bandwidth                     | $V_{OUT} = 2.0\text{ V}_{PP}$                |     | 375       |     | MHz        |
| 0.1 dBBW                            | 0.1 dB Bandwidth                    | $V_{OUT} = 0.5\text{ V}_{PP}$                |     | 100       |     | MHz        |
| GFP                                 | Peaking                             | DC to 200 MHz                                |     | 0.4       |     | dB         |
| XTLK                                | Channel to Channel Crosstalk        | All Hostile, $f = 5\text{ MHz}$              |     | –85       |     | dBc        |
| <b>Time Domain Response</b>         |                                     |  |     |           |     |            |
| TRL                                 | Rise and Fall Time                  | 2V Step                                      |     | 2         |     | ns         |
| TSS                                 | Settling Time to 0.05%              | 2V Step                                      |     | 20        |     | ns         |
| OS                                  | Overshoot                           | 2V Step                                      |     | 5         |     | %          |
| SR                                  | Slew Rate                           | 2V Step                                      |     | 1400      |     | V/ $\mu$ s |
| <b>Distortion</b>                   |                                     |  |     |           |     |            |
| HD2                                 | 2 <sup>nd</sup> Harmonic Distortion | 2 $V_{PP}$ , 10 MHz                          |     | –67       |     | dBc        |
| HD3                                 | 3 <sup>rd</sup> Harmonic Distortion | 2 $V_{PP}$ , 10 MHz                          |     | –87       |     | dBc        |
| <b>Static, DC Performance</b>       |                                     |  |     |           |     |            |
| VIO                                 | Input Offset Voltage                | $V_{IN} = 0V$                                |     | –5        |     | mV         |
| IBN                                 | Input Bias Current <sup>(2)</sup>   | $V_{IN} = 0V$                                |     | –3        |     | $\mu$ A    |
| PSRR                                | Power Supply Rejection Ratio        | DC, Input Referred                           |     | 49        |     | dB         |
| ICC                                 | Supply Current                      | No Load                                      |     | 12        |     | mA         |
| VIH                                 | Logic High Threshold                | Select & Enable Pins (SD & $\overline{EN}$ ) | 1.3 |           |     | V          |
| VIL                                 | Logic Low Threshold                 | Select & Enable Pins (SD & $\overline{EN}$ ) |     |           | 0.4 | V          |
| <b>Miscellaneous Performance</b>    |                                     |  |     |           |     |            |
| RIN+                                | Input Resistance                    |  |     | 5         |     | k $\Omega$ |
| CIN                                 | Input Capacitance                   |  |     | 0.8       |     | pF         |
| ROUT                                | Output Resistance                   |  |     | 0.06      |     | $\Omega$   |
| VO                                  | Output Voltage Range                | No Load                                      |     | $\pm 2$   |     | V          |
| VOL                                 |                                     | $R_L = 100\Omega$                            |     | $\pm 1.8$ |     | V          |
| CMIR                                | Input Voltage Range                 |  |     | $\pm 1.2$ |     | V          |
| IO                                  | Linear Output Current               | $V_{IN} = 0V$                                |     | $\pm 60$  |     | mA         |
| ISC                                 | Short Circuit Current               | $V_{IN} = \pm 1V$ , Output Shorted to Ground |     | $\pm 150$ |     | mA         |

- (1) Electrical Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that  $T_J = T_A$ . No ensure of parametric performance is indicated in the electrical tables under conditions of internal self heating where  $T_J > T_A$ . See [Application Notes](#) for information on temperature de-rating of this device. Min/Max ratings are based on product testing, characterization and simulation. Individual parameters are tested as noted.
- (2) Positive Value is current into device.

## Typical Performance Characteristics

$V_S = \pm 5V$ ,  $R_L = 100\Omega$ ,  $A_V = 2$ ,  $R_F = R_G = 575\Omega$ ; unless otherwise specified.

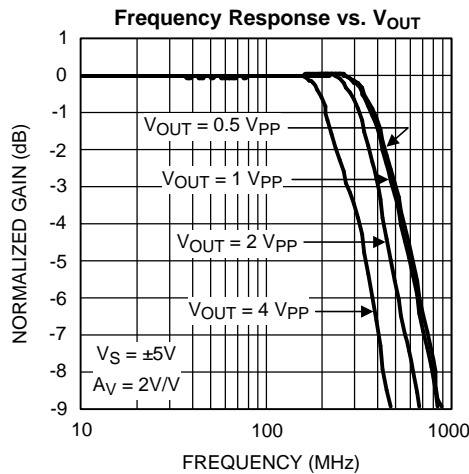


Figure 2.

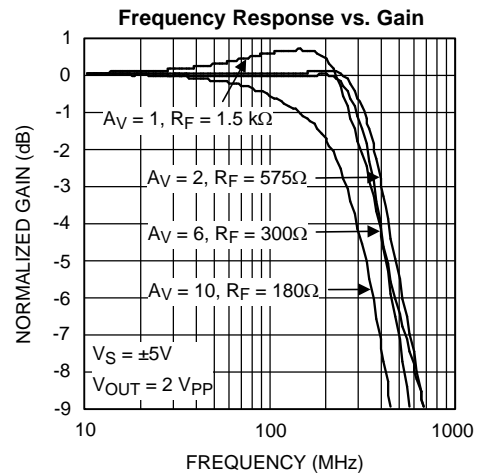


Figure 3.

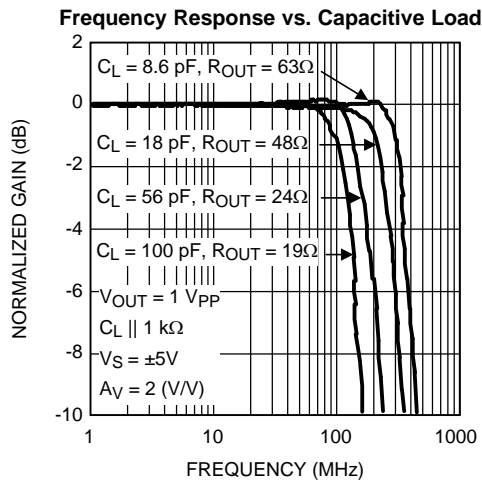


Figure 4.

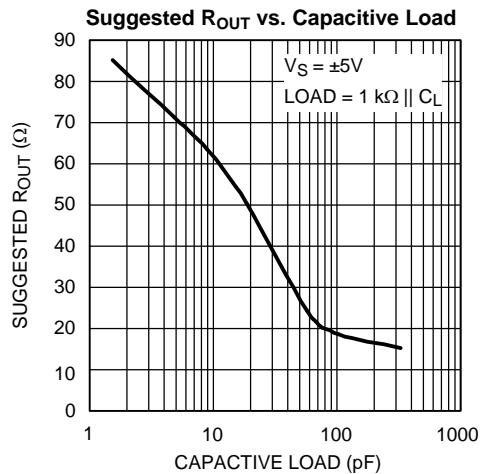


Figure 5.

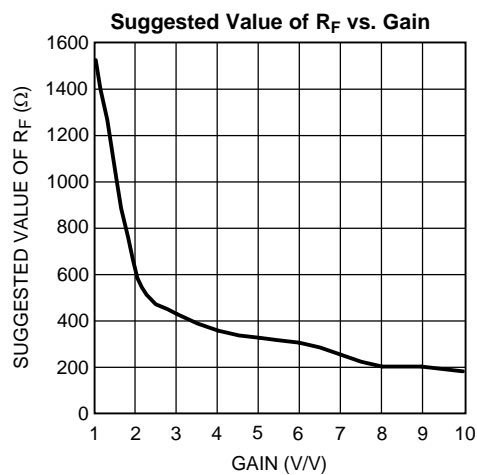


Figure 6.

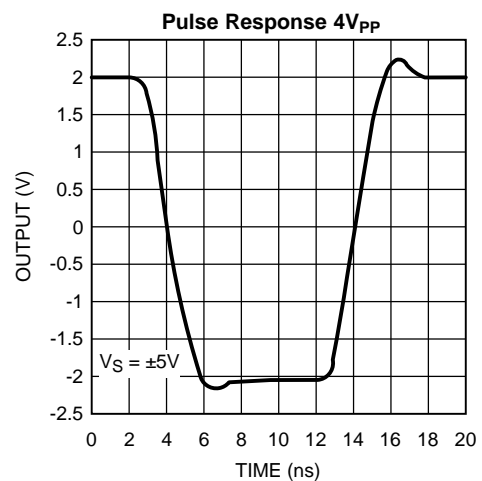


Figure 7.

## Typical Performance Characteristics (continued)

$V_S = \pm 5V$ ,  $R_L = 100\Omega$ ,  $A_V = 2$ ,  $R_F = R_G = 575\Omega$ ; unless otherwise specified.

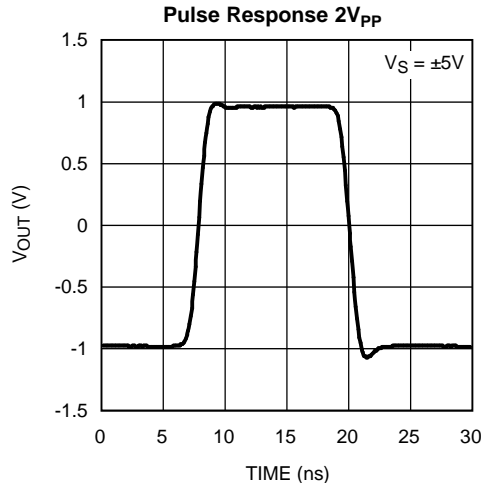


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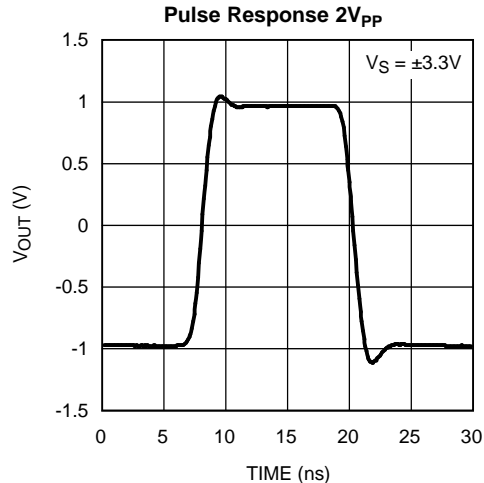


Figure 9.

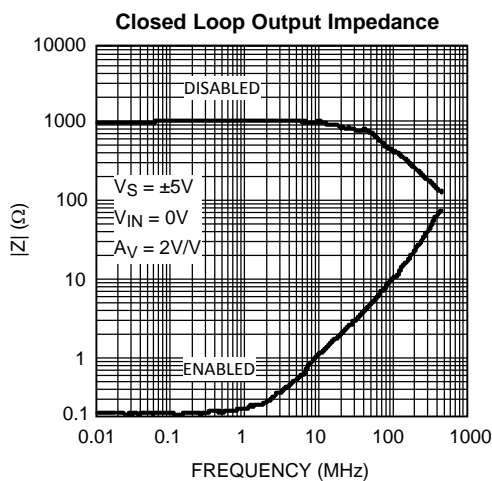


Figure 10.

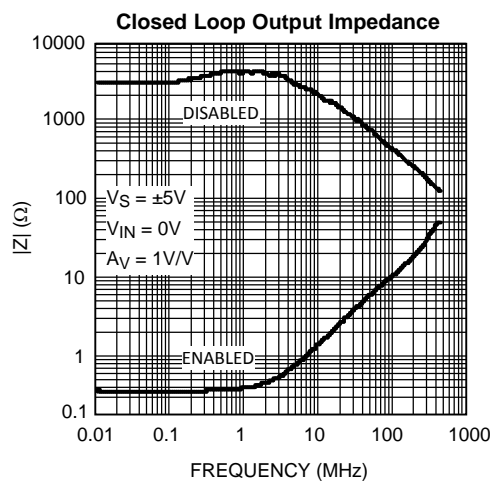


Figure 11.

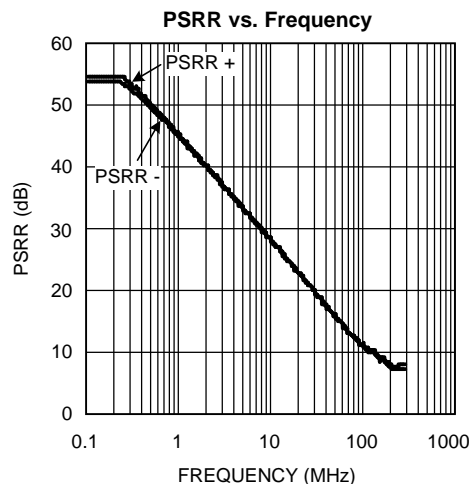


Figure 12.

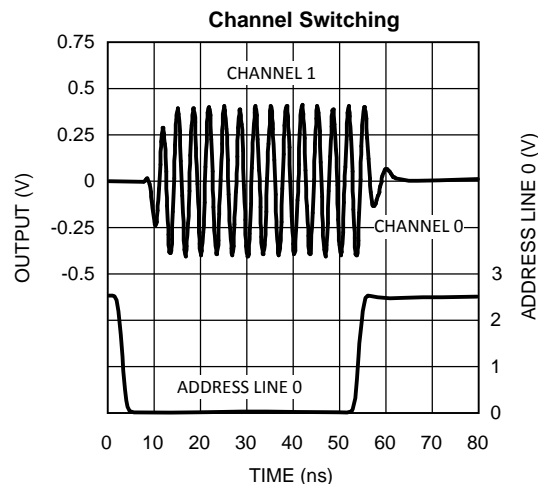


Figure 13.

### Typical Performance Characteristics (continued)

$V_s = \pm 5V$ ,  $R_L = 100\Omega$ ,  $A_V = 2$ ,  $R_F = R_G = 575\Omega$ ; unless otherwise specified.

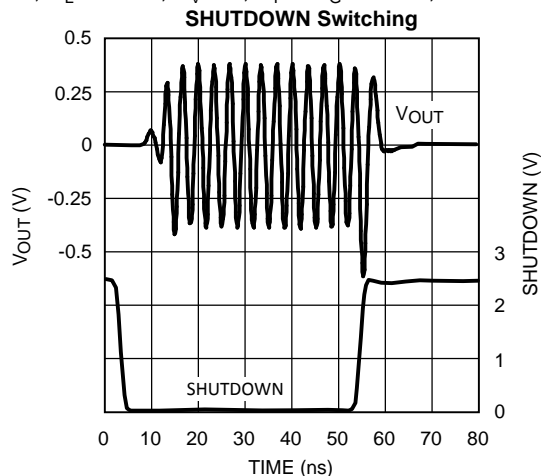


Figure 14.

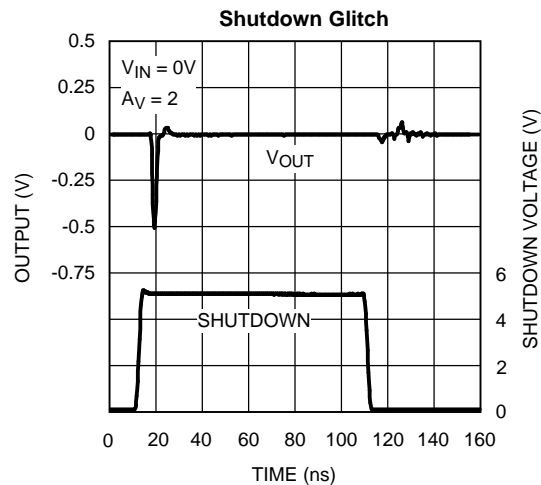


Figure 15.

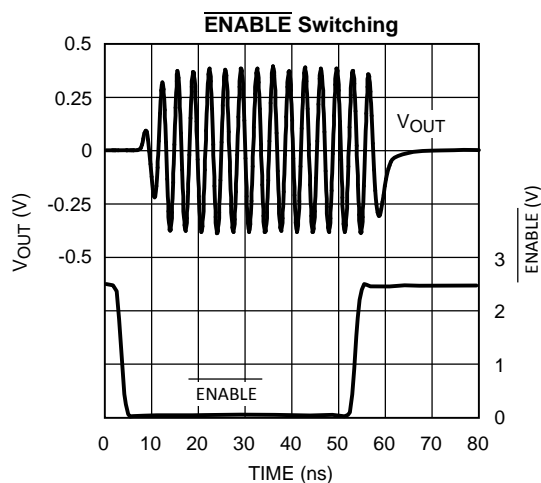


Figure 16.

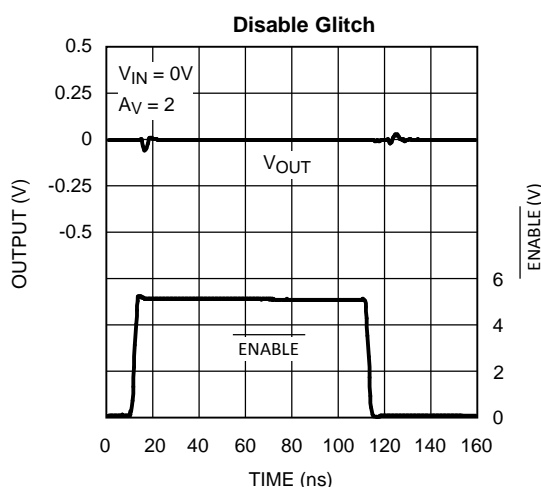


Figure 17.

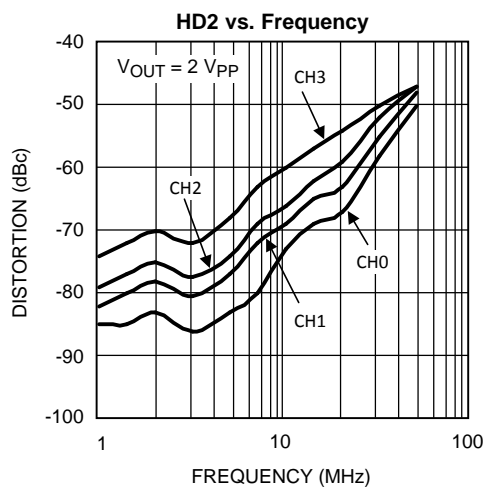


Figure 18.

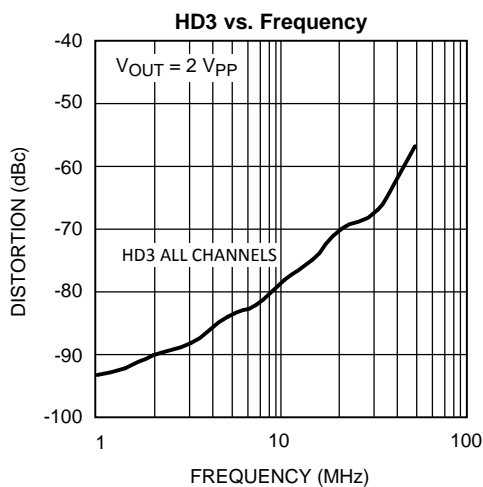


Figure 19.



## Typical Performance Characteristics (continued)

$V_s = \pm 5V$ ,  $R_L = 100\Omega$ ,  $A_V = 2$ ,  $R_F = R_G = 575\Omega$ ; unless otherwise specified.

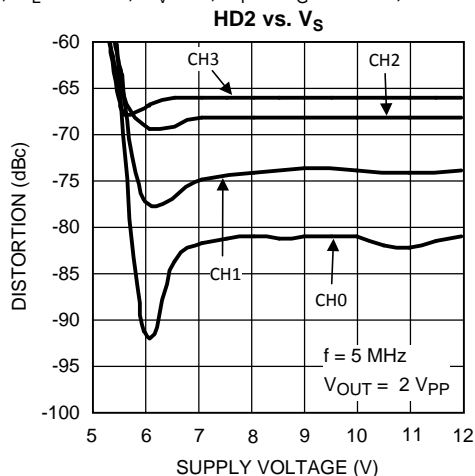


Figure 20.

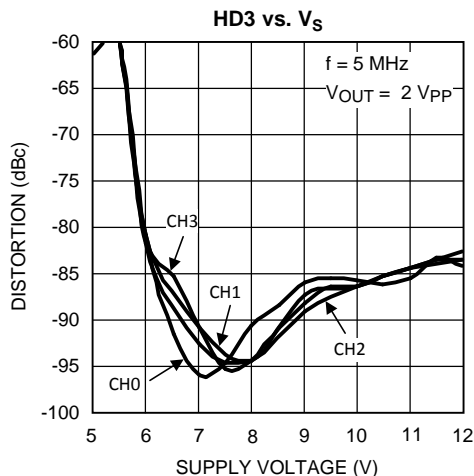


Figure 21.

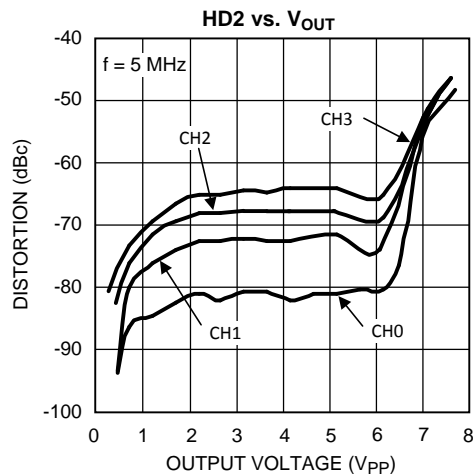


Figure 22.

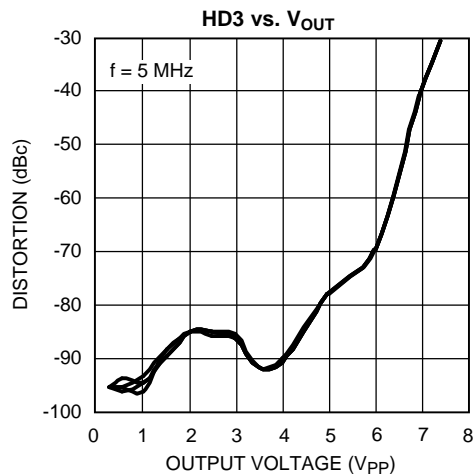


Figure 23.

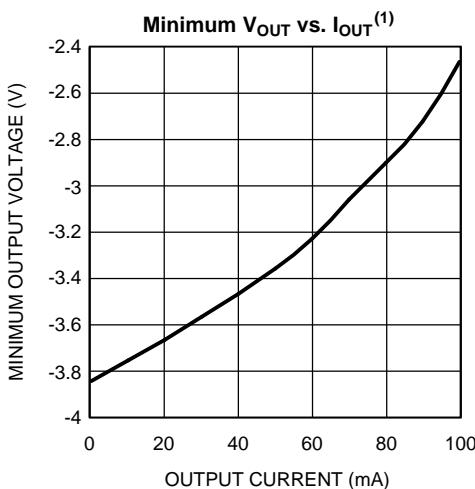


Figure 24.

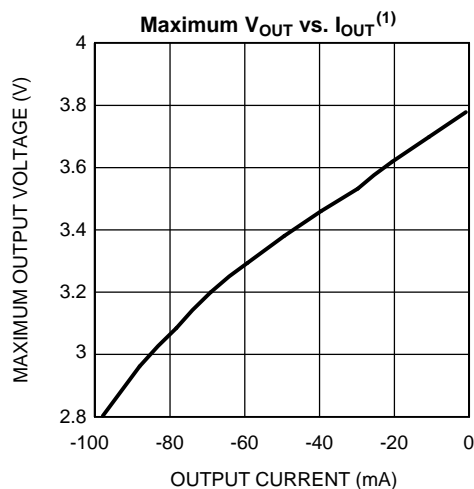
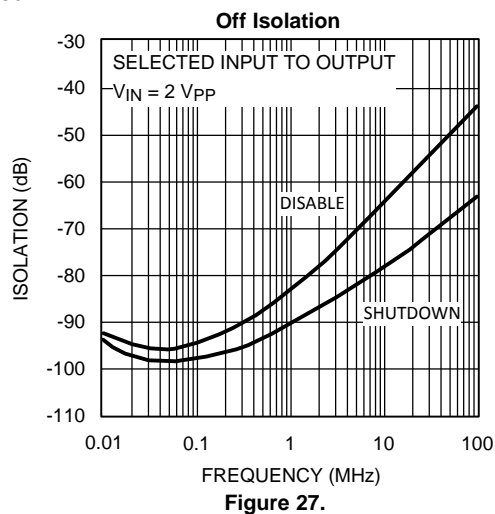
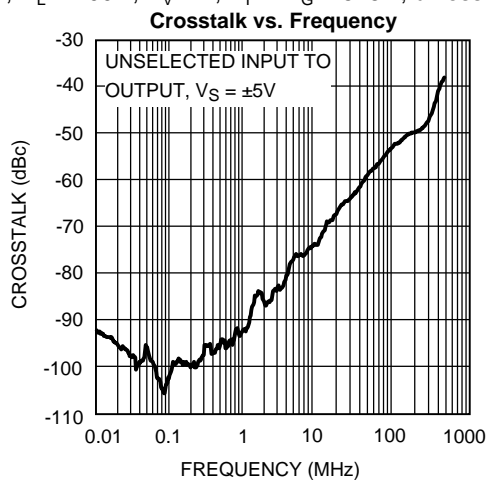


Figure 25.

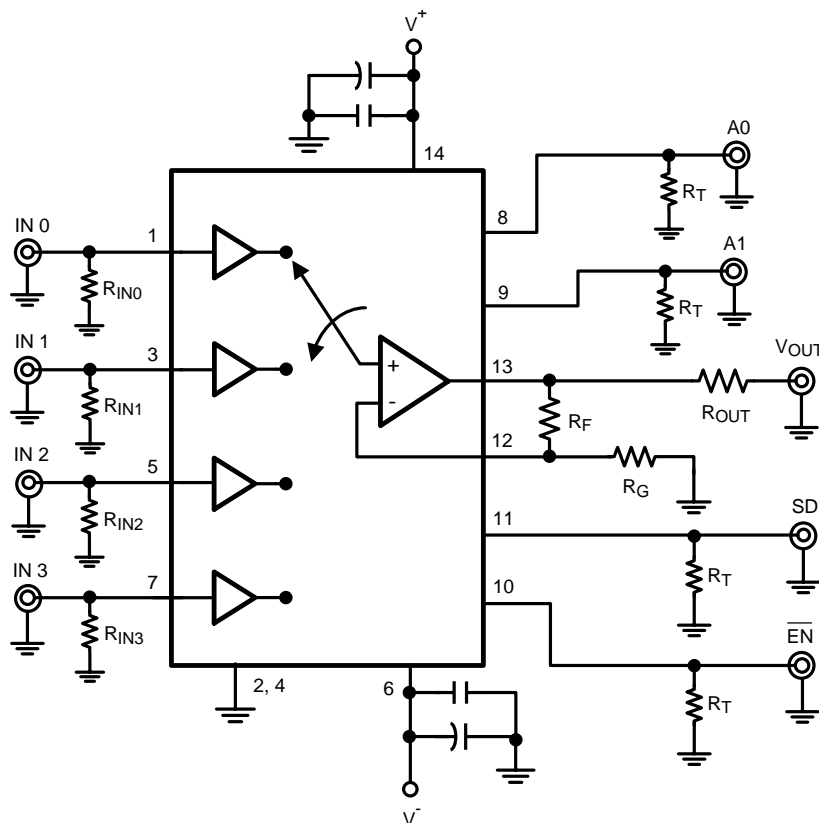
(1) Positive Value is current into device.

### Typical Performance Characteristics (continued)

$V_S = \pm 5V$ ,  $R_L = 100\Omega$ ,  $A_V = 2$ ,  $R_F = R_G = 575\Omega$ ; unless otherwise specified.



## GENERAL INFORMATION

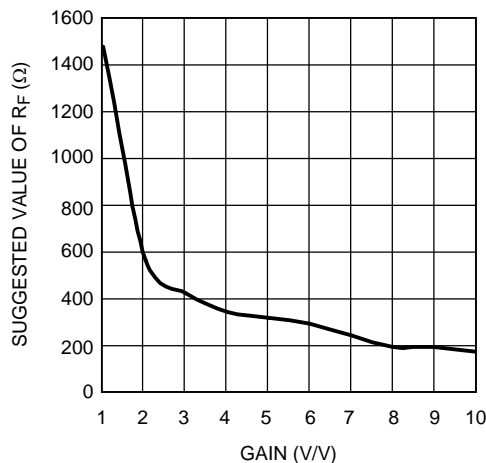


### Figure 28. Typical Application

## VIDEO PERFORMANCE

The LMH6574 has been designed to provide excellent performance with production quality video signals in a wide variety of formats such as HDTV and High Resolution VGA. Best performance will be obtained with back-terminated loads. The back termination reduces reflections from the transmission line and effectively masks transmission line and other parasitic capacitances from the amplifier output stage. [Figure 28](#) shows a typical configuration for driving a 75Ω. Cable. The output buffer is configured for a gain of 2, so using back terminated loads will give a net gain of 1.

## FEEDBACK RESISTOR SELECTION



**Figure 29. Suggested  $R_F$  vs. Gain**

The LMH6574 has a current feedback output buffer with gain determined by external feedback ( $R_F$ ) and gain set ( $R_G$ ) resistors. With current feedback amplifiers, the closed loop frequency response is a function of  $R_F$ . For a gain of 2 V/V, the recommended value of  $R_F$  is 575 $\Omega$ . For other gains see [Figure 29](#). Generally, lowering  $R_F$  from the recommended value will peak the frequency response and extend the bandwidth while increasing the value of  $R_F$  will cause the frequency response to roll off faster. Reducing the value of  $R_F$  too far below the recommended value will cause overshoot, ringing and, eventually, oscillation.

Since all applications are slightly different it is worth some experimentation to find the optimal  $R_F$  for a given circuit. For more information see Application Note OA-13 ([SNOA366](#)) which describes the relationship between  $R_F$  and closed-loop frequency response for current feedback operational amplifiers. The impedance looking into pin 12 is approximately 20 $\Omega$ . This allows for good bandwidth at gains up to 10 V/V. When used with gains over 10 V/V, the LMH6574 will exhibit a "gain bandwidth product" similar to a typical voltage feedback amplifier. For gains of over 10 V/V consider selecting a high performance video amplifier like the LMH6720 to provide additional gain.

### SD vs. $\overline{EN}$

The LMH6574 has both shutdown and disable capability. The shutdown feature affects the entire chip, whereas the disable function only affects the output buffer. When in shutdown mode, minimal power is consumed. The shutdown function is very fast, but causes a very brief spike of about 400 mV to appear on the output. When in shutdown mode the LMH6574 consumes only 1.8 mA of supply current. For maximum input to output isolation use the shutdown function.

The  $\overline{EN}$  pin only disables the output buffer which results in a substantially reduced output glitch of only 50 mV. While disabled the chip consumes 4.7 mA, considerably more than when shutdown. This is because the input buffers are still active. For minimal output glitch use the  $\overline{EN}$  pin. Also, care should be taken to ensure that, while in the disabled state, the voltage differential between the active input buffer (the one selected by pins A0 and A1) and the output pin stays less than 2V. As the voltage differential increases, input to output isolation decreases. Normally this is not an issue. See the section on [MULTIPLEXER EXPANSION](#) for further details.

To reduce the output glitch when using the SD pin, switch the  $\overline{EN}$  pin at least 10 ns before switching the SD pin. This can be accomplished by using an RC delay circuit between the two pins if only one control signal is available.

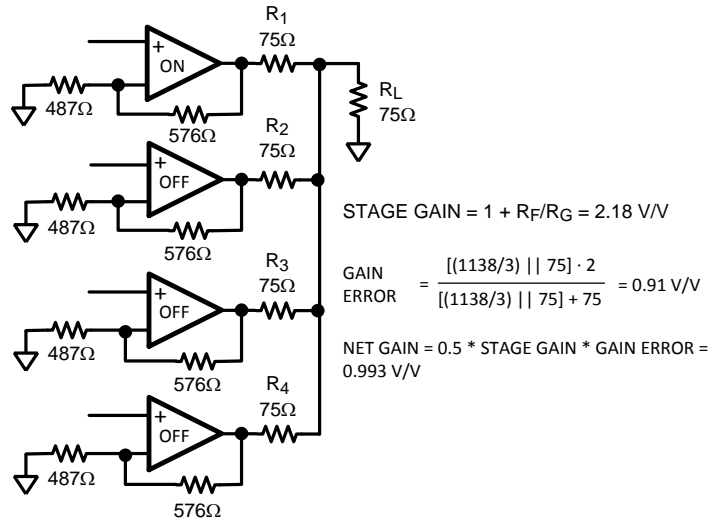
Logic inputs "SD" and " $\overline{EN}$ " will revert to the "High", while "A<sub>0</sub>" and "A<sub>1</sub>" will revert to the "Low" state when left floating.

Figure 30 shows an 8:1 MUX using two LMH6574s.

**Figure 30. 8:1 MUX USING TWO LMH6574s**

### Figure 31. Delay Circuit Implementation

With the SHUTDOWN pin putting the output stage into a high impedance state, several LMH6574's can be tied together to form a larger input MUX. However, there is a loading effect on the active output caused by the unselected devices. The circuit in Figure 32 shows how to compensate for this effect. For the 16:1 MUX function shown in Figure 32 below the gain error would be about -0.8 dB, or about 9%. In the circuit in Figure 32, resistor ratios have been adjusted to compensate for this gain error. By adjusting the gain of each multiplexer circuit the error can be reduced to the tolerance of the resistors used (1% in this example).



**Figure 32. Multiplexer Gain Compensation**

Disabling of the LMH6574 using the  $\overline{\text{EN}}$  pin is not recommended for use when doing multiplexer expansion. While disabled, if the voltage between the selected input and the chip output exceeds approximately 2V the device will begin to enter a soft breakdown state. This will show up as reduced input to output isolation. The signal on the non-inverting input of the output driver amplifier will leak through to the inverting input, and then to the output through the feedback resistor. The worst case is a gain of 1 configuration where the non inverting input follows the active input buffer and (through the feedback resistor) the inverting input follows the voltage driving the output stage. The solution for this is to use shutdown mode for multiplexer expansion.

## Other Applications

The LMH6574 could support a multi antenna receiver with up to four separate antennas. Monitoring the signal strength of all 4 antennas and connecting the strongest signal to the final IF stage would provide effective spacial diversity.

For direction finding, the LMH6574 could be used to provide high speed sampling of four separate antennas to a single DSP which would use the information to calculate the direction of the received signal.

## DRIVING CAPACITIVE LOADS

Capacitive output loading applications will benefit from the use of a series output resistor  $R_{OUT}$ . Figure 33 shows the use of a series output resistor,  $R_{OUT}$ , to stabilize the amplifier output under capacitive loading. Capacitive loads of 5 to 120 pF are the most critical, causing ringing, frequency response peaking and possible oscillation. The chart Figure 34 gives a recommended value for selecting a series output resistor for mitigating capacitive loads. The values suggested in the charts are selected for 0.5 dB or less of peaking in the frequency response. This gives a good compromise between settling time and bandwidth. For applications where maximum frequency response is needed and some peaking is tolerable, the value of  $R_{OUT}$  can be reduced slightly from the recommended values.

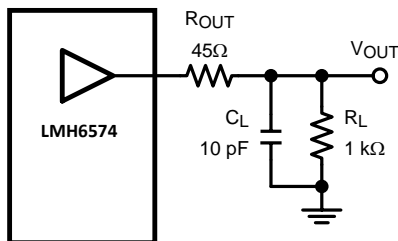


Figure 33. Decoupling Capacitive Loads

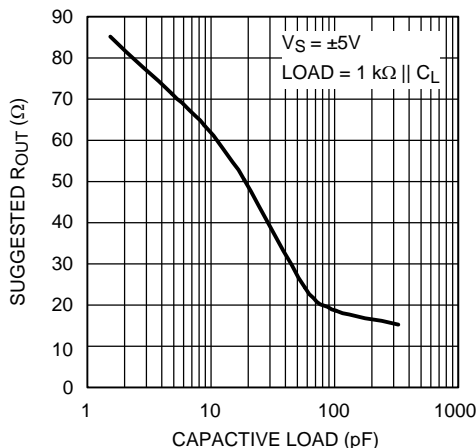


Figure 34. Suggested  $R_{OUT}$  vs. Capacitive Load

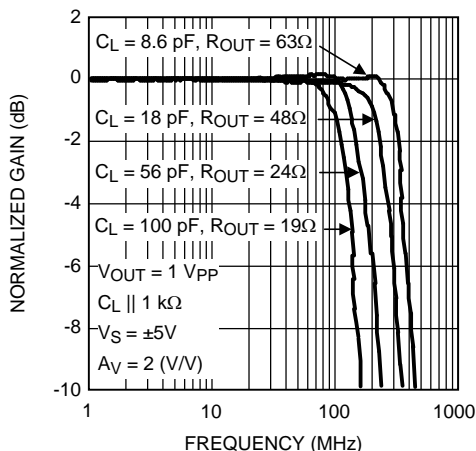


Figure 35. Frequency Response vs. Capacitive Load

## LAYOUT CONSIDERATIONS

Whenever questions about layout arise, use the evaluation board as a guide. The LMH730276 is the evaluation board supplied with samples of the LMH6574. To reduce parasitic capacitances, ground and power planes should be removed near the input and output pins. For long signal paths controlled impedance lines should be used, along with impedance matching elements at both ends. Bypass capacitors should be placed as close to the device as possible. Bypass capacitors from each rail to ground are applied in pairs. The larger electrolytic bypass capacitors can be located farther from the device, the smaller ceramic capacitors should be placed as close to the device as possible. In Figure 28, the capacitor between  $V^+$  and  $V^-$  is optional, but is recommended for best second harmonic distortion. Another way to enhance performance is to use pairs of 0.01  $\mu\text{F}$  and 0.1  $\mu\text{F}$  ceramic capacitors for each supply bypass.

## POWER DISSIPATION

The LMH6574 is optimized for maximum speed and performance in the small form factor of the standard SOIC package. To ensure maximum output drive and highest performance, thermal shutdown is not provided. Therefore, it is of utmost importance to make sure that the  $T_{JMAX}$  is never exceeded due to the overall power dissipation.

Follow these steps to determine the Maximum power dissipation for the LMH6574:

1. Calculate the quiescent (no-load) power.

$$P_{AMP} = I_{CC} * (V_S)$$

where

- $V_S = V^+ - V^-$  (1)

2. Calculate the RMS power dissipated in the output stage:

$$P_D (rms) = rms ((V_S - V_{OUT}) * I_{OUT})$$

where

- $V_{OUT}$  is the voltage across the external load
- $I_{OUT}$  is the current through the external load
- $V_S$  is the total supply voltage (2)

3. Calculate the total RMS power:  $P_T = P_{AMP} + P_D$ .

The maximum power that the LMH6574 package can dissipate at a given temperature can be derived with the following equation:

$$P_{MAX} = (150^\circ - T_{AMB}) / \theta_{JA}$$

where

- $T_{AMB}$  = Ambient temperature ( $^\circ\text{C}$ )
- $\theta_{JA}$  = Thermal resistance, from junction to ambient, for a given package ( $^\circ\text{C}/\text{W}$ ) (3)

For the SOIC package  $\theta_{JA}$  is  $130^\circ\text{C}/\text{W}$ .

## ESD PROTECTION

The LMH6574 is protected against electrostatic discharge (ESD) on all pins. The LMH6574 will survive 2000V Human Body model and 200V Machine model events. Under normal operation the ESD diodes have no effect on circuit performance. There are occasions, however, when the ESD diodes will be evident. If the LMH6574 is driven by a large signal while the device is powered down the ESD diodes will conduct. The current that flows through the ESD diodes will either exit the chip through the supply pins or will flow through the device, hence it is possible to power up a chip with a large signal applied to the input pins. Using the shutdown mode is one way to conserve power and still prevent unexpected operation.

## EVALUATION BOARDS

Texas Instruments provides the following evaluation boards as a guide for high frequency layout and as an aid in device testing and characterization. Many of the data sheet plots were measured with this board.

| Device  | Package | Evaluation Board |
|---------|---------|------------------|
| LMH6574 | SOIC    | LMH730276        |

An evaluation board can be shipped when a sample request is placed with Texas Instruments. Samples can be ordered on the TI web page.



## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| LMH6574MA        | NRND          | SOIC         | D                  | 14   | 55             | TBD                        | Call TI                 | Call TI              | -40 to 85    | LMH65<br>74MA           |                         |
| LMH6574MA/NOPB   | ACTIVE        | SOIC         | D                  | 14   | 55             | Green (RoHS<br>& no Sb/Br) | SN   CU SN              | Level-1-260C-UNLIM   | -40 to 85    | LMH65<br>74MA           | <a href="#">Samples</a> |
| LMH6574MAX/NOPB  | ACTIVE        | SOIC         | D                  | 14   | 2500           | Green (RoHS<br>& no Sb/Br) | SN   CU SN              | Level-1-260C-UNLIM   | -40 to 85    | LMH65<br>74MA           | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

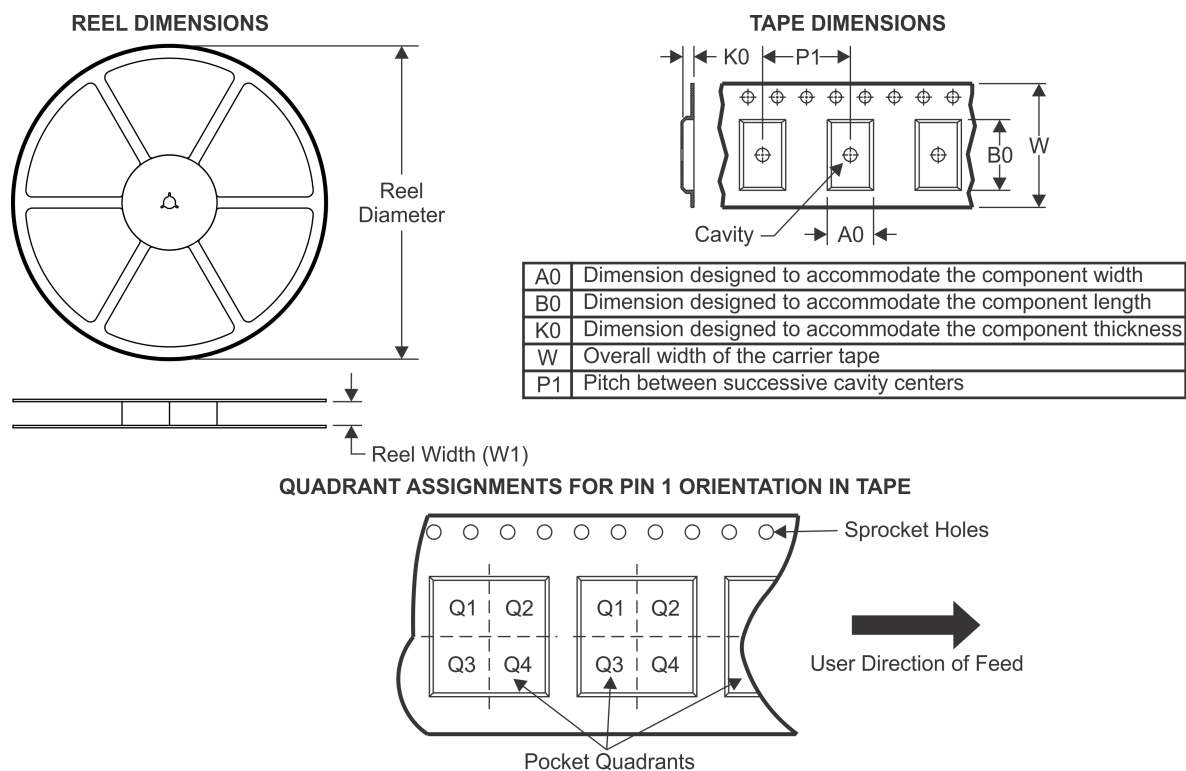
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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LMH6574MAX/NOPB | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.35    | 2.3     | 8.0     | 16.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS

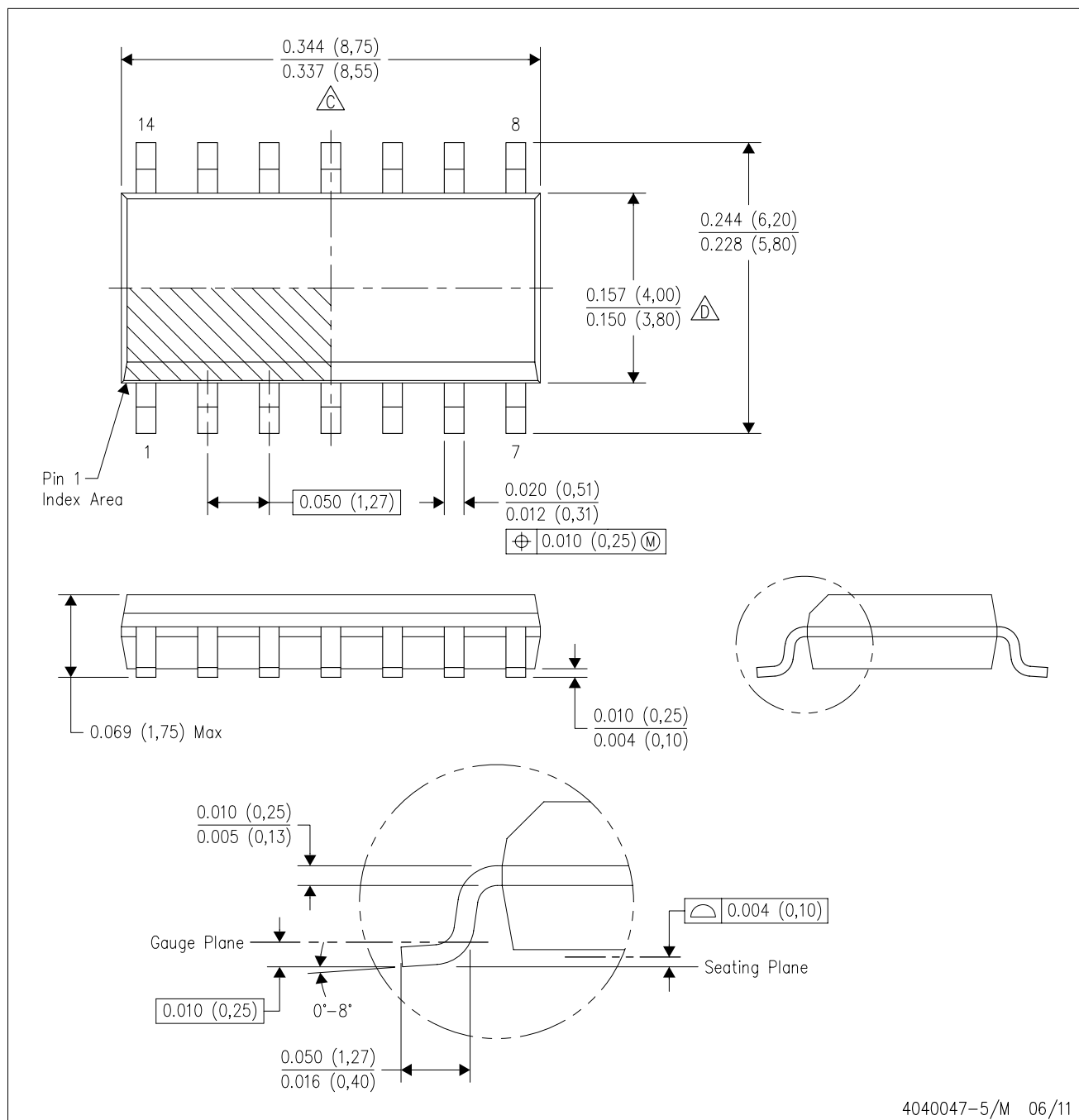


\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LMH6574MAX/NOPB | SOIC         | D               | 14   | 2500 | 367.0       | 367.0      | 35.0        |

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

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