LMC568 Low Power Phase-Locked Loop

Check for Samples: LMC568

FEATURES

- **Demodulates ±15% Deviation FM/FSK Signals**
- **Carrier Detect Output with Hysteresis**
- **Operation to 500 kHz Input Frequency**
- **Low THD—0.5% Typ. for ±10% Deviation**
- **2V to 9V Supply Voltage Range**
- **Low Supply Current Drain**

DESCRIPTION

The LMC568 is an amplitude-linear phase-locked loop consisting of a linear VCO, fully balanced phase detectors, and a carrier detect output. LMCMOS technology is employed for high performance with low power consumption.

The VCO has a linearized control range of ±30% to allow demodulation of FM and FSK signals. Carrier detect is indicated when the PLL is locked to an input signal greater than 26 mVrms. LMC568 applications include FM SCA and TV second audio program decoders, FSK data demodulators, and voice pagers.

Typical Application

(100 kHz input frequency, refer to Notes to Typical Application)

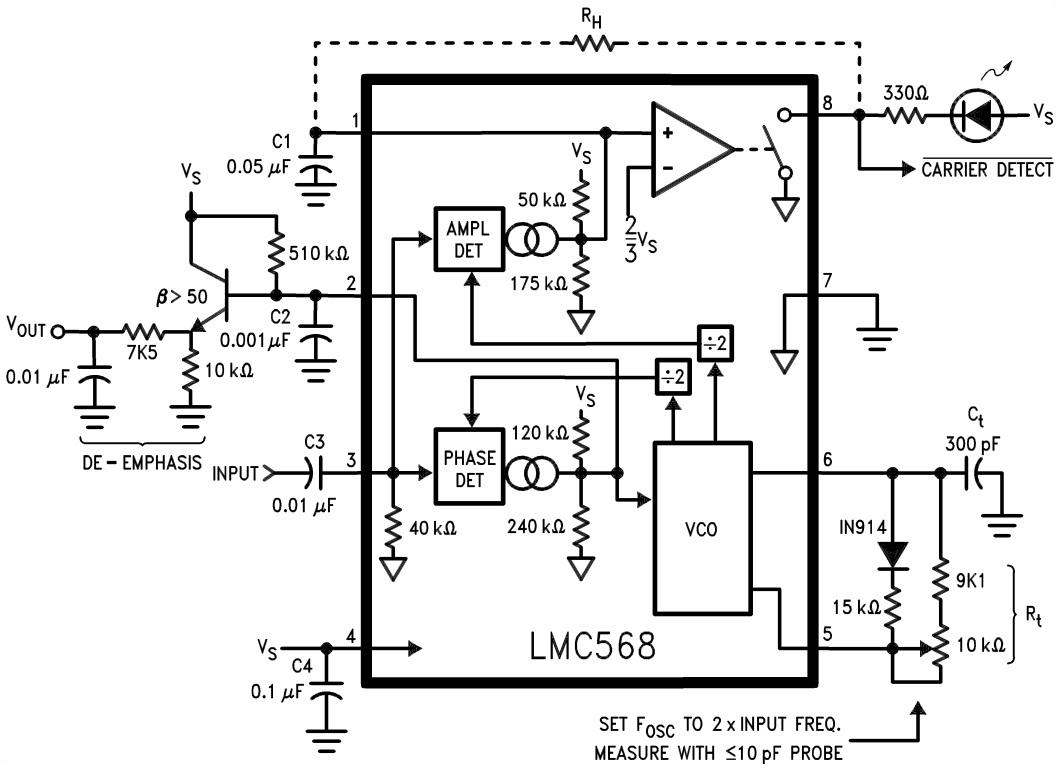


Figure 1. 8-Pin SOIC or PDIP
See D or P Package

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

Input Voltage, Pin 3			2 V_{p-p}
Supply Voltage, Pin 4			10V
Output Voltage, Pin 8			13V
Voltage at All Other Pins			V_s to Gnd
Output Current, Pin 8			30 mA
Package Dissipation			500 mW
Operating Temperature Range (T_A)			−25°C to +125°C
Storage Temperature Range			−55°C to +150°C
Soldering Information	PDIP Package	Soldering (10 seconds)	260°C
	SOIC Package	Vapor Phase (60 seconds)	215°C
		Infrared (15 seconds)	220°C

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

Electrical Characteristics

Test Circuit, T_A= 25°C, V_S= 5V, RtCt #2, Sw. 1 Pos. 0; and no input unless otherwise noted.

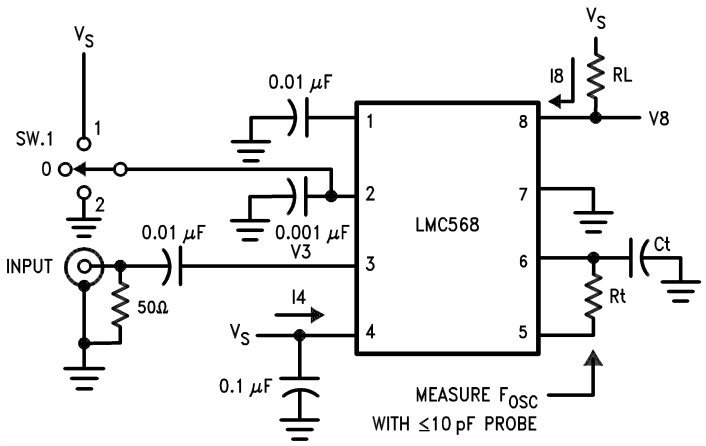
Symbol	Parameter	Conditions		Min	Typ	Max	Units
I4	Power Supply Current	RtCt # 1, Quiescent or Activated	V_S = 2V		0.35		mAdc
			V_S = 5V		0.75	1.5	
			V_S = 9V		1.2	2.4	
V3	Input D.C. Bias				0		mVdc
R3	Input Resistance				40		kΩ
I8	Output Leakage				1	100	nAdc
f_0	Center Frequency $F_{osc} \div 2$	RtCt #2, Measure Oscillator Frequency and Divide by 2	V_S = 2V		98		kHz
			V_S = 5V	90	103	115	
			V_S = 9V		105		
Δf_0	Center Frequency Shift with Supply	$\frac{f_0\|_{9V} - f_0\|_{2V}}{7\, f_0\|_{5V}} \times 100$			1.0	2.0	%/V
V_{in}	Input Threshold	Set Input Frequency Equal to f_0 Measured Above, Increase Input Level until Pin 8 Goes Low.	V_S = 2V	8	16	25	mVrms
			V_S = 5V	15	26	42	
			V_S = 9V		45		
ΔV_{in}	Input Hysteresis	Starting at Input Threshold, Decrease Input Level until Pin 8 Goes High			1.5		mVrms
V8	Output "Sat" Voltage	Input Level > Threshold Choose RL for Specified I8	I8 = 2 mA		0.06	0.15	Vdc
			I8 = 20 mA		0.7		
L.D.B.W.	Largest Detection Bandwidth	Measure F_{osc} with Sw. 1 in Pos. 0, 1, and 2; $L.D.B.W. = \frac{F_{osc}\|_{P2} - F_{osc}\|_{P1}}{F_{osc}\|_{P0}} \times 100$	V_S = 2V		30		%
			V_S = 5V	40	55		
			V_S = 9V		60		
ΔBW	Bandwidth Skew	$Skew = \left(\frac{F_{osc}\|_{P2} - F_{osc}\|_{P1}}{2\, F_{osc}\|_{P0}} - 1\right) \times 100$			1	±5	%
V_{out}	Recovered Audio	Typical Application Circuit Input = 100 mVrms, F = 100 kHz F_{mod} = 400 Hz, ± 10 kHz Dev.	V_S = 2V		170		mVrms
			V_S = 5V		270		
			V_S = 9V		400		

Electrical Characteristics (continued)

Test Circuit, T_A= 25°C, V_S= 5V, RtCt #2, Sw. 1 Pos. 0; and no input unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
THD	Total Harmonic Distortion	Typical Application Circuit as Above, Measure V_{out} Distortion.		0.5		%
$\frac{S+N}{N}$	Signal to Noise Ratio	Typical Application Circuit Remove Modulation, Measure V_n (S + N)/N = 20 log (V_{out}/V_n).		65		dB
f_{max}	Highest Center Freq.	RtCt #3, Measure Oscillator Frequency and Divide by 2		700		kHz

Test Circuit



RtCt	Rt	Ct
#1	100k	300 pF
#2	10k	300 pF
#3	5.1k	62 pF

Notes to Typical Application

SUPPLY DECOUPLING

The decoupling of supply pin 4 becomes more critical at high supply voltages with high operating frequencies, requiring C4 to be placed as close to possible to pin 4. Also, due to pin voltages tracking supply, a large C4 is necessary for low frequency PSRR.

OSCILLATOR TIMING COMPONENTS

The voltage-controlled oscillator (VCO) on the LMC568 must be set up to run at twice the frequency of the input signal. The components shown in the typical application are for F_{osc} = 200 kHz (100 kHz input frequency). For operation at lower frequencies, increase the capacitor value; for higher frequencies proportionally reduce the resistor values.

If low distortion is not a requirement, the series diode/resistor between pins 6 and 5 may be omitted. This will reduce VCO supply dependence and increase V_{out} by approximately 2 dB with THD = 2% typical. The center frequency as a function of Rt and Ct is given by:

$$F_{OSC} \cong \frac{1}{1.4\ RtCt}\ Hz \quad (1)$$

To allow for I.C. and component value tolerences, the oscillator timing components will require a trim. This is generally accomplished by using a variable resistor as part of Rt, although Ct could also be padded. The amount of initial frequency variation due to the LMC568 itself is given in the electrical specifications; the total trim range must also accommodate the tolerances of Rt and Ct.

INPUT PIN

The input pin 3 is internally ground-referenced with a nominal 40 kΩ resistor. Signals that are centered on 0V may be directly coupled to pin 3; however, any d.c. potential must be isolated via C3.

OUTPUT TAKEOFF

The output signal is taken off the loop filter at pin 2. Pin 2 is the combined output of the phase detector and control input of the VCO for the phase-locked loop (PLL). The nominal pin 2 source resistance is 80 kΩ, requiring the use of an external buffer transistor to drive nominal loads.

For small values of C2, the PLL will have a fast acquisition time and the pull-in range will be set by the built-in VCO frequency stops, which also determine the largest detection bandwidth (LDBW). Increasing C2 results in improved noise immunity at the expense of acquisition time, and the pull-in range will become narrower than the LDBW. However, the maximum hold-in range will always equal the LDBW. The 2 kHz de-emphasis pole shown may be modified or omitted as required by the application.

CARRIER DETECT

Pin 1 is the output of a negative-going amplitude detector which has a nominal 0 signal output of 7/9 V_s. The output at pin 8 is an N-channel FET switch to ground which is activated when the PLL is locked and the input is of sufficient amplitude to cause pin 1 to fall below 2/3 V_s. The carrier detect threshold is internally set to 26 mVrms typical on a 5V supply.

Capacitor C1 in conjunction with the nominal 40 kΩ pin 1 internal resistance forms the output filter. The size of C1 is a tradeoff between slew rate and carrier ripple at the output comparator. Optional resistor R_H increases the hysteresis in the pin 8 output for applications such as audio mute control. The minimum allowable value for R_H is 330 kΩ.

LMC568 Typical Performance Characteristics

Frequency Drift with Temperature

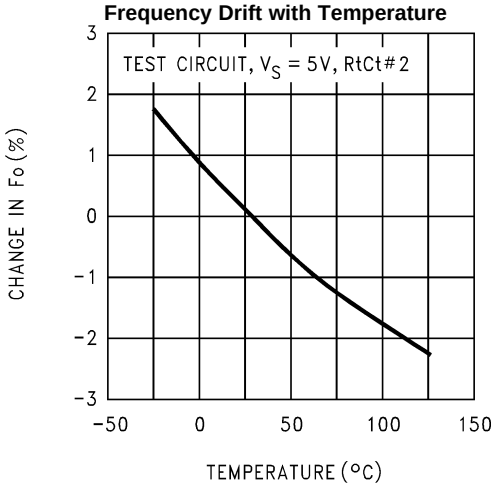


Figure 2.

Peak Deviation vs Input Signal Level

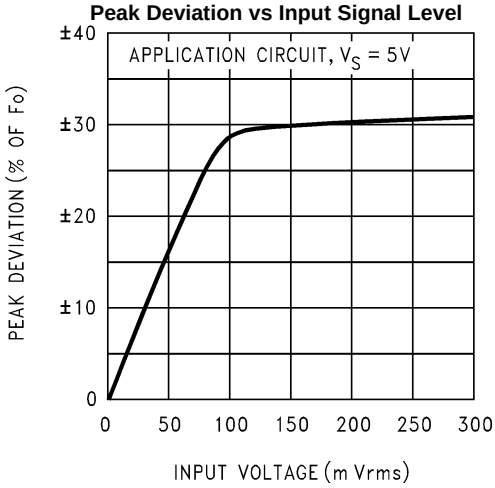


Figure 3.

Pull-In Range as a Function of C2

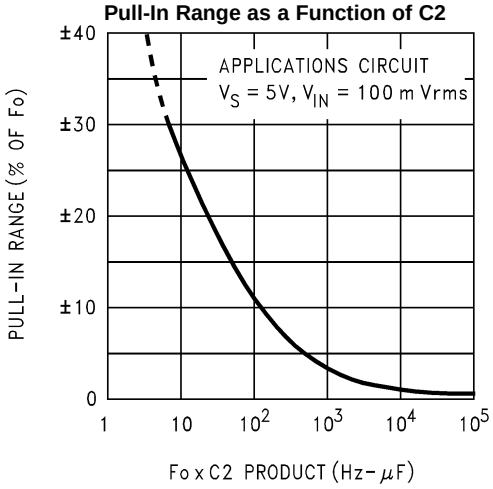


Figure 4.

REVISION HISTORY

Changes from Revision A (April 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	5

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LMC568CM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-25 to 100	LMC 568CM	Samples
LMC568CMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-25 to 100	LMC 568CM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

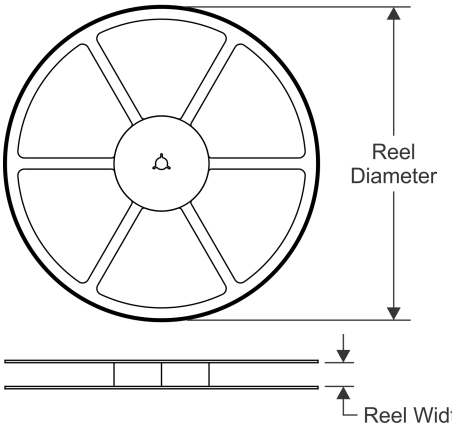
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

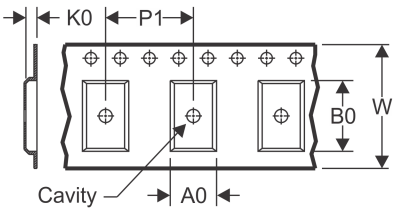
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

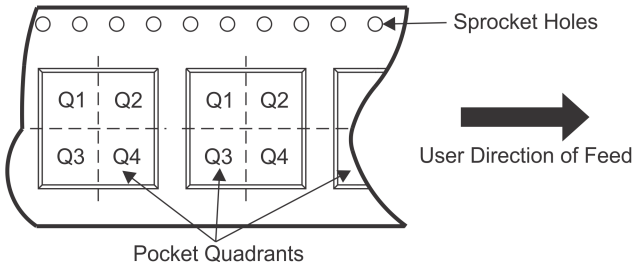


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

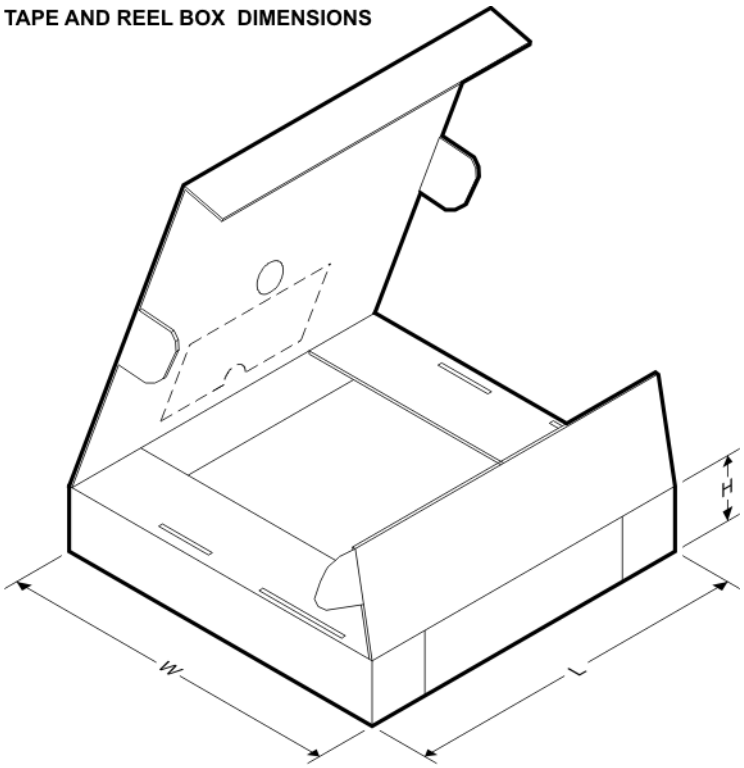
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMC568CMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

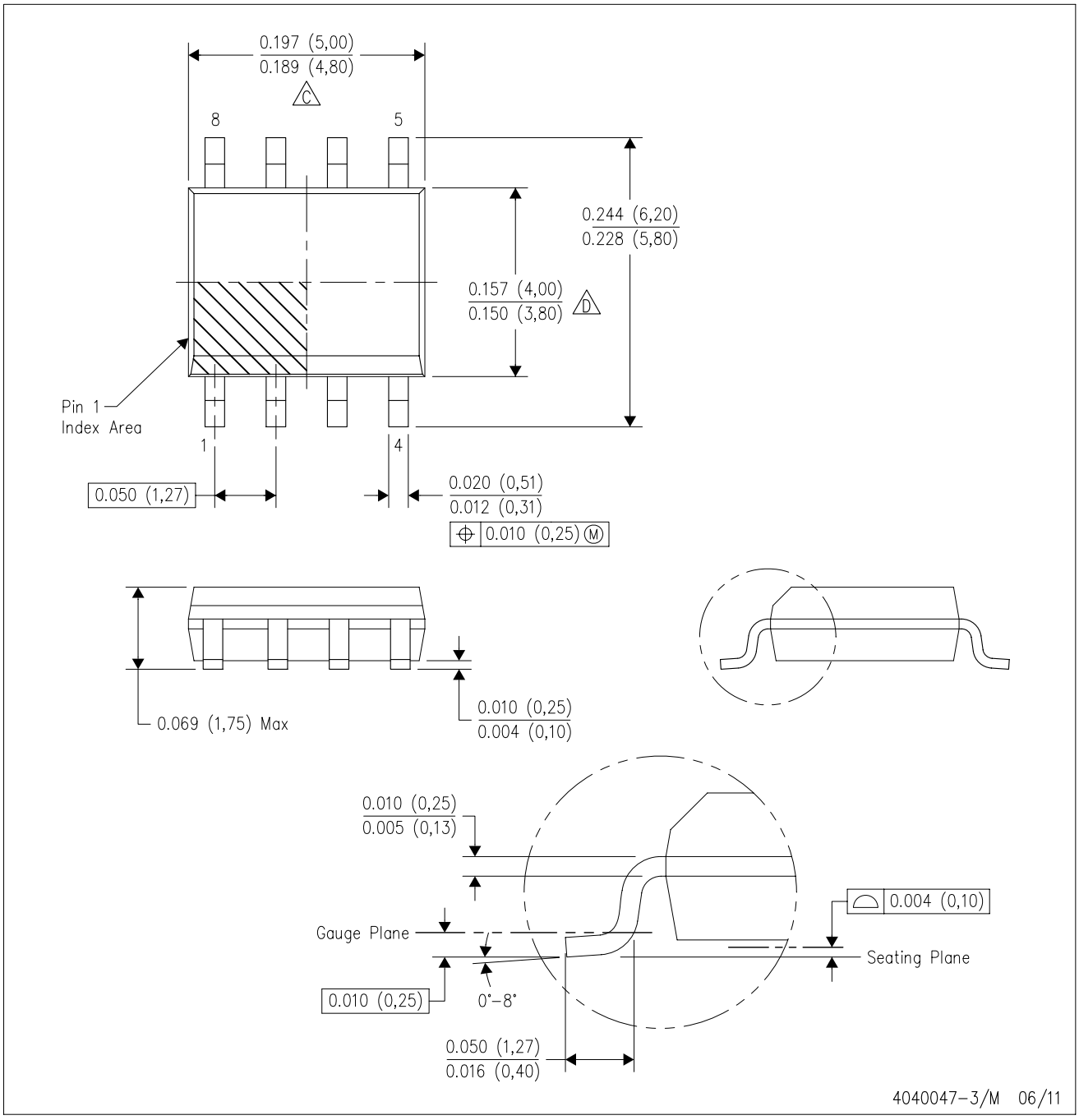
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMC568CMX/NOPB	SOIC	D	8	2500	349.0	337.0	45.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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