

# LM49321 Boomer® Audio Power Amplifier Series Audio Sub-System with Stereo DAC, Mono Class AB Loudspeaker Amplifier, OCL/SE Stereo Headphone Output and RF Suppression

Check for Samples: [LM49321](#), [LM49321RLEVAL](#)

## FEATURES

- 8-Bit Stereo DAC with up to 192kHz Sampling Rate
- Multiple Distinct Output Modes
- Mono Class AB Speaker Amplifier
- Stereo OCL/SE Headphone Amplifier
- Mono Earpiece Amplifier
- Differential Mono Analog Input
- Single-Ended Analog Inputs
- Independent Loudspeaker, Headphone and Mono Earpiece Volume controls
- I<sup>2</sup>C/SPI (Selectable) Compatible Interface
- Ultra Low Shutdown Current
- Click and Pop Suppression Circuit

## APPLICATIONS

- Cell Phones
- PDAs
- Laptop Computers
- Portable Devices

## KEY SPECIFICATIONS

- P<sub>OUT</sub> LS, 8Ω, 3.3V, 1% THD+N: 520 mW (Typ)
- P<sub>OUT</sub> HP, 32Ω, 3.3V, 1% THD+N: 36 mW (Typ)
- P<sub>OUT</sub> Mono Earpiece, 32Ω, 1% THD+N: 55 mW (Typ)
- Shutdown Current: 0.6 μA (Typ)
- SNR (DAC + Amplifier): 85 dB (Typ)

## DESCRIPTION

The LM49321 is an integrated audio sub-system designed for mono voice, stereo music cell phones connecting to base band processors with mono differential analog voice paths. Operating on a 3.3V supply, it combines a mono speaker amplifier delivering 520mW into an 8Ω load, a stereo headphone amplifier delivering 36mW per channel into a 32Ω load, and a mono earpiece amplifier delivering 55mW into a 32Ω load. The headphone amplifier can be configured for output capacitor-less (OCL) or single-ended (SE) mode. It integrates the audio amplifiers, volume control, mixer, and power management control all into a single package. In addition, the LM49321 routes and mixes the single-ended stereo and differential mono inputs into multiple distinct output modes. The LM49321 features an I<sup>2</sup>S serial interface for full range audio and an I<sup>2</sup>C or SPI compatible interface for control. The full range music path features an SNR of 85dB with up to 192kHz playback.

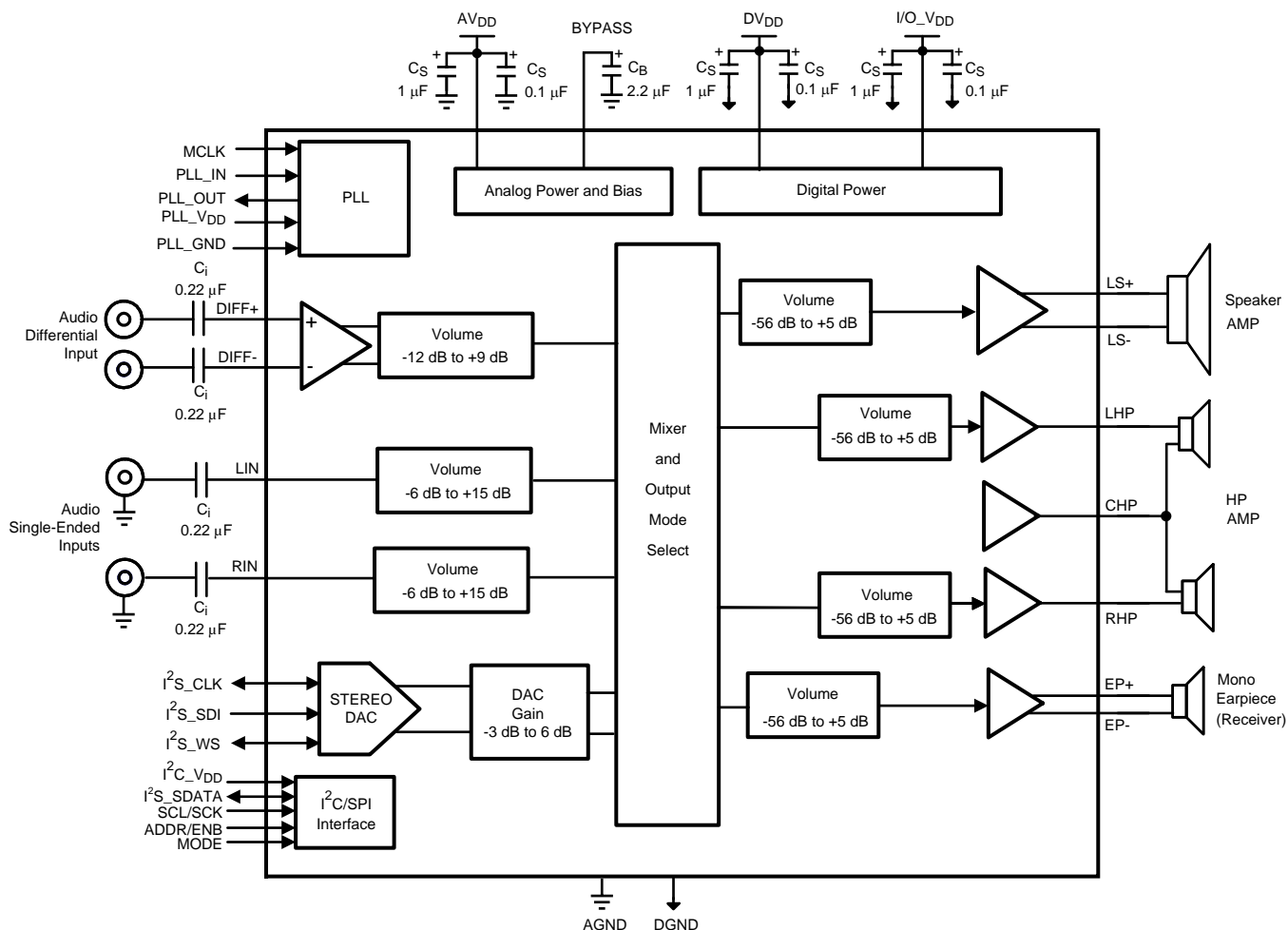
Boomer audio power amplifiers are designed specifically to provide high quality output power with a minimal amount of external components.



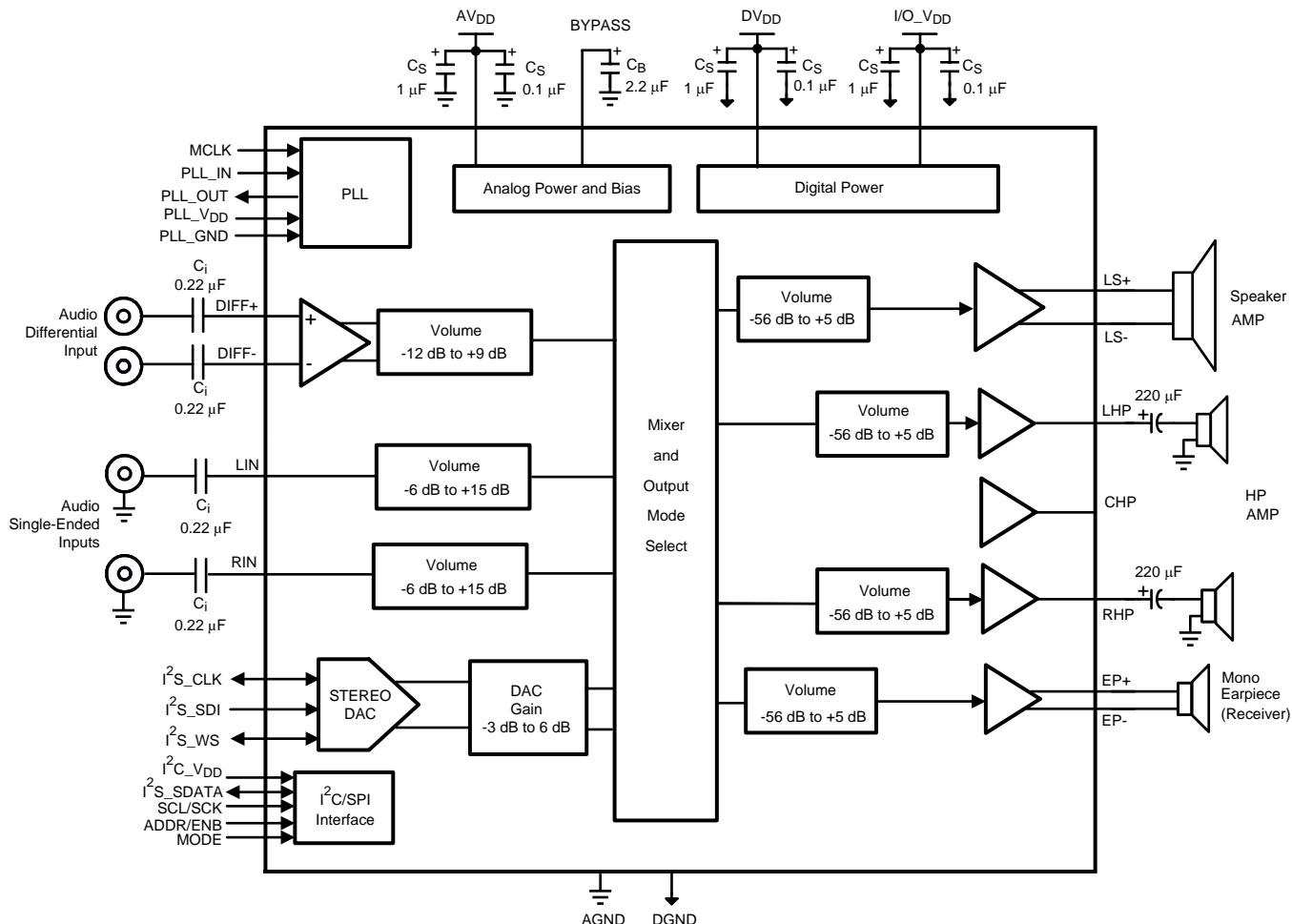
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## Block Diagram

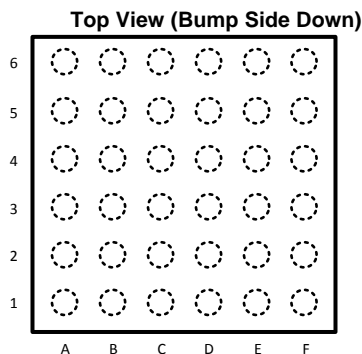


**Figure 1. Typical Audio Amplifier Subsystem Application Circuit with Output Capacitor-Less (OCL) Headphone Configuration**



**Figure 2. Typical Audio Amplifier Subsystem Application Circuit with Cap-Coupled Single-Ended (SE) Headphone Configuration**

### Connection Diagram



**Figure 3. 36 - Bump DSBGA Package**  
See Package Number YPG0036LVA

**PIN DESCRIPTIONS**

| Pin | Pin Name                         | Digital /Analog | I/O, Power | Description   |
|-----|----------------------------------|-----------------|------------|---|
| A1  | DGND                             | D               | P          | DIGITAL GND   |
| A2  | MCLK                             | D               | I          | MASTER CLOCK  |
| A3  | I <sup>2</sup> S_WS              | D               | I/O        | I <sup>2</sup> S WORD SELECT                          |
| A4  | SDA/SDI                          | D               | I/O        | I <sup>2</sup> C SDA OR SPI SDI                       |
| A5  | DV <sub>DD</sub>                 | D               | P          | DIGITAL SUPPLY VOLTAGE                                |
| A6  | I/O_V <sub>DD</sub>              | D               | P          | I/O SUPPLY VOLTAGE                                    |
| B1  | PLL_VDD                          | D               | P          | PLL SUPPLY VOLTAGE                                    |
| B2  | I <sup>2</sup> S_SDATA           | D               | I          | I <sup>2</sup> S SERIAL DATA INPUT                    |
| B3  | I <sup>2</sup> S_CLK             | D               | I/O        | I <sup>2</sup> S CLOCK SIGNAL                         |
| B4  | GPIO                             | D               | O          | TEST PIN (MUST BE LEFT FLOATING)                      |
| B5  | I <sup>2</sup> C_V <sub>DD</sub> | D               | P          | I <sup>2</sup> C SUPPLY VOLTAGE                       |
| B6  | SDL/SCK                          | D               | I          | I <sup>2</sup> C_SCL OR SPI_SCK                       |
| C1  | PLL_GND                          | D               | P          | PHASE LOCK LOOP GROUND                                |
| C2  | PLL_OUT                          | D               | O          | PHASE LOCK LOOP FILTER OUTPUT                         |
| C3  | PLL_IN                           | D               | I          | PLL FILTER INPUT                                      |
| C4  | ADDR/ENB                         | D               | I          | I <sup>2</sup> C ADDRESS OR SPI ENB DEPENDING ON MODE |
| C5  | BYPASS                           | A               | I          | HALF-SUPPLY BYPASS                                    |
| C6  | AV <sub>DD</sub>                 | A               | P          | ANALOG SUPPLY VOLTAGE                                 |
| D1  | AGND                             | A               | P          | ANALOG GROUND   |
| D2  | AGND                             | A               | P          | ANALOG GROUND   |
| D3  | NC                               |                 |            | NO CONNECT (MUST BE LEFT FLOATING)                    |
| D4  | MODE                             | D               | I          | SELECTS BETWEEN I <sup>2</sup> C OR SPI CONTROL       |
| D5  | RHP                              | A               | O          | RIGHT HEADPHONE OUTPUT                                |
| D6  | CHP                              | A               | O          | HEADPHONE CENTER PIN OUTPUT (1/2 VDD or GND)          |
| E1  | DIFF-                            | A               | I          | ANALOG NEGATIVE DIFFERENTIAL INPUT                    |
| E2  | LIN                              | A               | I          | ANALOG LEFT CHANNEL INPUT                             |
| E3  | RIN                              | A               | I          | ANALOG RIGHT CHANNEL INPUT                            |
| E4  | NC                               |                 |            | NO CONNECT (MUST BE LEFT FLOATING)                    |
| E5  | LHP                              | A               | O          | LEFT HEADPHONE OUTPUT                                 |
| E6  | AGND                             | A               | P          | ANALOG GROUND   |
| F1  | DIFF+                            | A               | I          | ANALOG POSITIVE DIFFERENTIAL INPUT                    |
| F2  | EP-                              | A               | O          | MONO EARPIECE- OUTPUT                                 |
| F3  | EP+                              | A               | O          | MONO EARPIECE+ OUTPUT                                 |
| F4  | LS-                              | A               | O          | LOUDSPEAKER OUTPUT-                                   |
| F5  | AV <sub>DD</sub>                 | A               | P          | ANALOG SUPPLY VOLTAGE                                 |
| F6  | LS+                              | A               | O          | LOUDSPEAKER OUTPUT+                                   |



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

**Absolute Maximum Ratings<sup>(1)(2)(3)(4)</sup>**

|   |                         |                                |
|---|-------------------------|--------------------------------|
| Analog Supply Voltage <sup>(1)</sup>      |                         | 6.0V                           |
| Digital Supply Voltage <sup>(1)</sup>     |                         | 6.0V                           |
| Storage Temperature                       |                         | -65°C to +150°C                |
| Input Voltage                             |                         | -0.3V to V <sub>DD</sub> +0.3V |
| Power Dissipation <sup>(5)</sup>          |                         | Internally Limited             |
| ESD Ratings <sup>(6)</sup>                |                         | 2000V                          |
| ESD Ratings <sup>(7)</sup>                |                         | 200V                           |
| Junction Temperature (T <sub>JMAX</sub> ) |                         | 150°C                          |
| Thermal Resistance                        | θ <sub>JA</sub> (RLA36) | 100°C/W                        |

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.
- (2) The Electrical Characteristics tables list specified specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
- (3) Soldering Information: See AN-1279 "Microfill Wafer Level Underfilled Chip Scale package" (Literature Number [SNOA430](#))
- (4) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
- (5) Maximum allowable power dissipation is P<sub>DMAX</sub> = (T<sub>JMAX</sub> - T<sub>A</sub>) / θ<sub>JA</sub> or the number given in Absolute Maximum Ratings, whichever is lower.
- (6) Human body model, applicable std. JESD22-A114C.
- (7) Machine model, applicable std. JESD22-A115-A.

**Operating Ratings<sup>(1)(2)</sup>**

|   |  |  |
|---|--|--|
| Temperature Range (T <sub>MIN</sub> ≤ T <sub>A</sub> ≤ T <sub>MAX</sub> ) |  | -40°C ≤ T <sub>A</sub> ≤ +85°C                 |
| Supply Voltage  |  | 2.7V ≤ AV <sub>DD</sub> ≤ 5.5V                 |
|   |  | 2.7V ≤ DV <sub>DD</sub> ≤ 4.0V                 |
|   |  | 1.7V ≤ I <sup>2</sup> C_V <sub>DD</sub> ≤ 4.0V |
|   |  | 1.7V ≤ I/O_V <sub>DD</sub> ≤ 4.0V              |

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**Audio Amplifier Electrical Characteristics  $AV_{DD} = 3.0V$ ,  $DV_{DD} = 3.0V^{(1)(2)}$** 

The following specifications apply for the circuit shown in [Figure 41](#) with all programmable gain set at 0dB, unless otherwise specified. Limits apply for  $T_A = 25^\circ C$ .

| Parameter     |                                 | Test Conditions  | LM49321            |                       | Units<br>(Limits) |
|---------------|---------------------------------|--|--------------------|-----------------------|-------------------|
|               |                                 |  | Typ <sup>(3)</sup> | Limits <sup>(4)</sup> |                   |
| $I_{DD}$      | Supply Current                  | $V_{IN} = 0$ , No Load<br>All Amps On + DAC, OCL <sup>(5)</sup>                            | 13                 | 18                    | mA (max)          |
|               |                                 | Headphone Mode Only, OCL, DAC off  | 4.6                | 6.25                  | mA (max)          |
|               |                                 | Headphone Mode Only, OCL, DAC Off<br>STEREO_OUTPUT_ONLY = 1,<br>STEREO_INPUT_ONLY = 1      | 4                  | 5.5                   | mA                |
|               |                                 | Headphone Mode only OCL, DAC On,<br>OSR = 64, DAC_INPUT_ONLY = 1<br>STEREO_OUTPUT_ONLY = 1 | 7.5                | 10                    | mA (max)          |
|               |                                 | Mono Loudspeaker Mode Only   | 6.5                | 11.5                  | mA (max)          |
|               |                                 | Mono Earpiece Speaker Mode Only<br>MONO_ONLY = 1 (register 01h)<br>MONO_ONLY = 0           | 3.7<br>3.3         | 5                     | mA (max)<br>mA    |
|               |                                 | DAC Off, All Amps On (OCL) <sup>(5)</sup>  | 10                 | 13.5                  | mA (max)          |
|               |                                 |  |                    |                       |                   |
| $I_{SD}$      | Shutdown Current                | See <sup>(6)</sup>   | 0.6                | 1                     | $\mu A$ (max)     |
| $P_O$         | Output Power                    | Speaker; THD = 1%; $f = 1kHz$ , 8 $\Omega$ BTL   | 420                | 370                   | mW (min)          |
|               |                                 | Headphone; THD = 1%; $f = 1kHz$ , 32 $\Omega$ SE   | 27                 | 24                    | mW (min)          |
|               |                                 | Earpiece; THD = 1%; $f = 1kHz$ , 32 $\Omega$ BTL   | 45                 | 40                    | mW (min)          |
| $V_{FS\ DAC}$ | Full Scale DAC Output           |  | 2.4                |                       | $V_{RMS}$         |
| THD+N         | Total Harmonic Distortion+Noise | Speaker; $P_O = 200mW$ ; $f = 1kHz$ , 8 $\Omega$ BTL                                       | 0.04               |                       | %                 |
|               |                                 | Headphone; $P_O = 10mW$ ; $f = 1kHz$ , 32 $\Omega$ SE                                      | 0.01               |                       | %                 |
|               |                                 | Earpiece; $P_O = 20mW$ ; $f = 1kHz$ , 32 $\Omega$ BTL                                      | 0.04               |                       | %                 |
| $V_{OS}$      | Offset Voltage                  | Speaker  | 10                 | 55                    | mV (max)          |
|               |                                 | Earpiece   | 8                  | 50                    | mV (max)          |
|               |                                 | Headphone (OCL)  | 8                  | 15                    | mV (max)          |
| $\epsilon_O$  | Output Noise                    | A-weighted; 0dB gain   | Table 1            |                       |                   |
| PSRR          | Power Supply Rejection Ratio    | $f = 217Hz$ ; $V_{RIPPLE} = 200mV_{P-P}$ , $C_B = 2.2\mu F$                                | Table 2            |                       |                   |
| $X_{TALK}$    | Crosstalk                       | Headphone; $P_O = 10mW$ , $f = 1kHz$ ; OCL   | -60                |                       | dB                |
| $T_{WU}$      | Wake-Up Time                    | $C_B = 2.2\mu F$ , $CD\_6 = 0$   | 35                 |                       | ms                |
|               |                                 | $C_B = 2.2\mu F$ , $CD\_6 = 1$   | 85                 |                       | ms                |
| CMRR          | Common-Mode Rejection Ratio     | $f = 217Hz$ , $V_{RMS} = 200mV_{PP}$   | 56                 |                       | dB                |

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.
- (2) The Electrical Characteristics tables list specified specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
- (3) Typical values represent most likely parametric norms at  $T_A = +25^\circ C$ , and at the Recommended Operation Conditions at the time of product characterization and are not ensured.
- (4) Datasheet min/max specification limits are ensured by test or statistical analysis.
- (5) Enabling mono bit (MONO\_ONLY in Output Control Register 01h) will save 400 $\mu A$  (typ) from specified current.
- (6) Shutdown current is measured in a normal room environment.

**Audio Amplifier Electrical Characteristics  $AV_{DD} = 5.0V$ ,  $DV_{DD} = 3.3V^{(1)(2)}$** 

The following specifications apply for the circuit shown in [Figure 41](#) with all programmable gain set at 0dB, unless otherwise specified. Limits apply for  $T_A = 25^\circ C$ .

| Parameter     |                                   | Test Conditions   | LM49321                 |                       | Units<br>(Limits) |
|---------------|-----------------------------------|---|-------------------------|-----------------------|-------------------|
|               |                                   |   | Typ <sup>(3)</sup>      | Limits <sup>(4)</sup> |                   |
| $I_{DD}$      | Supply Current                    | $V_{IN} = 0$ , No Load<br>All Amps On + DAC, OCL <sup>(5)</sup>                             | 17.5                    |                       | mA (max)          |
|               |                                   | Headphone Mode Only, OCL, DAC Off   | 5.8                     |                       | mA (max)          |
|               |                                   | Headphone Mode Only, OCL, DAC Off<br>STEREO_OUTPUT_ONLY = 1,<br>STEREO_INPUT_ONLY = 1       | 5.5                     |                       | mA                |
|               |                                   | Headphone Mode Only, OCL, DAC On,<br>OSR = 64, DAC_INPUT_ONLY = 1<br>STEREO_OUTPUT_ONLY = 1 | 9.5                     |                       | mA                |
|               |                                   | Mono Loudspeaker Mode Only <sup>(5)</sup>   | 11.6                    |                       | mA                |
|               |                                   | Mono Earpiece Mode Only <sup>(5)</sup>  | 5                       |                       | mA                |
|               |                                   | DAC Off, All Amps On (OCL) <sup>(5)</sup>   | 12.9                    |                       | mA                |
| $I_{SD}$      | Shutdown Current                  | See <sup>(6)</sup>  | 1.6                     |                       | $\mu A$           |
| $P_O$         | Output Power                      | Speaker; THD = 1%; f = 1kHz, 8 $\Omega$ BTL   | 1.25                    |                       | mW                |
|               |                                   | Headphone; THD = 1%; f = 1kHz, 32 $\Omega$ SE   | 80                      |                       | mW                |
|               |                                   | Earpiece; THD = 1%; f = 1kHz, 32 $\Omega$ BTL   | 175                     |                       | mW                |
| $V_{FS\ DAC}$ | Full Scale DAC Output             |   | 2.4                     |                       | $V_{RMS}$         |
| THD+N         | Total Harmonic Distortion + Noise | Speaker; $P_O = 500mW$ ; f = 1kHz, 8 $\Omega$ BTL   | 0.03                    |                       | %                 |
|               |                                   | Headphone; $P_O = 30mW$ ; f = 1kHz, 32 $\Omega$ SE  | 0.01                    |                       | %                 |
|               |                                   | Earpiece; $P_O = 40mW$ ; f = 1kHz, 32 $\Omega$ BTL  | 0.04                    |                       | %                 |
| $V_{OS}$      | Offset Voltage                    | Speaker   | 10                      |                       | mV                |
|               |                                   | Earpiece  | 8                       |                       | mV                |
|               |                                   | HP (OCL)  | 8                       |                       | mV                |
| $\epsilon_O$  | Output Noise                      | A-weighted; 0dB gain;   | <a href="#">Table 1</a> |                       |                   |
| PSRR          | Power Supply Rejection Ratio      | f = 217Hz; $V_{ripple} = 200mV_{P-P}$ , $C_B = 2.2\mu F$                                    | <a href="#">Table 3</a> |                       |                   |
| $X_{TALK}$    | Crosstalk                         | Headphone; $P_O = 15mW$ , f = 1kHz; OCL   | -56                     |                       | dB                |
| $T_{WU}$      | Wake-Up Time                      | $C_B = 2.2\mu F$ , $CD\_6 = 0$  | 45                      |                       | ms                |
|               |                                   | $C_B = 2.2\mu F$ , $CD\_6 = 1$  | 130                     |                       | ms                |

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- (2) The Electrical Characteristics tables list specified specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
- (3) Typical values represent most likely parametric norms at  $T_A = +25^\circ C$ , and at the Recommended Operation Conditions at the time of product characterization and are not ensured.
- (4) Datasheet min/max specification limits are ensured by test or statistical analysis.
- (5) Enabling mono bit (MONO\_ONLY in Output Control Register 01h) will save 400 $\mu A$  (typ) from specified current.
- (6) Shutdown current is measured in a normal room environment.

## Volume Control Electrical Characteristics<sup>(1)(2)</sup>

The following specifications apply for  $3.0V \leq AV_{DD} \leq 5.0V$  and  $2.7V \leq DV_{DD} \leq 4.0V$ , unless otherwise specified. Limits apply for  $T_A = 25^\circ C$ .

| Parameter          |   | Test Conditions                                       | LM49321            |                       | Units<br>(Limits) |
|--------------------|---|---|--------------------|-----------------------|-------------------|
|                    |   |   | Typ <sup>(3)</sup> | Limits <sup>(4)</sup> |                   |
| PGR                | Stereo Analog Inputs Pre-Amp Gain Setting Range                             | Minimum gain setting                                  | –6                 | –7                    | dB (min)          |
|                    |   |   |                    | –5                    | dB (max)          |
|                    | Differential Mono Analog Input Pre-Amp Gain Setting Range                   | Maximum gain setting                                  | 15                 | 15.5                  | dB (max)          |
|                    |   |   |                    | 14.5                  | dB (min)          |
|                    |   | Minimum gain setting                                  | –12                | –13                   | dB (min)          |
|                    |   |   |                    | –11                   | dB (max)          |
| VCR                | Output Volume Control for Loudspeaker, Headphone Output, or Earpiece Output | Minimum gain setting                                  | –56                | –59                   | dB (min)          |
|                    |   |   |                    | –53                   | dB (max)          |
|                    |   | Maximum gain setting                                  | +5                 | 4.5                   | dB (min)          |
|                    |   |   |                    | 5.5                   | dB (max)          |
| $\Delta A_{CH-CH}$ | Stereo Channel to Channel Gain Mismatch                                     |   | 0.3                |                       | dB                |
| $A_{MUTE}$         | Mute Attenuation  | $V_{IN} = 1V_{RMS}$ , Gain = 0dB with load, Headphone | –90                |                       | dB                |
| $R_{INPUT}$        | DIFF+, DIFF–, $L_{IN}$ and $R_{IN}$ Input Impedance                         |   | 23                 | 18                    | k $\Omega$ (min)  |
|                    |   |   |                    | 28                    | k $\Omega$ (max)  |

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- (2) The Electrical Characteristics tables list specified specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
- (3) Typical values represent most likely parametric norms at  $T_A = +25^\circ C$ , and at the Recommended Operation Conditions at the time of product characterization and are not ensured.
- (4) Datasheet min/max specification limits are ensured by test or statistical analysis.

## Digital Section Electrical Characteristics<sup>(1)(2)</sup>

The following specifications apply for  $3.0V \leq AV_{DD} \leq 5.0V$  and  $2.7V \leq DV_{DD} \leq 4.0V$ , unless otherwise specified. Limits apply for  $T_A = 25^\circ C$ .

| Parameter   |   | Test Conditions  | LM49321                          |  | Units<br>(Limits) |
|---|---|--|----------------------------------|--|-------------------|
|   |   |  | Typ <sup>(3)</sup>               | Limits <sup>(4)</sup>                      |                   |
| DI <sub>SD</sub>  | Digital Shutdown Current                | Mode 0, DV <sub>DD</sub> = 3.0V  |                                  |  |                   |
|   |   | No MCLK  | 0.01                             |  | μA                |
| DI <sub>DD</sub>  | Digital Power Supply Current            | f <sub>MCLK</sub> = 12MHz, DV <sub>DD</sub> = 3.0V<br>ALL MODES EXCEPT 0                   | 5.3                              | 6.5  | mA (max)          |
| PLLI <sub>DD</sub>  | PLL Quiescent Current                   | f <sub>MCLK</sub> = 12MHz, DV <sub>DD</sub> = 3.0V   | 4.8                              | 6  | mA (max)          |
| <b>Audio DAC (Typical numbers are with 6.144MHz audio clock and 48kHz sampling frequency)</b> |   |  |                                  |  |                   |
| R <sub>DAC</sub>  | Audio DAC Ripple                        | 20Hz - 20kHz through headphone output  | +/-0.1                           |  | dB                |
| PB <sub>DAC</sub>   | Audio DAC Passband width                | -3dB point   | 22.6                             |  | kHz               |
| SBA <sub>DAC</sub>  | Audio DAC Stop band Attenuation         | Above 24kHz  | 76                               |  | dB                |
| DR <sub>DAC</sub>   | Audio DAC Dynamic Range                 | DC - 20kHz, -60dBFS; AES17 Standard  | Table 4                          |  | dB                |
| SNR   | Audio DAC-AMP Signal to Noise Ratio     | A-Weighted, Signal = V <sub>O</sub> at 0dBFS, f = 1kHz<br>Noise = digital zero, A-weighted | Table 4                          |  | dB                |
| SNR <sub>DAC</sub>  | Internal DAC SNR                        | A-weighted <sup>(5)</sup>  | 95                               |  | dB                |
| <b>PLL</b>  |   |  |                                  |  |                   |
| f <sub>IN</sub>   | Input Frequency on MCLK pin             |  | 12                               | 10<br>26                                   | MHz               |
| <b>SPI/I<sup>2</sup>C (1.7V ≤ I<sup>2</sup>C_V<sub>DD</sub> ≤ 2.2V)</b>                       |   |  |                                  |  |                   |
| f <sub>SPI</sub>  | Maximum SPI Frequency                   |  |                                  | 1000                                       | kHz (max)         |
| t <sub>SPISETD</sub>  | SPI Data Setup Time                     |  |                                  | 250  | ns (max)          |
| t <sub>SPISETENB</sub>  | SPI ENB Setup Time                      |  |                                  | 250  | ns (max)          |
| t <sub>SPIHOLDD</sub>   | SPI Data Hold Time                      |  |                                  | 250  | ns (max)          |
| t <sub>SPIHOLDENB</sub>   | SPI ENB Hold Time                       |  |                                  | 250  | ns (max)          |
| t <sub>SPICL</sub>  | SPI Clock Low Time                      |  |                                  | 500  | ns (max)          |
| t <sub>SPICH</sub>  | SPI Clock High Time                     |  |                                  | 500  | ns (max)          |
| f <sub>CLKI2C</sub>   | I <sup>2</sup> C_CLK Frequency          |  |                                  | 400  | kHz (max)         |
| t <sub>I2CHOLD</sub>  | I <sup>2</sup> C_DATA Hold Time         |  |                                  | 250  | ns (max)          |
| t <sub>I2CSET</sub>   | I <sup>2</sup> C_DATA Setup Time        |  |                                  | 250  | ns (max)          |
| V <sub>IH</sub>   | I <sup>2</sup> C/SPI Input High Voltage |  | I <sup>2</sup> C_V <sub>DD</sub> | 0.7 x<br>I <sup>2</sup> C_V <sub>DD</sub>  | V (min)           |
| V <sub>IL</sub>   | I <sup>2</sup> C/SPI Input Low Voltage  |  | 0                                | 0.25 x<br>I <sup>2</sup> C_V <sub>DD</sub> | V (max)           |
| <b>SPI/I<sup>2</sup>C (2.2V ≤ I<sup>2</sup>C_V<sub>DD</sub> ≤ 4.0V)</b>                       |   |  |                                  |  |                   |
| f <sub>SPI</sub>  | Maximum SPI Frequency                   |  |                                  | 4000                                       | kHz (max)         |
| t <sub>SPISETD</sub>  | SPI Data Setup Time                     |  |                                  | 100  | ns (max)          |
| t <sub>SPISETENB</sub>  | SPI ENB Setup Time                      |  |                                  | 100  | ns (max)          |
| t <sub>SPIHOLDD</sub>   | SPI Data Hold Time                      |  |                                  | 100  | ns (max)          |
| t <sub>SPIHOLDENB</sub>   | SPI ENB Hold Time                       |  |                                  | 100  | ns (max)          |

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.
- (2) The Electrical Characteristics tables list specified specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.
- (3) Typical values represent most likely parametric norms at  $T_A = +25^\circ C$ , and at the Recommended Operation Conditions at the time of product characterization and are not ensured.
- (4) Datasheet min/max specification limits are ensured by test or statistical analysis.
- (5) Internal DAC only with DAC modes 00 and 01.

**Digital Section Electrical Characteristics<sup>(1)(2)</sup> (continued)**

The following specifications apply for  $3.0V \leq AV_{DD} \leq 5.0V$  and  $2.7V \leq DV_{DD} \leq 4.0V$ , unless otherwise specified. Limits apply for  $T_A = 25^\circ C$ .

| Parameter   |   | Test Conditions  | LM49321                          |                           | Units<br>(Limits)      |
|---|---|--|----------------------------------|---------------------------|------------------------|
|   |   |  | Typ <sup>(3)</sup>               | Limits <sup>(4)</sup>     |                        |
| $t_{SPICL}$   | SPI Clock Low Time                      |  |                                  | 125                       | ns (max)               |
| $t_{SPICH}$   | SPI Clock High Time                     |  |                                  | 125                       | ns (max)               |
| $f_{CLKI2C}$  | I <sup>2</sup> C_CLK Frequency          |  |                                  | 400                       | kHz (max)              |
| $t_{I2CHOLD}$   | I <sup>2</sup> C_DATA Hold Time         |  |                                  | 100                       | ns (max)               |
| $t_{I2CSET}$  | I <sup>2</sup> C_DATA Setup Time        |  |                                  | 100                       | ns (max)               |
| $V_{IH}$  | I <sup>2</sup> C/SPI Input High Voltage |  | I <sup>2</sup> C_V <sub>DD</sub> | $0.7 \times I^2C\_V_{DD}$ | V (min)                |
| $V_{IL}$  | I <sup>2</sup> C/SPI Input Low Voltage  |  | 0                                | $0.3 \times I^2C\_V_{DD}$ | V (max)                |
| <b>I<sup>2</sup>S(1.7V ≤ I/O_V<sub>DD</sub> ≤ 2.7V)</b> |   |  |                                  |                           |                        |
| $f_{CLKI^2S}$   | I <sup>2</sup> S_CLK Frequency          | I <sup>2</sup> S_RESOLUTION = 1<br>I <sup>2</sup> S_RESOLUTION = 0 | 1536<br>3072                     | 6144<br>12288             | kHz (max)<br>kHz (max) |
|   | I <sup>2</sup> S_WS Duty Cycle          |  | 50                               | 40<br>60                  | % (min)<br>% (max)     |
| $V_{IH}$  | Digital Input High Voltage              |  |                                  | $0.75 \times I/O\_V_{DD}$ | V (min)                |
| $V_{IL}$  | Digital Input Low Voltage               |  |                                  | $0.25 \times I/O\_V_{DD}$ | V (max)                |
| <b>I<sup>2</sup>S(2.7V ≤ I/O_V<sub>DD</sub> ≤ 4.0V)</b> |   |  |                                  |                           |                        |
| $f_{CLKI^2S}$   | I <sup>2</sup> S_CLK Frequency          | I <sup>2</sup> S_RESOLUTION = 0                                    | 1536<br>3072                     | 6144<br>12288             | kHz (max)<br>kHz (max) |
|   | I <sup>2</sup> S_WS Duty Cycle          | I <sup>2</sup> S_RESOLUTION = 1                                    | 50                               | 40<br>60                  | %<br>%                 |
| $V_{IH}$  | Digital Input High Voltage              |  |                                  | $0.7 \times I/O\_V_{DD}$  | V (min)                |
| $V_{IL}$  | Digital Input Low Voltage               |  |                                  | $0.3 \times I/O\_V_{DD}$  | V (max)                |

**Table 1. Output Noise  $AV_{DD} = 5.0V$  and  $AV_{DD} = 3.0V$ . All gains set to 0dB. Units in  $\mu V$ , A-weighted, Inputs terminated to ground.**

| MODE | EP | LS | HP OCL | Units   |
|------|----|----|--------|---------|
| 1    | 22 | 22 | 8      | $\mu V$ |
| 2    | 22 | 22 | 8      | $\mu V$ |
| 3    | 22 | 22 | 8      | $\mu V$ |
| 4    | 68 | 88 | 46     | $\mu V$ |
| 5    | 38 | 48 | 24     | $\mu V$ |
| 6    | 29 | 34 | 18     | $\mu V$ |
| 7    | 38 | 48 | 24     | $\mu V$ |

**Table 2. VPSRR  $AV_{DD} = 3.0V$ ,  $f_{RIPPLE} = 217Hz$ ;  $V_{RIPPLE} = 200mV_{P-P}$ ;  $C_B = 2.2\mu F$ ; All gains set to 0dB.**

| MODE | EP(Typ) | LS (Typ) | LS (Limit) | HP (Typ) | HP (Limit) | Units |
|------|---------|----------|------------|----------|------------|-------|
| 1    | 69      | 76       |            | 72       |            | dB    |
| 2    | 69      | 76       | 67         | 72       | 68         | dB    |
| 3    | 69      | 76       |            | 72       |            | dB    |
| 4    | 63      | 62       |            | 55       |            | dB    |
| 5    | 69      | 68       |            | 61       |            | dB    |
| 6    | 69      | 70       |            | 64       |            | dB    |
| 7    | 69      | 68       |            | 61       |            | dB    |

**Table 3. PSRR  $AV_{DD} = 5.0V$ ,  $f_{RIPPLE} = 217Hz$ ;  $V_{RIPPLE} = 200mV_{P-P}$ ;  $C_B = 2.2\mu F$ ; All gains set to 0dB.**

| MODE | EP (Typ) | LS (Typ) | HP (Typ) | Units |
|------|----------|----------|----------|-------|
| 1    | 68       | 72       | 71       | dB    |
| 2    | 68       | 72       | 71       | dB    |
| 3    | 68       | 72       | 71       | dB    |
| 4    | 68       | 66       | 69       | dB    |
| 5    | 68       | 69       | 70       | dB    |
| 6    | 69       | 72       | 71       | dB    |
| 7    | 68       | 69       | 70       | dB    |

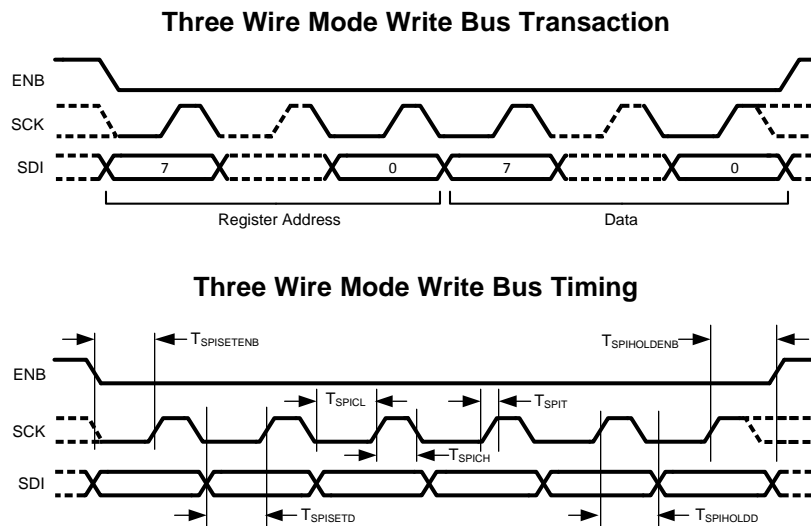
**Table 4. Dynamic Range and SNR.  $3.0V \leq AV_{DD} \leq 5.0V$ . All programmable gain set to 0dB. Units in dB.**

|    | DR (Typ) | SNR (Typ) | Units |
|----|----------|-----------|-------|
| LS | 95       | 85        | dB    |
| HP | 95       | 85        | dB    |
| EP | 97       | 85        | dB    |

## System Control

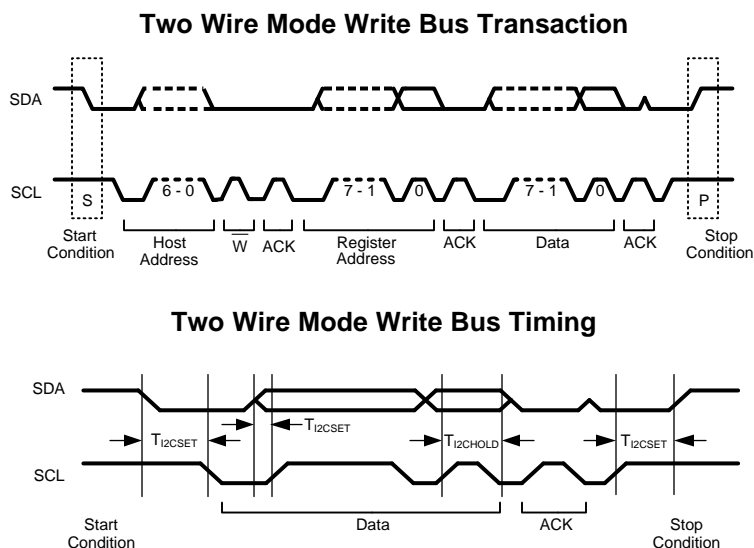
The LM49321 is controlled via either a two wire I<sup>2</sup>C compatible interface or three wire SPI interface, selectable with the MODE pin. This interface is used to configure the operating mode, interfaces, data converters, mixers and amplifiers. The LM49321 is controlled by writing 8 bit data into a series of write-only registers, the device is always a slave for both type of interfaces.

### THREE WIRE, SPI INTERFACE (MODE = 1)



**Figure 4. Three Wire Mode Write Bus**

When the part is configured as an SPI device and the enable (ENB) line is lowered the serial data on SDI is clocked in on the rising edge of the SCK line. The protocol used is 16bit, MSB first. The upper 8 bits (15:8) are used to select an address within the device, the lower 8 bits (7:0) contain the updated data for this register.

**TWO WIRE I<sup>2</sup>C COMPATIBLE INTERFACE (MODE = 0)****Figure 5. Two Wire Mode Write Bus**

When the part is configured as an I<sup>2</sup>C device then the LM49321 will respond to one of two addresses, according to the ADDR input. If ADDR is low then the address portion of the I<sup>2</sup>C transaction should be set to write to 0010000. When ADDR is high then the address input should be set to write to 1110000.

**Table 5. Chip Address**

|              | <b>A7</b> | <b>A6</b> | <b>A5</b> | <b>A4</b> | <b>A3</b> | <b>A2</b> | <b>A1</b> | <b>A0</b> |
|--------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Chip Address | 0         | EC        | EC        | 1         | 0         | 0         | 0         | 0         |
| ADR = 0      | 0         | 0         | 0         | 1         | 0         | 0         | 0         | 0         |
| ADR = 1      | 0         | 1         | 1         | 1         | 0         | 0         | 0         | 0         |

EC — Externally configured by ADR pin

**Table 6. Control Registers**

| Address | Register                 | D7              | D6           | D5             | D4                | D3                    | D2                    | D1                          | D0                            |
|---------|--------------------------|-----------------|--------------|----------------|-------------------|-----------------------|-----------------------|-----------------------------|-------------------------------|
| 00h     | MODE_CONTROL             | 0               | CD_6         | 0              | OCL               | MODE_CONTROL          |                       |                             |                               |
| 01h     | OUTPUT_CONTROL           | STEREO_OUT_ONLY | MONO_ONLY    | DAC_INPUT_ONLY | STEREO_INPUT_ONLY | HP_R_OUTPUT           | HP_L_OUTPUT           | LS_OUTPUT                   | MONO_OUTPUT                   |
| 02h     | EP_VOL                   | 0               | 0            | 0              | EP_VOL            |                       |                       |                             |                               |
| 03h     | LS_VOL                   | 0               | 0            | 0              | LS_VOL            |                       |                       |                             |                               |
| 04h     | RESERVED                 | 0               | 0            | 0              | 0                 | 0                     | 0                     | 0                           | 0                             |
| 05h     | HP_L_VOL                 | 0               | 0            | 0              | HP_L_VOL          |                       |                       |                             |                               |
| 06h     | HP_R_VOL                 | 0               | 0            | 0              | HP_R_VOL          |                       |                       |                             |                               |
| 07h     | ANALOG_INPUT_GAIN        | 0               | 0            | ANA_R_GAIN     |                   |                       | ANA_L_GAIN            |                             |                               |
| 08h     | ANALOG_DAC_GAIN          | 0               | DAC_R_GAIN   |                | DAC_L_GAIN        |                       | MONO_L_GAIN           |                             |                               |
| 09h     | CLOCKS                   | R_DIV           |              |                |                   | PLL_ENABLE            | AUDIO_CLK_SEL         | PLL_INPUT                   | FAST_CLOCK                    |
| 0Ah     | PLL_M                    | 0               | PLL_M        |                |                   |                       |                       |                             |                               |
| 0Bh     | PLL_N                    |                 |              |                |                   |                       |                       |                             |                               |
| 0Ch     | PLL_N_MOD                | VCO_FAS<br>T    | DITHER_LEVEL | DITHER_LEVEL   | PLL_N_MOD         |                       |                       |                             |                               |
| 0Dh     | PLL_P                    | 0               | 0            | 0              | 0                 | PLL_P                 |                       |                             |                               |
| 0Eh     | DAC_SET UP               | 0               | CUST_COMP    | DITHER_ALW_ON  | DITHER_OFF        | MUTE_R                | MUTE_L                | DAC_MODE                    |                               |
| 0Fh     | INTERFACE                | 0               | 0            | 0              | 0                 | I <sup>2</sup> C_FAST | I <sup>2</sup> S_MODE | I <sup>2</sup> S_RESOLUTION | I <sup>2</sup> S_MASTER_SLAVE |
| 10h     | COMPENSATION_C OEFF0_LSB |                 |              |                |                   |                       |                       |                             |                               |
| 11h     | COMPENSATION_C OEFF0_MSB |                 |              |                |                   |                       |                       |                             |                               |
| 12h     | COMPENSATION_C OEFF1_LSB |                 |              |                |                   |                       |                       |                             |                               |
| 13h     | COMPENSATION_C OEFF1_MSB |                 |              |                |                   |                       |                       |                             |                               |
| 14h     | COMPENSATION_C OEFF2_LSB |                 |              |                |                   |                       |                       |                             |                               |
| 15h     | COMPENSATION_C OEFF2_MSB |                 |              |                |                   |                       |                       |                             |                               |

## Mixer Control Registers

This register is used to control the different mixer modes that the LM49321 supports.

**Table 7. Mode Control Register (00h)<sup>(1)</sup>**

| Bits | Field        | Description  |      |               |                                    |                |                 |
|------|--------------|--|------|---------------|------------------------------------|----------------|-----------------|
| 3:0  | MODE_CONTROL | This sets the different mixer output modes.                                |      |               |                                    |                |                 |
|      |              | MODE_CONTROL   | Mode | Mono Earpiece | Loudspeaker                        | Headphone Left | Headphone Right |
|      |              | 0000   | 0    | SD            | SD                                 | SD             | SD              |
|      |              | 1001   | 1    | M             | M                                  | M              | M               |
|      |              | 1010   | 2    | AL+AR         | AL+AR                              | AL             | AR              |
|      |              | 1011   | 3    | M+AL+AR       | M+AL+AR                            | M+AL           | M+AR            |
|      |              | 1100   | 4    | DL+DR         | DL+DR                              | DL             | DR              |
|      |              | 1101   | 5    | DL+DR+AL+AR   | DL+DR+AL+AR                        | DL+AL          | DR+AR           |
|      |              | 1110   | 6    | M+DL+DR+AL+AR | M+DL+DR+AL+AR                      | M+DL+AL        | M+DR+AR         |
|      |              | 1111   | 7    | M+DL+DR       | M+DL+DR                            | M+DL           | M+DR            |
| 4    | OCL          | This sets the headphone output to use output capacitor-less configuration. |      |               |                                    |                |                 |
|      |              | OCL  |      |               | Headphone output configuration     |                |                 |
|      |              | 0  |      |               | Cap-coupled Single-ended Mode (SE) |                |                 |
|      |              | 1  |      |               | Output capacitor-less (OCL)        |                |                 |

- (1) SD — Shutdown  
M — Mono Differential Input  
AL — Analog Left Channel  
AR — Analog Right Channel  
DL — I2S DAC Left Channel  
DR — I2S DAC Right Channel  
Note: Power-On Default Mode is Mode 0

This register is used to control the different output configurations.

**Table 8. Output Control (01h)**

| Bits | Field       | Description                               |  |
|------|-------------|---|--|
| 0    | EP_OUTPUT   | This enables the Mono Earpiece output.    |  |
|      |             | EP_OUTPUT                                 | Status   |
|      |             | 0   | Mono earpiece output off                                 |
|      |             | 1   | Mono earpiece output on                                  |
| 1    | LS_OUTPUT   | This enables the Mono Loudspeaker output. |  |
|      |             | LS_OUTPUT                                 | Status   |
|      |             | 0   | Loudspeaker output off                                   |
|      |             | 1   | Loudspeaker output on                                    |
| 2    | HP_L_OUTPUT | This enables the Headphone left output.   |  |
|      |             | HP_L_OUTPUT                               | Status   |
|      |             | 0   | Headphone left output off. If OCL=1, output is in mute.  |
|      |             | 1   | Headphone left output on                                 |
| 3    | HP_R_OUTPUT | This enables the Headphone right output.  |  |
|      |             | HP_R_OUTPUT                               | Status   |
|      |             | 0   | Headphone right output off. If OCL=1, output is in mute. |
|      |             | 1   | Headphone right output on                                |

**Table 8. Output Control (01h) (continued)**

| Bits | Field              | Description  |
|------|--------------------|--|
| 4    | STEREO_INPUT_ONLY  | This enables the analog left (AL) and analog right (AR) and disables all other inputs.   |
|      |                    | STEREO_INPUT_ONLY      Status  |
|      |                    | 0      Normal  |
|      |                    | 1      Enables AL and AR inputs only   |
| 5    | DAC_INPUT_ONLY     | This enables the DAC left (DL) and analog right (DR) and disables all other inputs.  |
|      |                    | DAC_INPUT_ONLY      Status   |
|      |                    | 0      Normal  |
|      |                    | 1      Enables DL and DR inputs only   |
| 6    | MONO_ONLY          | This enables mono earpiece (EP) and loudspeaker (LS) outputs MUX and disables the headphone outputs MUX. Enabling this mode can save up to 400µA of current. |
|      |                    | MONO_ONLY      Status  |
|      |                    | 0      Normal  |
|      |                    | 1      Enable mono earpiece and loudspeaker outputs MUX  |
| 7    | STEREO_OUTPUT_ONLY | This enables the headphone output MUX only and disables all other output MUX's. Enabling this mode can save up to 200µA of current.                          |
|      |                    | STEREO_OUTPUT_ONLY      Status   |
|      |                    | 0      Normal  |
|      |                    | 1      Enables the headphone output MUX  |

## Volume Control Registers

These registers are used to control output volume control levels for Earpiece, Loudspeaker and Headphone.

**Table 9. Volume Control Register**  
**EP\_VOL (02h), LS\_VOL (03h), HP\_L\_VOL (05h), HP\_R\_VOL (06h)**

| Bits | Field                                    | Description   |            |
|------|--|---|------------|
| 4:0  | EP_VOL<br>LS_VOL<br>HP_L_VOL<br>HP_R_VOL | This programs the Earpiece, Loudspeaker and Headphone volume level. |            |
|      |  | VOL   | Level (dB) |
|      |  | 00000   | MUTE       |
|      |  | 00001   | –56        |
|      |  | 00010   | –52        |
|      |  | 00011   | –48        |
|      |  | 00100   | –45        |
|      |  | 00101   | –42        |
|      |  | 00110   | –39        |
|      |  | 00111   | –36        |
|      |  | 01000   | –33        |
|      |  | 01001   | –30        |
|      |  | 01010   | –28        |
|      |  | 01011   | –26        |
|      |  | 01100   | –24        |
|      |  | 01101   | –22        |
|      |  | 01110   | –20        |
|      |  | 01111   | –18        |
|      |  | 10000   | –16        |
|      |  | 10001   | –14        |
|      |  | 10010   | –12        |
|      |  | 10011   | –10        |
|      |  | 10100   | –8         |
|      |  | 10101   | –6         |
|      |  | 10110   | –4         |
|      |  | 10111   | –3         |
|      |  | 11000   | –2         |
|      |  | 11001   | –1         |
|      |  | 11010   | 0          |
|      |  | 11011   | 1          |
|      |  | 11100   | 2          |
|      |  | 11101   | 3          |
|      |  | 11110   | 4          |
|      |  | 11111   | 5          |

This register is used to control input gain for left and right analog inputs.

**Table 10. Analog Left and Right Input Control (07h)**

| Bits | Field      | Description                               |
|------|------------|---|
| 2:0  | ANA_L_GAIN | This program the analog left input gain.  |
|      |            | ANA_L_GAIN      Level (dB)                |
|      |            | 000      –6                               |
|      |            | 001      –3                               |
|      |            | 010      0                                |
|      |            | 011      3                                |
|      |            | 100      6                                |
|      |            | 101      9                                |
|      |            | 110      12                               |
|      |            | 111      15                               |
| 5:3  | ANA_R_GAIN | This program the analog Right input gain. |
|      |            | ANA_R_GAIN      Level (dB)                |
|      |            | 000      –6                               |
|      |            | 001      –3                               |
|      |            | 010      0                                |
|      |            | 011      3                                |
|      |            | 100      6                                |
|      |            | 101      9                                |
|      |            | 110      12                               |
|      |            | 111      15                               |

This register is sued to control input gain for Mono, DAC left and right inputs.

**Table 11. Mono and DAC Input Gain Control (08h)**

| Bits | Field        | Description                           |
|------|--------------|---------------------------------------|
| 2:0  | MONO_IN_GAIN | This program the mono input gain.     |
|      |              | MONO_IN_GAIN      Level (dB)          |
|      |              | 000      –12                          |
|      |              | 001      –9                           |
|      |              | 010      –6                           |
|      |              | 011      –3                           |
|      |              | 100      0                            |
|      |              | 101      3                            |
|      |              | 110      6                            |
|      |              | 111      9                            |
| 4:3  | DAC_L_GAIN   | This program the DAC left input gain. |
|      |              | DAC_L_GAIN      Level (dB)            |
|      |              | 00      –3                            |
|      |              | 01      0                             |
|      |              | 10      3                             |
|      |              | 11      6                             |

**Table 11. Mono and DAC Input Gain Control (08h) (continued)**

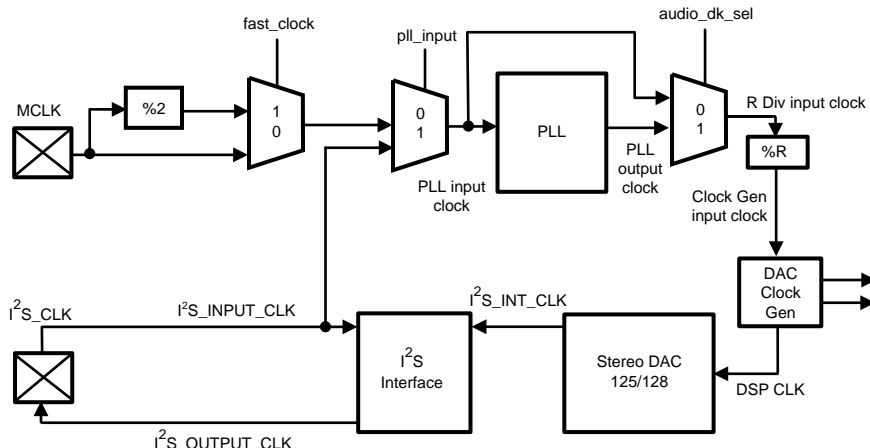
| Bits | Field      | Description                            |
|------|------------|--|
| 6:5  | DAC_R_GAIN | This program the DAC Right input gain. |
|      |            | DAC_R_GAIN      Level (dB)             |
|      |            | 00      –3                             |
|      |            | 01      0                              |
|      |            | 10      3                              |
|      |            | 11      6                              |

## Clock Configuration Register

This register is used to control the multiplexers and clock R divider in the clock module.

**Table 12. CLOCK (09h)**

| Bits | Register      | Description   |
|------|---------------|---|
| 0    | FAST_CLOCK    | If set master clock is divided by two.                |
|      |               | FAST_CLOCK      MCLK Frequency                        |
|      |               | 0      Normal   |
|      |               | 1      Divided by 2                                   |
| 1    | PLL_INPUT     | Programs the PLL input multiplexer to select:         |
|      |               | PLL_INPUT      PLL Input Source                       |
|      |               | 0      MCLK   |
| 2    | AUDIO_CLK_SEL | Selects which clock is passed to the audio sub-system |
|      |               | DAC_CLK_SEL      DAC Sub-system Input Source          |
|      |               | 0      PLL Input                                      |
|      |               | 1      PLL Output                                     |
| 3    | PLL_ENABLE    | If set enables the PLL. (MODES 4–7 only)              |
| 7:4  | R_DIV         | Programs the R divider                                |
|      |               | R_DIV      Divide Value                               |
|      |               | 0000      1   |
|      |               | 0001      1   |
|      |               | 0010      1.5   |
|      |               | 0011      2   |
|      |               | 0100      2.5   |
|      |               | 0101      3   |
|      |               | 0110      3.5   |
|      |               | 0111      4   |
|      |               | 1000      4.5   |
|      |               | 1001      5   |
|      |               | 1010      5.5   |
|      |               | 1011      6   |
|      |               | 1100      6.5   |
|      |               | 1101      7   |
|      |               | 1110      7.5   |
|      |               | 1111      8   |



By default the stereo DAC operates at  $250 \times f_s$ , i.e. 12.000MHz (at the clock generator input clock) for 48kHz data. It is expected that the PLL be used to drive the audio system unless a 12.000MHz master clock is supplied. The PLL can also use the I2S clock input as a source. In this case, the audio DAC uses the clock from the output of the PLL.

### Common Clock Settings for the DAC

The DAC can work in 4 modes, each with different oversampling rates, 125,128,64 and 32. In normal operation 125x oversampling provides for the simplest clocking solution as it will work from 12.000MHz (common in most systems with Bluetooth or USB) at 48kHz exactly. The other modes are useful if data is being provided to the DAC from an uncontrollable isochronous source (such as a CD player, DAB, or other external digital source) rather than being decoded from memory. In this case the PLL can be used to derive a clock for the DAC from the I2S clock.

The DAC oversampling rate can be changed to allow simpler clocking strategies, this is controlled in the DAC SETUP register but the oversampling rates are as follows:

| DAC MODE | Over sampling Ratio Used |
|----------|--------------------------|
| 00       | 125                      |
| 01       | 128                      |
| 10       | 64                       |
| 11       | 32                       |

The following table describes the clock required at the clock generator input for various clock sample rates in the different DAC modes:

| Fs (kHz) | DAC Oversampling Ratio | Required CLock at DAC Clock Generator Input (MHz) |
|----------|------------------------|---|
| 8        | 125                    | 2   |
| 8        | 128                    | 2.048   |
| 11.025   | 125                    | 2.75625   |
| 11.025   | 128                    | 2.8224  |
| 12       | 125                    | 3   |
| 12       | 128                    | 3.072   |
| 16       | 125                    | 4   |
| 16       | 128                    | 4.096   |
| 22.05    | 125                    | 5.5125  |
| 22.05    | 128                    | 5.6448  |
| 24       | 125                    | 6   |
| 24       | 128                    | 6.144   |

| Fs (kHz) | DAC Oversampling Ratio | Required CLock at DAC Clock Generator Input (MHz) |
|----------|------------------------|---|
| 32       | 125                    | 8   |
| 32       | 128                    | 8.192   |
| 44.1     | 125                    | 11.025  |
| 44.1     | 128                    | 11.2896   |
| 48       | 125                    | 12  |
| 48       | 128                    | 12.288  |
| 88.2     | 64                     | 11.2896   |
| 96       | 64                     | 12.288  |
| 176.4    | 32                     | 22.5792   |
| 192      | 32                     | 24.576  |

Methods for producing these clock frequencies are described in the [PLL](#) section.

The R divider can be used when the master clock is exactly 12.00 MHz in order to generate different sample rates. The Table below shows different sample rates supported from 12.00MHz by using only the R divider and disabling the PLL. In this way we can save power and the clock jitter will be low.

| R_DIV | Divide Value | DAC Clock Generator Input Frequency <MHz> | Sample Rate Supported <KHz> |
|-------|--------------|---|-----------------------------|
| 11    | 6            | 2   | 8                           |
| 9     | 5            | 2.4                                       | 9.6                         |
| 7     | 4            | 3   | 12                          |
| 5     | 3            | 4   | 16                          |
| 4     | 2.5          | 4.8                                       | 19.2                        |
| 3     | 2            | 6   | 24                          |
| 2     | 1.5          | 8   | 32                          |
| 0     | 1            | 12  | 48                          |

The R divider can also be used along with the P divider in order to create the clock needed to support low sample rates.

## PLL Configuration Registers

### PLL M DIVIDER CONFIGURATION REGISTER

This register is used to control the input divider of the PLL.

**Table 13. PLL\_M (0Ah)<sup>(1)</sup>**

| Bits | Register | Description                               |
|------|----------|---|
| 6:0  | PLL_M    | Programs the PLL input divider to select: |
|      |          | PLL_M                                     |
|      |          | Divide Ratio                              |
|      |          | 0000000                                   |
|      |          | Divider Off                               |
|      |          | 0000001                                   |
|      |          | 1   |
|      |          | 0000010                                   |
|      |          | 1.5                                       |
|      |          | 0000011                                   |
|      |          | 2   |
|      |          | 0000100                                   |
|      |          | 2.5                                       |
|      |          | ...                                       |
|      |          | 1111110                                   |
|      |          | 63.5                                      |

- (1) The M divider should be set such that the output of the divider is between 0.5 and 5MHz. See the PLL setup section for details.  
 The division of the M divider is derived from PLL\_M as such:  
 $M = (PLL\_M + 1) / 2$

## PLL N DIVIDER CONFIGURATION REGISTER

This register is used to control PLL N divider.

**Table 14. PLL\_N (0Bh)<sup>(1)</sup>**

| Bits | Register | Description                        |              |
|------|----------|------------------------------------|--------------|
| 7:0  | PLL_N    | Programs the PLL feedback divider: |              |
|      |          | PLL_N                              | Divide Ratio |
|      |          | 00000000                           | Divider Off  |
|      |          | 00000001 → 00001010                | 10           |
|      |          | 00001011                           | 11           |
|      |          | 00001100                           | 12           |
|      |          | ...                                | ...          |
|      |          | 11111000                           | 248          |
|      |          | 11111001                           | 249          |

(1) The N divider should be set such that the output of the divider is between 0.5 and 5MHz. See the PLL setup section for details. The N divider should never be set so that  $(F_{in}/M) * N > 55\text{MHz}$  (or 80MHz if FAST\_VCO is set in the PLL\_N\_MOD register).

The non-sigma-delta division of the N divider is derived from the PLL\_N as such:

$$N = \text{PLL\_N}$$

$F_{in}/M$  is often referred to as  $F_{comp}$  (Frequency of Comparison) or  $F_{ref}$  (Reference Frequency). In this document,  $F_{comp}$  is used

## PLL P DIVIDER CONFIGURATION REGISTER

This register is used to control the PLL's P divider.

**Table 15. PLL\_P<sup>(1)</sup>**

| Bits | Register | Description                               |             |
|------|----------|---|-------------|
| 3:0  | PLL_P    | Programs the PLL input divider to select: |             |
|      |          | 0000                                      | Divider Off |
|      |          | 0001                                      | 1           |
|      |          | 0010                                      | 1.5         |
|      |          | 0011                                      | 2           |
|      |          | ...                                       | → 2.5       |
|      |          | 1101                                      | 7           |
|      |          | 1110                                      | 7.5         |
|      |          | 1111                                      | 8           |

(1) The output of this divider should be either 12 or 24MHz in USB mode or 11.2896MHz, 12.288MHz or 24.576MHz in non-USB modes.

The division of the P divider is derived from PLL\_P as such:

$$P = (\text{PLL\_P} + 1) / 2$$

## PLL N MODULATOR AND DITHER SELECT CONFIGURATION REGISTER

This register is used to control the Fractional component of the PLL.

**Table 16. PLL\_N\_MOD (0Ch)<sup>(1)</sup>**

| Bits | Register     | Description  |                             |
|------|--------------|--|-----------------------------|
| 4:0  | PLL_N_MOD    | This programs the PLL N Modulator's fractional component:  |                             |
|      |              | PLL_N_MOD  | Fractional Addition         |
|      |              | 00000  | 0/32                        |
|      |              | 00001  | 1/32                        |
|      |              | 00010 → 11110  | 2/32 → 30/32                |
| 6:5  | DITHER_LEVEL | Allows control over the dither used by the N Modulator     |                             |
|      |              | DITHER_LEVEL   | DAC Sub-system Input Source |
|      |              | 00   | Medium (32)                 |
|      |              | 01   | Small (16)                  |
|      |              | 10   | Large (48)                  |
| 7    | VCO_FAST     | If set the VCO maximum and minimum frequencies are raised: |                             |
|      |              | VCO_FAST   | Maximum F <sub>VCO</sub>    |
|      |              | 0  | 40–55MHz                    |

(1) The complete N divider is a fractional divider as such:

$$N = \text{PLL\_N} + (\text{PLL\_N\_MOD}/32)$$

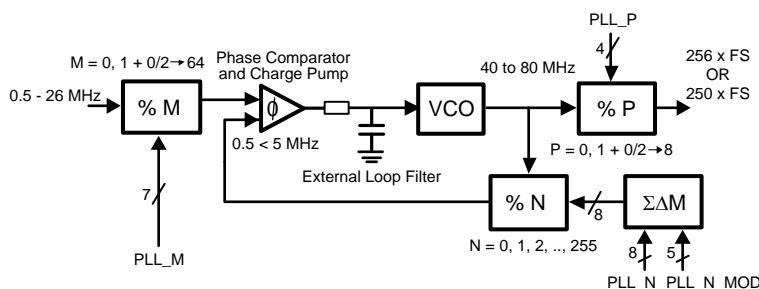
If the modulus input is zero, then the N divider is simply an integer N divider. The output from the PLL is determined by the following formula:

$$F_{\text{out}} = (F_{\text{in}} * N) / (M * P)$$

Please see over for more details on the PLL and common settings.

## Further Notes on PLL Programming

The sigma-delta PLL is designed to drive audio circuits requiring accurate clock frequencies of up to 25MHz with frequency errors noise-shaped away from the audio band. The 5 bits of modulus control provide exact synchronization of 48kHz and 44.1kHz sample rates from any common clock source when the oversampling rate of the audio system is 128fs. In systems where 128x oversampling must be used (for example with an isochronous I<sup>2</sup>S data stream) a clock synchronous to the sample rate should be used as input to the PLL (typically the I<sup>2</sup>S clock). If no isochronous source is available then the PLL can be used to obtain a clock that is accurate to within typical crystal tolerances of the real sample rate.



**Table 17. Example Of PLL Settings For 48Khz Sample Rates**

| f_in (MHz) | fsamp (kHz) | M    | N        | P | PLL_M | PLL_N | PLL_N_MOD | PLL_P | f_out (MHz) |
|------------|-------------|------|----------|---|-------|-------|-----------|-------|-------------|
| 11         | 48          | 11   | 60       | 5 | 21    | 60    | 0         | 9     | 12          |
| 12         | 48          | 5    | 25       | 5 | 9     | 25    | 0         | 9     | 12          |
| 12.288     | 48          | 4    | 19.53125 | 5 | 7     | 19    | 17        | 9     | 12          |
| 13         | 48          | 13   | 60       | 5 | 25    | 60    | 0         | 9     | 12          |
| 14.4       | 48          | 9    | 37.5     | 5 | 17    | 37    | 16        | 9     | 12          |
| 16.2       | 48          | 27   | 100      | 5 | 53    | 100   | 0         | 9     | 12          |
| 16.8       | 48          | 14   | 50       | 5 | 27    | 50    | 0         | 9     | 12          |
| 19.2       | 48          | 13   | 40.625   | 5 | 25    | 40    | 20        | 9     | 12          |
| 19.44      | 48          | 27   | 100      | 6 | 53    | 100   | 0         | 11    | 12          |
| 19.68      | 48          | 20.5 | 62.5     | 5 | 40    | 62    | 16        | 9     | 12          |
| 19.8       | 48          | 16.5 | 50       | 5 | 32    | 50    | 0         | 9     | 12          |

**Table 18. Example PLL Settings For 44.1Khz Sample Rates**

| f_in (MHz) | fsamp (kHz) | M    | N        | P | PLL_M | PLL_N | PLL_N_MOD | PLL_P | f_out (MHz) |
|------------|-------------|------|----------|---|-------|-------|-----------|-------|-------------|
| 11         | 44.1        | 11   | 55.125   | 5 | 21    | 55    | 4         | 9     | 11.025000   |
| 11.2896    | 44.1        | 8    | 39.0625  | 5 | 15    | 39    | 2         | 9     | 11.025000   |
| 12         | 44.1        | 5    | 22.96875 | 5 | 9     | 22    | 31        | 9     | 11.025000   |
| 13         | 44.1        | 13   | 55.125   | 5 | 25    | 55    | 4         | 9     | 11.025000   |
| 14.4       | 44.1        | 12   | 45.9375  | 5 | 23    | 45    | 30        | 9     | 11.025000   |
| 16.2       | 44.1        | 9    | 30.625   | 5 | 17    | 30    | 20        | 9     | 11.025000   |
| 16.8       | 44.1        | 17   | 55.78125 | 5 | 33    | 55    | 25        | 9     | 11.025000   |
| 19.2       | 44.1        | 16   | 45.9375  | 5 | 31    | 45    | 30        | 9     | 11.025000   |
| 19.44      | 44.1        | 13.5 | 38.28125 | 5 | 26    | 38    | 9         | 9     | 11.025000   |
| 19.68      | 44.1        | 20.5 | 45.9375  | 4 | 40    | 45    | 30        | 7     | 11.025000   |
| 19.8       | 44.1        | 11   | 30.625   | 5 | 21    | 30    | 20        | 9     | 11.025000   |

These tables cover the most common applications, obtaining clocks for sample rates such as 22.05kHz and 192kHz should be done by changing the P divider value or the R divider in the clock configuration diagram.

If the user needs to obtain a clock unrelated to those described above, the following method is advised. An example of obtaining 11.2896 from 12.000MHz is shown below.

Choose a small range of P so that the VCO frequency is swept between 45 and 55MHz (or 60-80MHz if VCOFAST is used). Remembering that the P divider can divide by half integers. So for  $P = 4.0 \rightarrow 7.0$  sweep the M inputs from 2.5  $\rightarrow$  24. The most accurate N and N\_MOD can be calculated by:

$$N = \text{FLOOR}(((F_{\text{out}}/F_{\text{in}}) * (P * M)), 1)$$

$$N\_MOD = \text{ROUND}(32 * (((F_{\text{out}}/F_{\text{in}}) * (P * M)) - N), 0)$$

This shows that setting  $M = 11.5$ ,  $N = 75$ ,  $N\_MOD = 47$ ,  $P = 7$  gives a comparison frequency of just over 1MHz, a VCO frequency of just under 80MHz (so VCO\_FAST must be set) and an output frequency of 11.289596 which gives a sample rate of 44.099985443kHz, or accurate to 0.33 ppm.

Care must be taken when synchronization of isochronous data is not possible, i.e. when the PLL has to be used in the above mode. The I2S should be master on the LM49321 so that the data source can support appropriate SRC as required. This method should only be used with data being read on demand to eliminate sample rate mismatch problems.

Where a system clock exists at an integer multiple of the required DAC clock rate it is preferable to use this rather than the PLL. The LM49321 is designed to work in 8,12,16,24,32, and 48kHz modes from a 12MHz clock without the use of the PLL. This saves power and reduces clock jitter.

## DAC Setup Register

This register is used to configure the basic operation of the stereo DAC.

**Table 19. DAC\_SETUP (0Eh)**

| Bits | Register            | Description   |                   |                        |                         |
|------|---------------------|---|-------------------|------------------------|-------------------------|
| 1:0  | DAC_MODE            | The DAC used in the LM49321 can operate in one of 4 oversampling modes. The modes are described as follows:   |                   |                        |                         |
|      |                     | DAC_MODE  | Oversampling Rate | Typical f <sub>s</sub> | MCLK Required           |
|      |                     | 00  | 125               | 48KHz                  | 12.000MHz (USB Mode)    |
|      |                     | 01  | 128               | 44.1KHz<br>48KHz       | 11.2896MHz<br>12.288MHz |
|      |                     | 10  | 64                | 96KHz                  | 12.288MHz               |
|      |                     | 11  | 32                | 192KHz                 | 24.576MHz               |
| 2    | MUTE_L              | Mutes the left DAC channel on the next zero crossing.   |                   |                        |                         |
| 3    | MUTE_R              | Mutes the right DAC channel on the next zero crossing.  |                   |                        |                         |
| 4    | DITHER_OFF          | If set the dither in DAC is disabled.   |                   |                        |                         |
| 5    | DITHER<br>ALWAYS_ON | If set the dither in DAC is enabled all the time.   |                   |                        |                         |
| 6    | CUST_COMP           | If set the DAC frequency response can be programmed manually via a 5 tap FIR “compensation” filter. This can be used to enhance the frequency response of small loudspeakers or provide a crude tone control. The compensation Coefficients can be set by using registers 10h to 15h. |                   |                        |                         |

## Interface Control Register

This register is used to control the I<sup>2</sup>S and I<sup>2</sup>C compatible interface on the chip.

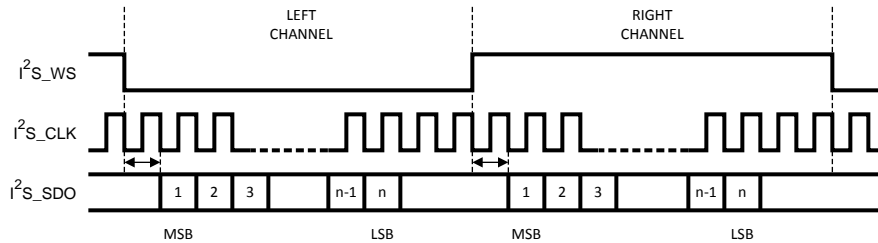
**Table 20. INTERFACE (0Fh)<sup>(1)</sup>**

| Bits | Field                         | Description  |   |
|------|-------------------------------|--|---|
| 0    | I <sup>2</sup> S_MASTER_SLAVE | This enables I <sup>2</sup> S in master or slave mode.   |   |
|      |                               | I <sup>2</sup> S_MASTER_SLAVE  | Comments  |
|      |                               | 0  | LM49321 acts as a slave where both I <sup>2</sup> S clock and word select are configured as inputs.                                       |
|      |                               | 1  | LM49321 acts as a master for I <sup>2</sup> S, so both I <sup>2</sup> S clock and I <sup>2</sup> S word select are configured as outputs. |
| 1    | I <sup>2</sup> S_RESOLUTION   | This set the I <sup>2</sup> S resolution and affects the I <sup>2</sup> S Interface in master mode. In slave mode the I <sup>2</sup> S Interface can support any I <sup>2</sup> S compatible resolution. In master mode the I <sup>2</sup> S resolution also depends on the DAC mode as the note below explains. |   |
|      |                               | I <sup>2</sup> S_RESOLUTION  | Comments  |
|      |                               | 0  | I <sup>2</sup> S resolution is set to 16 bits.  |
|      |                               | 1  | I <sup>2</sup> S resolution is set to 32 bits.  |
| 2    | I <sup>2</sup> S_MODE         | This set the I <sup>2</sup> S mode timing.   |   |
|      |                               | I <sup>2</sup> S_MODE  | Comments  |
|      |                               | 0  | I <sup>2</sup> S interface is configured in normal I <sup>2</sup> S mode timing.  |
|      |                               | 1  | I <sup>2</sup> S is configured in left justified mode timing.   |

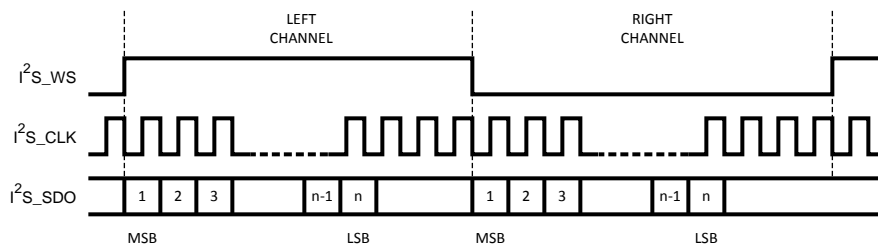
(1) The master I<sup>2</sup>S format depends on the DAC mode. In USB mode the number of bits per word is 25 (i.e. 2.4MHz for a 48kHz sample rate). The duty cycle is 40/60. In non-USB modes the format is 32 or 16 bits per word, depending on I<sup>2</sup>S\_RESOLUTION and the duty cycle is always 50-50. In slave mode it will decode any I<sup>2</sup>S compatible data stream.

**Table 20. INTERFACE (0Fh)<sup>(1)</sup> (continued)**

| Bits | Field                 | Description  |
|------|-----------------------|--|
| 3    | I <sup>2</sup> C_FAST | This set the I <sup>2</sup> C Clock speed.   |
|      |                       | I <sup>2</sup> C_FAST  |
|      |                       | 0  |
|      |                       | 1  |
|      |                       | Comments   |
|      |                       | I <sup>2</sup> C speed gets its default value of a maximum of 400kHz.                              |
|      |                       | This enables the I <sup>2</sup> C to run in fast mode with an I <sup>2</sup> C clock up to 3.4MHz. |



**Figure 6. I<sup>2</sup>S Mode Timing**



**Figure 7. Left Justified Mode Timing**

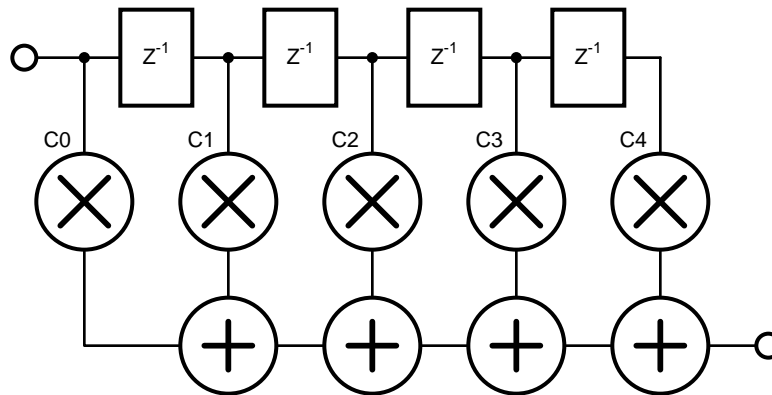
## FIR Compensation Filter Configuration Registers

These registers are used to configure the DAC's FIR compensation filter. Three 16 bit coefficients are required and must be programmed via the I2C/SPI Interface in bytes as follows:

**Table 21. COMP\_COEFF (10h → 15h)<sup>(1)</sup>**

| Address | Register        | Description  |
|---------|-----------------|--|
| 10h     | COMP_COEFF0_LSB | Bits [7:0] of the 1st and 5th FIR tap (C0 and C4)  |
| 11h     | COMP_COEFF0_MSB | Bits [15:8] of the 1st and 5th FIR tap (C0 and C4) |
| 12h     | COMP_COEFF1_LSB | Bits [7:0] of the 2nd and 4th FIR tap (C1 and C3)  |
| 13h     | COMP_COEFF1_MSB | Bits [15:8] of the 2nd and 4th FIR tap (C1 and C3) |
| 14h     | COMP_COEFF2_LSB | Bits [7:0] of the 3rd FIR tap (C2)                 |
| 15h     | COMP_COEFF2_MSB | Bits [15:8] of the 3rd FIR tap (C2)                |

(1) The filter must be phase linear to ensure the data keeps the correct stereo imaging so the second half of the FIR filter must be the reverse of the 1st half.

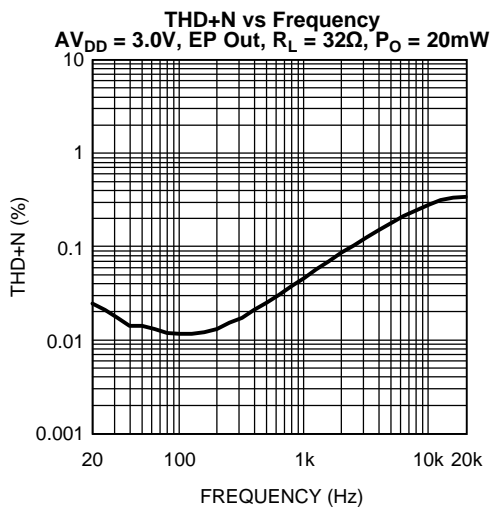


If the CUST\_COMP option in register 0Eh is not set the FIR filter will use its default values for a linear response from the DAC into the analog mixer, these values are:

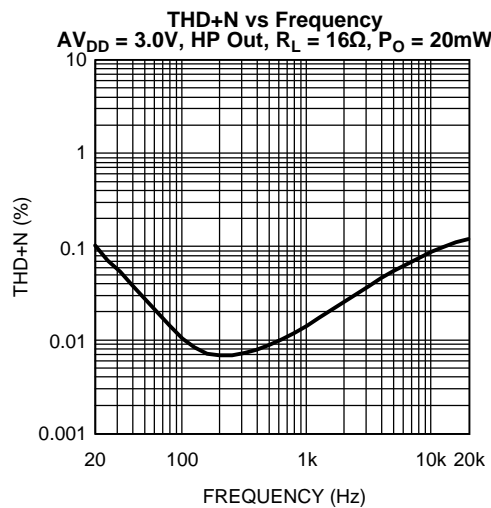
| DAC_OSR    | C0, C4 | C1, C3 | C2    |
|------------|--------|--------|-------|
| 00         | 434    | -2291  | 26984 |
| 01, 10, 11 | 61     | -371   | 25699 |

If using 96 or 192kHz data then the custom compensation may be required to obtain flat frequency responses above 24kHz. The total power of any custom filter must not exceed that of the above examples or the filters within the DAC will clip. The coefficient must be programmed in 2's complement.

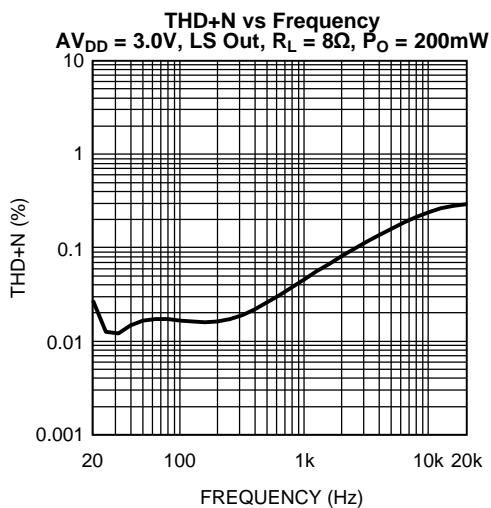
## Typical Performance Characteristics



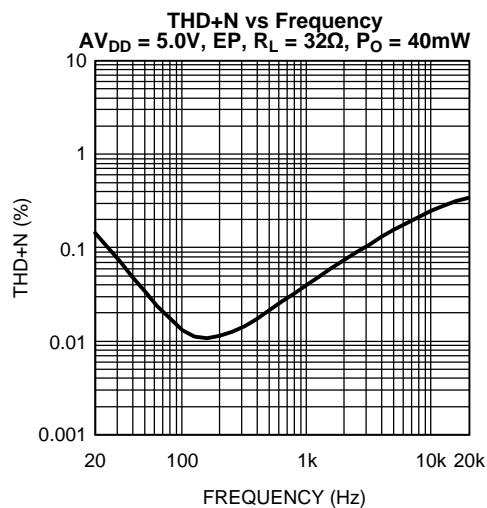
**Figure 8.**



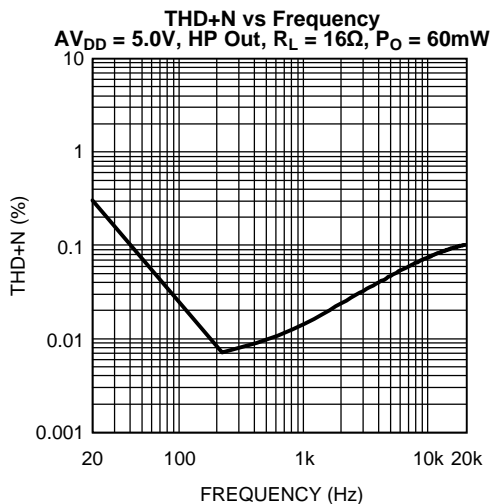
**Figure 9.**



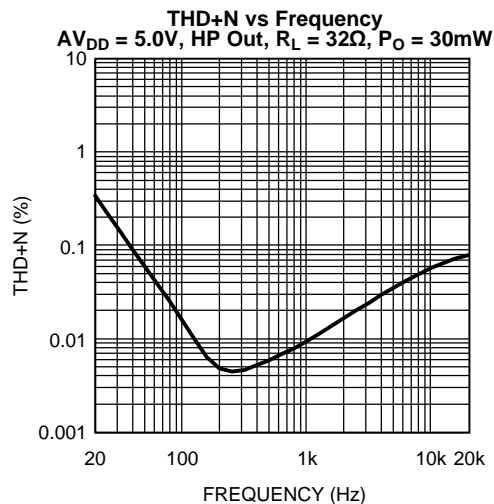
**Figure 10.**



**Figure 11.**



**Figure 12.**



**Figure 13.**

### Typical Performance Characteristics (continued)

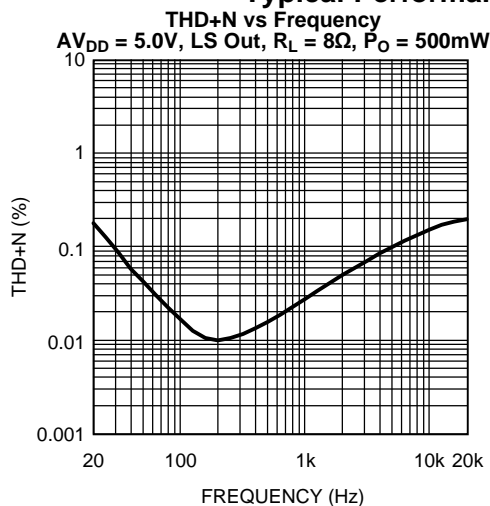


Figure 14.

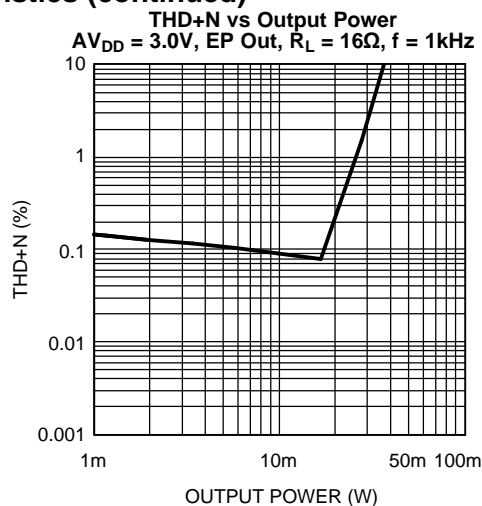


Figure 15.

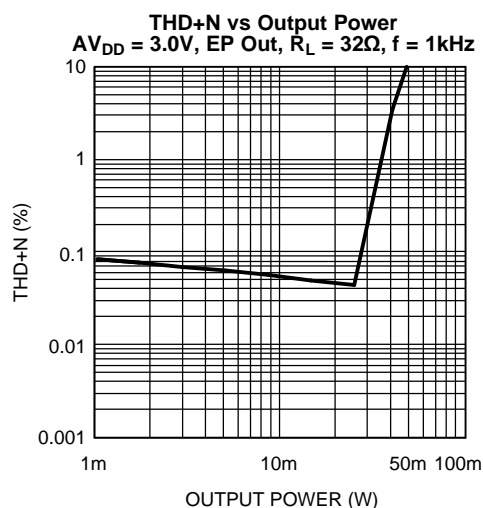


Figure 16.

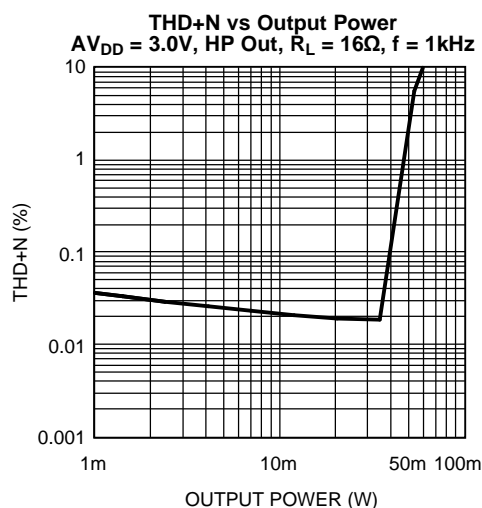


Figure 17.

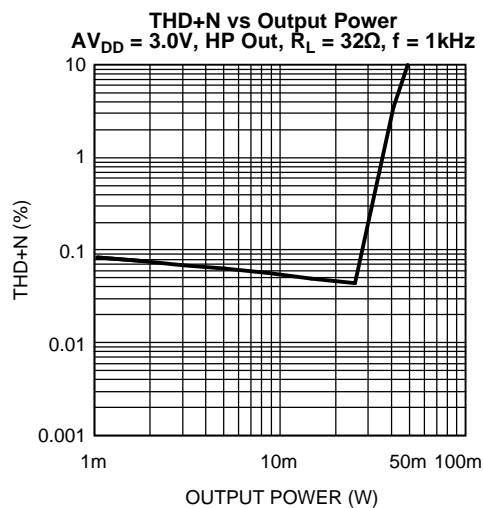


Figure 18.

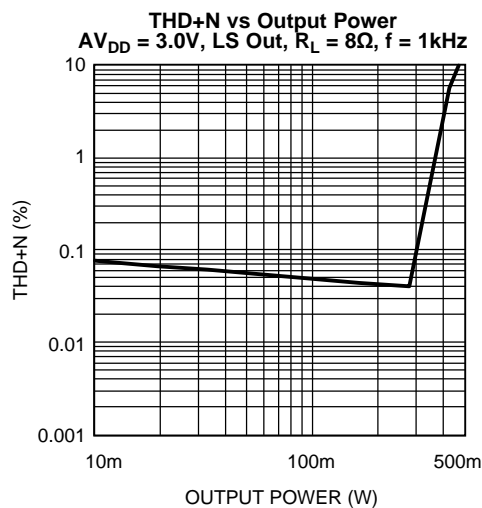


Figure 19.

## Typical Performance Characteristics (continued)

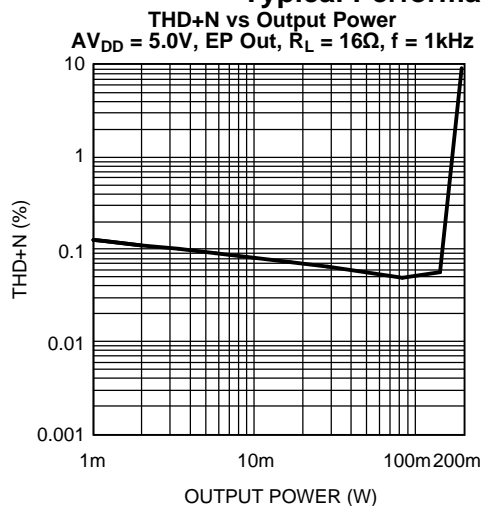


Figure 20.

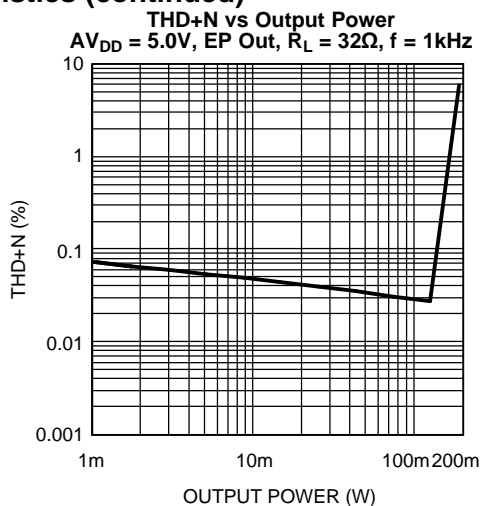


Figure 21.

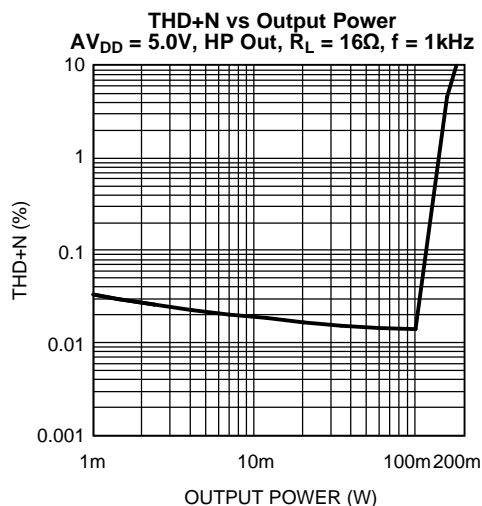


Figure 22.

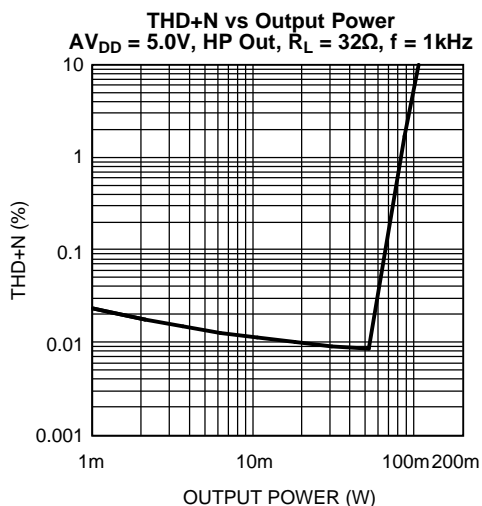


Figure 23.

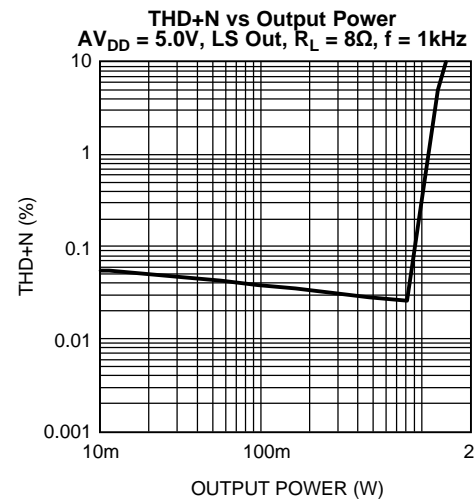


Figure 24.

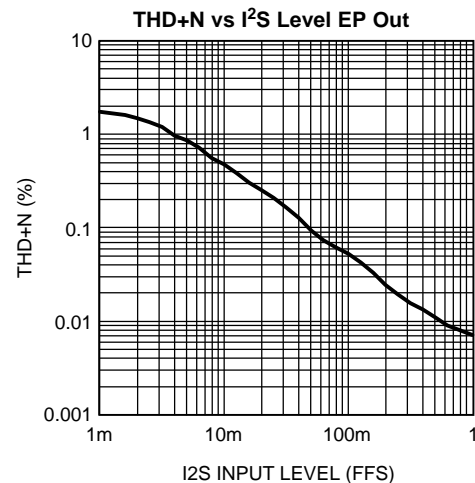


Figure 25.

### Typical Performance Characteristics (continued)

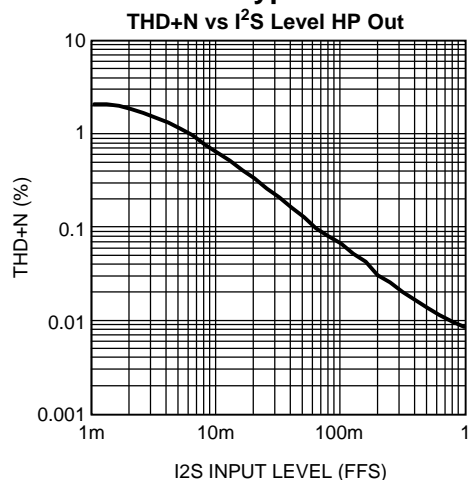


Figure 26.

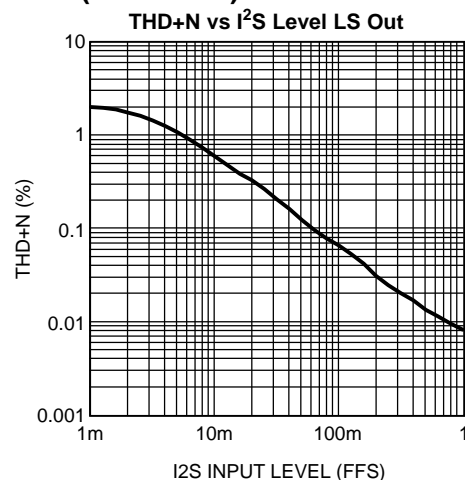


Figure 27.

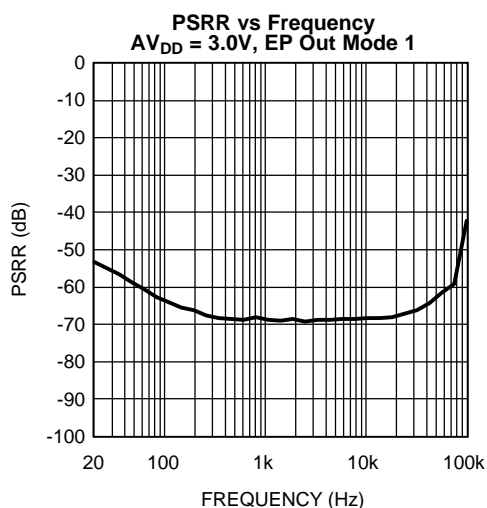


Figure 28.

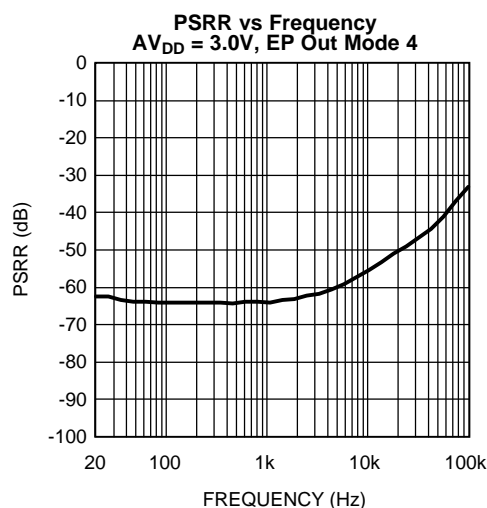


Figure 29.

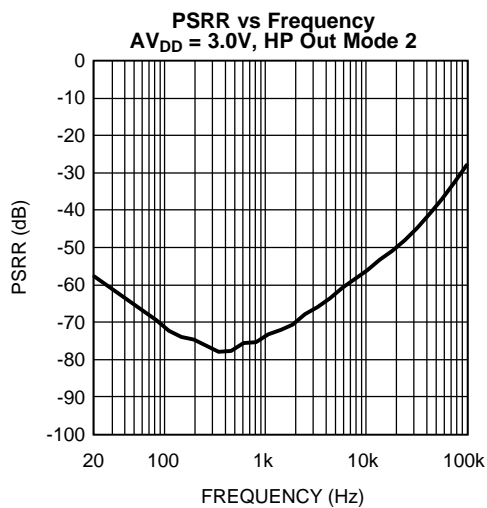


Figure 30.

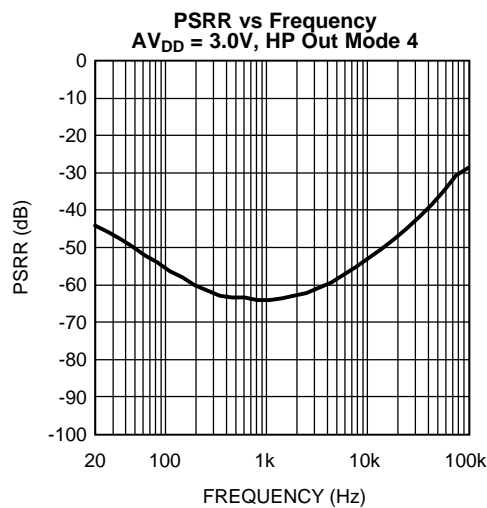


Figure 31.

### Typical Performance Characteristics (continued)

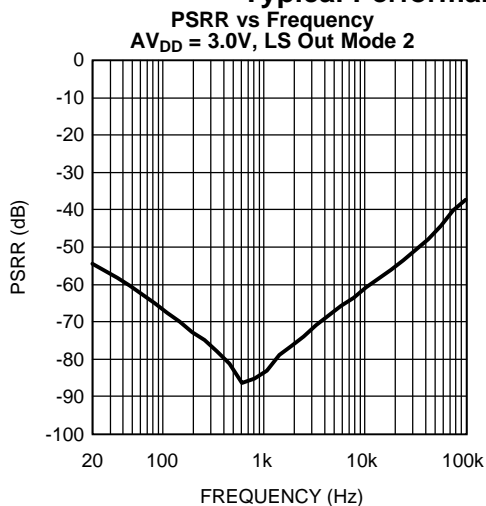


Figure 32.

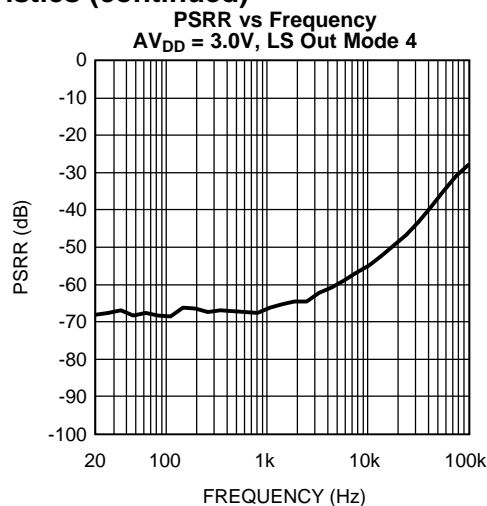


Figure 33.

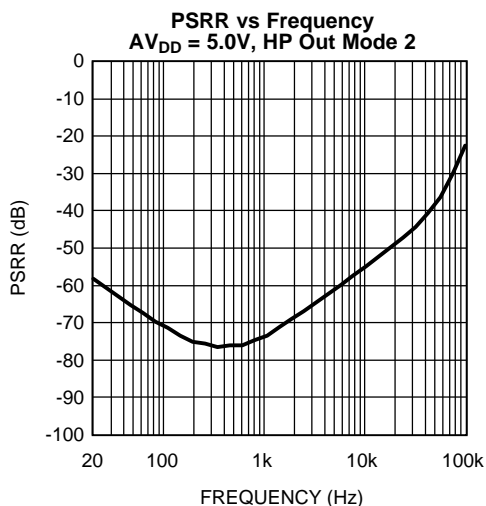


Figure 34.

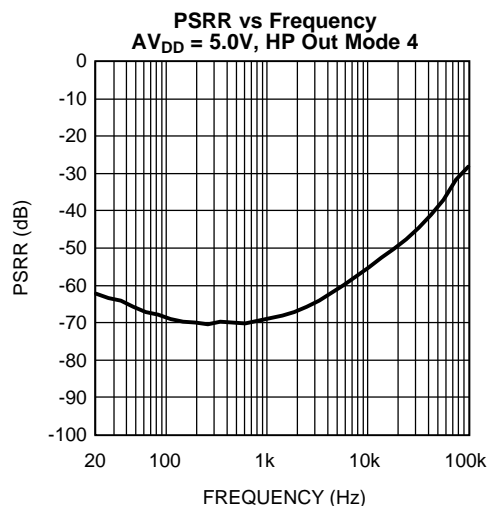


Figure 35.

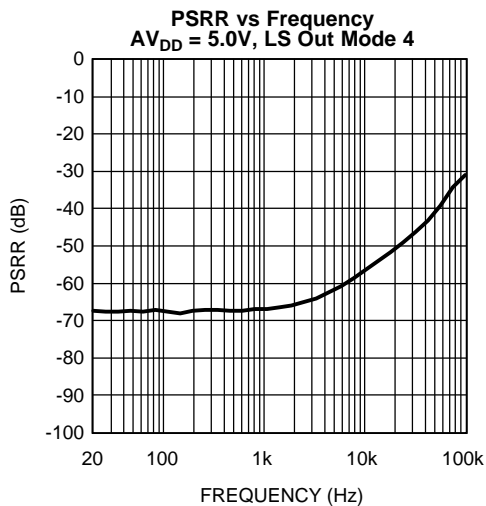


Figure 36.

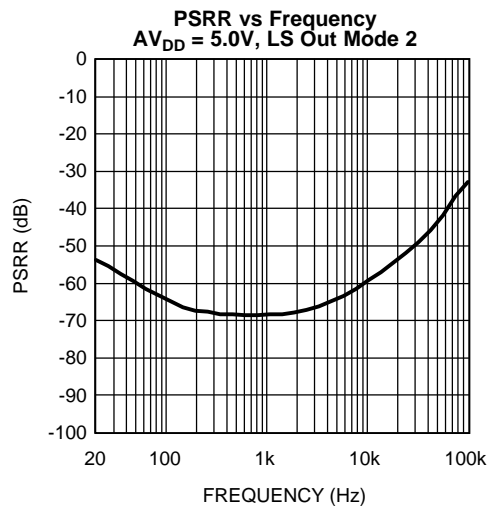


Figure 37.

### Typical Performance Characteristics (continued)

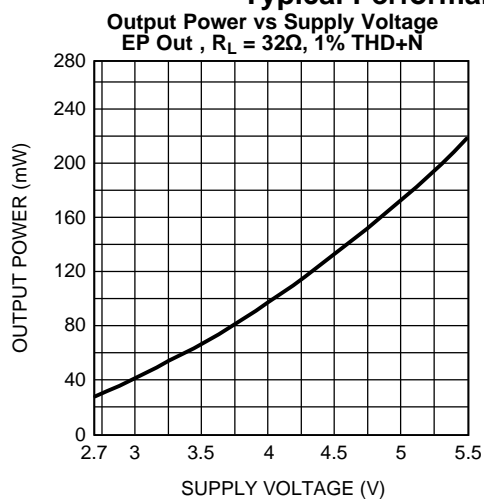


Figure 38.

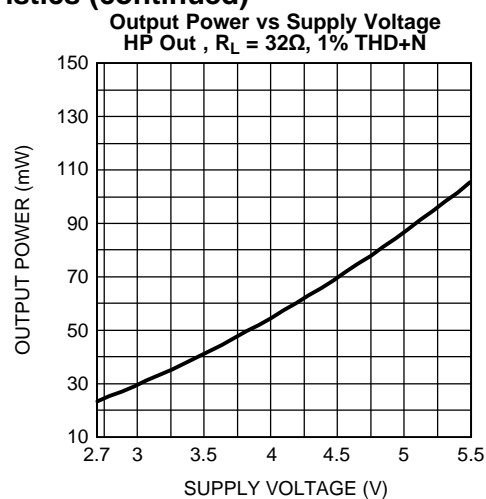


Figure 39.

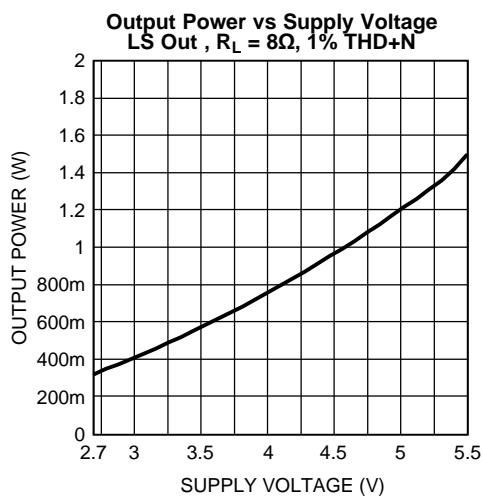
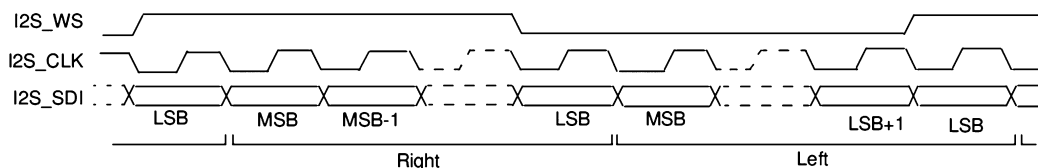


Figure 40.

## APPLICATION INFORMATION

### I<sup>2</sup>S

The LM49321 supports both master and slave I<sup>2</sup>S transmission at either 16 or 32 bits per word at clock rates up to 3.072MHz (48kHz stereo, 32bit). The basic format is shown below:



**Figure 41.**

### MONO ONLY SETTING

The LM49321 may be restricted to mono amplification only by setting MONO\_ONLY in Output Control register 0x01h to 1. This may save an additional 400μA from I<sub>DD</sub>.

### LM49321 DEMOBOARD OPERATION

#### BOARD LAYOUT

#### DIGITAL SUPPLIES

- JP14 — Digital Power DVDD
- JP10 — I/O Power IOVDD
- JP13 — PLL Supply PLLVDD
- JP16 — USB Board Supply BBVDD
- JP15 — I<sup>2</sup>CVDD

All supplies may be set independently. All digital ground is common. Jumpers may be used to connect all the digital supplies together.

- S9 – connects VDD\_PLL to VDD\_D
- S10 – connects VDD\_D to VDD\_IO
- S11 – connects VDD\_IO to VDD\_I2C
- S12 – connects VDD\_I2C to Analog VDD
- S17 – connects BB\_VDD to USB3.3V (from USB board)
- S19 – connects VDD\_D to USB3.3V (from USB board)
- S20 – connects VDD\_D to SPDIF receiver chip

#### ANALOG SUPPLY

- JP11 — Analog Supply
- S12 — connects Analog VDD with Digital VDD (I2C\_VDD)
- S16 — connects Analog Ground with Digital Ground
- S21 — connects Analog VDD to SPDIF receiver chip

## INPUTS

### Analog Inputs

JP2 — Mono Differential Input

JP6 — Left Input

JP7 — Right Input

### Digital Inputs

JP19 — Digital Interface

Pin 1 — MCLK

Pin 2 — I2S\_CLK

Pin 3 — I2S\_SDI

Pin 4 — I<sup>2</sup>S\_WS

JP20 — Toslink SPDIF Input

JP21 — Coaxial SPDIF Input

Coaxial and Toslink inputs may be toggled between by use of S25. Only one may be used at a time. Must be used in conjunction with on-board SPDIF receiver chip.

## OUTPUTS

JP5 — BTL Loudspeaker Output

JP1 — Left Headphone Output (Single-Ended or OCL)

JP3 — Right Headphone Output (Single-Ended or OCL)

P1 — Stereo Headphone Jack (Same as JP1, JP2, Single-Ended or OCL)

JP12 — Mono BTL Earpiece Output

## CONTROL INTERFACE

X1, X2 – USB Control Bus for I<sup>2</sup>C/SPI

X1

Pin 9 – Mode Select (SPI or I<sup>2</sup>C)

X2

Pin 1 – SDA

Pin 3 – SCL

Pin 15 – ADDR/END

Pin 14 – USB5V

Pin 16 – USB3.3V

Pin 16 – USB GND

## MISCELLANEOUS

### I<sup>2</sup>S BUS SELECT

S23, S24, S26, S27 – I<sup>2</sup>S Bus select. Toggles between on-board and external I<sup>2</sup>S (whether on-board SPDIF receiver is used). All jumpers must be set the same. Jumpers on top two pins selects external bus (JP19). Jumpers on bottom two pins selects on-board SPDIF receiver output.

## HEADPHONE OUTPUT CONFIGURATION

Jumpers S1, S2, S3, and S4 are used to configure the headphone outputs for either cap-coupled outputs or output capacitorless (OCL) mode in addition to the register control internal to the LM49321 for this feature. Jumpers S1 and S3 bypass the output DC blocking capacitors when OCL mode is required. S2 connects the center amplifier HPCOUT to the headphone ring when in OCL mode. S4 connects the center ring to GND when cap-coupled mode is desired. S4 must be removed for OCL mode to function properly. Jumper settings for each mode:

### OCL

S1 = ON

S2 = ON

S3 = ON

S4 = OFF

### Cap-Coupled

S1 = OFF

S2 = OFF

S3 = OFF

S4 = ON

## PLL FILTER CONFIGURATION

The LM49321 demo board comes with a simple filter setup by connecting jumpers S5 and S6. Removing these and connecting jumpers S7 and S8 will allow for an alternate PLL filter configuration to be used at R2 and C23.

## ON-BOARD SPDIF RECEIVER

The SPDIF receiver present on the LM49321 demo board allows quick demonstration of the capabilities of the LM49321 by using the common SPDIF output found on most CD/DVD players today. There are some limitations in its usage, as the receiver will not work with digital supplies of less than 3.0V and analog supplies of less than 4V. This means low analog supply voltage testing of the LM49321 must be done on the external digital bus.

The choice of using on-board or external digital bus is made using jumpers S23, S24, S26, and S27 as described above.

S25 selects whether the Toslink or Coaxial SPDIF input is used. The top two pins connects the toslink, the bottom two connect the coaxial input.

Power on the digital side is routed through S20 (connecting to the other digital supplies), while on the analog side it is interrupted by S21. Both jumpers must be in place for the receiver to function. The part is already configured for I<sup>2</sup>S standard outputs. Jumper S28 allows the DATA output to be pulled either high or low. Default is high (jumper on right two pins).

It may be necessary to quickly toggle S29 to reset the receiver and start it working upon initial power up. A quick short across S29 should clear this condition.

## LM49321 I<sup>2</sup>C/SPI INTERFACE SOFTWARE

Convenient graphical user interface software is available for demonstration purposes of the LM49321. It allows for either SPI or I<sup>2</sup>C control via either USB or parallel port connections to a Windows computer. Control options include all mode and output settings, volume controls, PLL and DAC setup, FIR setting and on-the-fly adjustment by an easy to use graphical interface. An advanced option is also present to allow direct, register-level commands. Software is available from [www.ti.com](http://www.ti.com) and is compatible with Windows operating systems of Windows 98 or more (with USB support) with the latest .NET updates from Microsoft.

## Demonstration Board Schematic

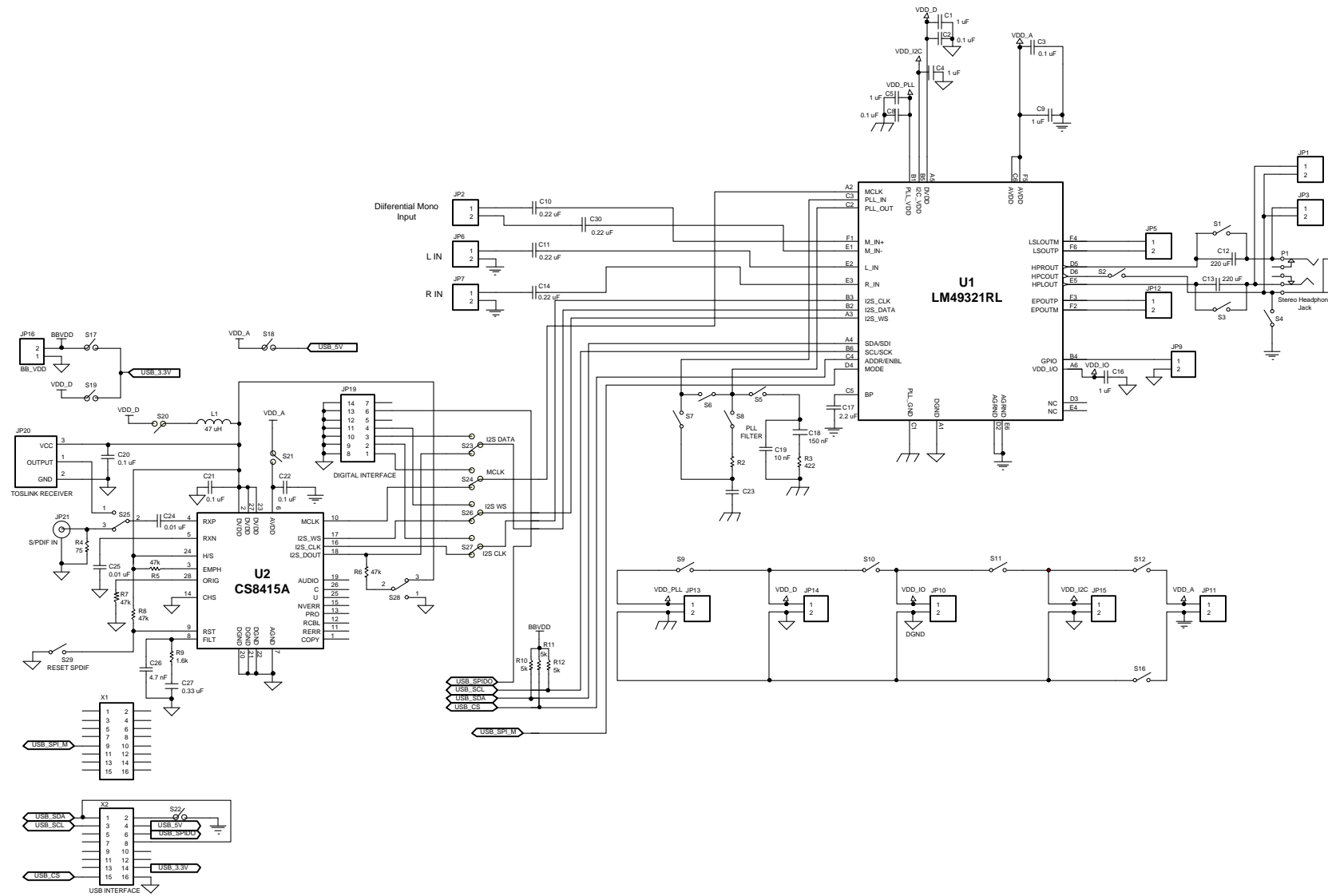
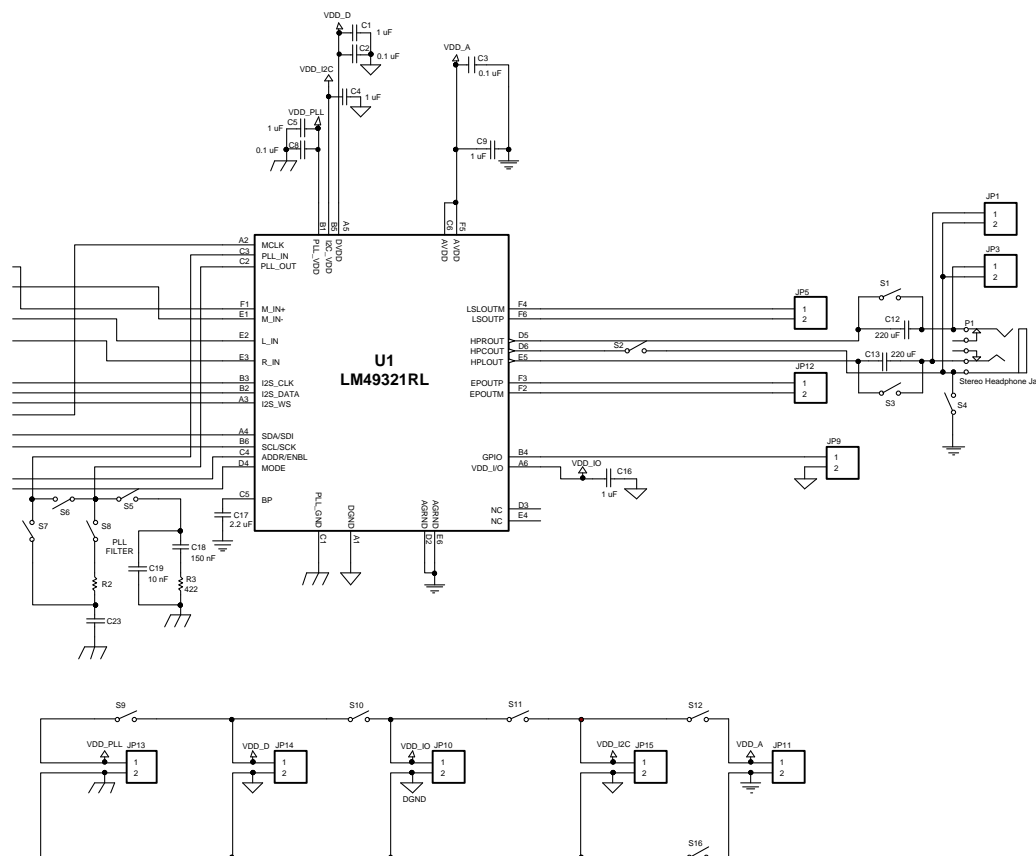


Figure 42. Complete Board Schematic





**Figure 44. Enlarged Board Schematic Part 2 of 2**

### Revision History

| Rev  | Date     | Description   |
|------|----------|---|
| 1.0  | 09/10/08 | Initial release.                                    |
| 1.01 | 09/23/08 | Text edits.   |
| 1.02 | 08/31/09 | Edited the package drawing and the top markings.    |
| C    | 05/03/13 | Changed layout of National Data Sheet to TI format. |

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish | MSL Peak Temp<br>(3) | Op Temp (°C) | Top-Side Markings<br>(4) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| LM49321RL/NOPB   | ACTIVE        | DSBGA        | YPG                | 36   | 250            | Green (RoHS<br>& no Sb/Br) | SNAG             | Level-1-260C-UNLIM   | -40 to 85    | GK9                      | <a href="#">Samples</a> |
| LM49321RLX/NOPB  | ACTIVE        | DSBGA        | YPG                | 36   | 1000           | Green (RoHS<br>& no Sb/Br) | SNAG             | Level-1-260C-UNLIM   | -40 to 85    | GK9                      | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

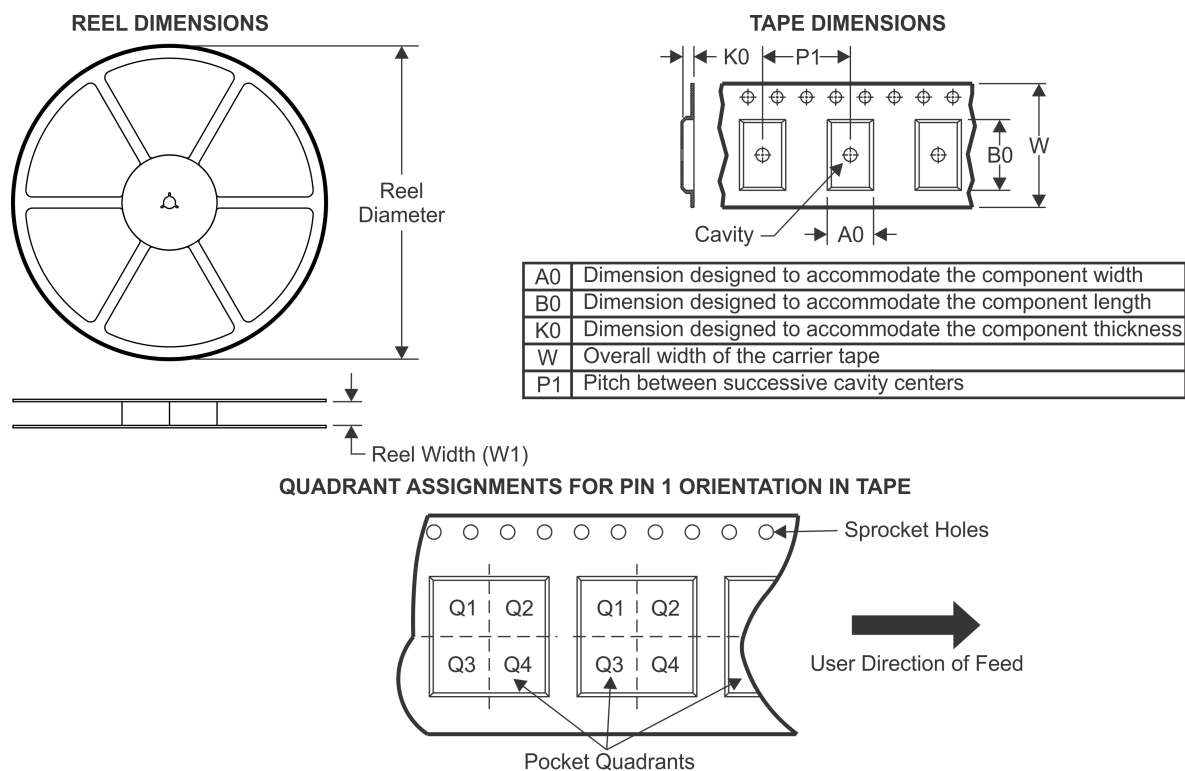
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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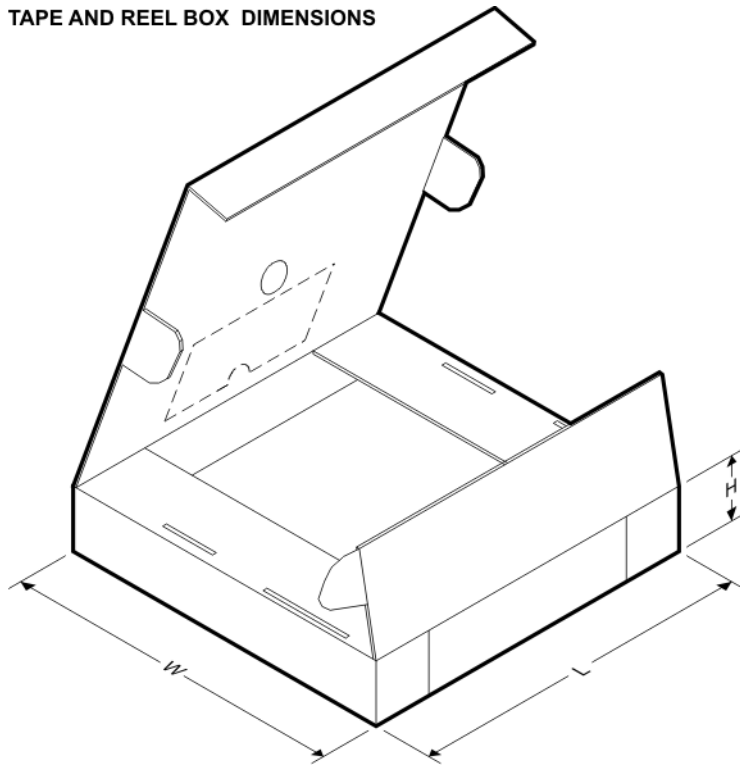
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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LM49321RL/NOPB  | DSBGA        | YPG             | 36   | 250  | 178.0              | 12.4               | 3.43    | 3.59    | 0.76    | 8.0     | 12.0   | Q1            |
| LM49321RLX/NOPB | DSBGA        | YPG             | 36   | 1000 | 178.0              | 12.4               | 3.43    | 3.59    | 0.76    | 8.0     | 12.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LM49321RL/NOPB  | DSBGA        | YPG             | 36   | 250  | 210.0       | 185.0      | 35.0        |
| LM49321RLX/NOPB | DSBGA        | YPG             | 36   | 1000 | 210.0       | 185.0      | 35.0        |



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